

## GENERAL DESCRIPTION

OB2269C is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications.

PWM switching frequency at normal operation is externally programmable and trimmed to tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved.

VDD low startup current and low operating current contribute to a reliable power on startup design with OB2269C. A large value resistor could thus be used in the startup circuit to minimize the standby power.

The internal slope compensation improves system large signal stability and reduces the possible sub-harmonic oscillation at high PWM duty cycle output. Leading-edge blanking on current sense input removes the signal glitch due to snubber circuit diode reverse recovery. This greatly helps to reduce the external component count and system cost in application.

OB2269C offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), over temperature protection (OTP), VDD over voltage protection (OVP) and under voltage lockout (UVLO). The Gate-drive output is clamped at 18V to protect the power MOSFET.

In OB2269C, OCP threshold slope is internally optimized to reach constant output power limit over universal AC input range.

Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique together with soft switching control at the totem pole gate drive output.

The tone energy at below 20KHZ is minimized in operation. Consequently, audio noise performance is greatly improved.

OB2269C is offered in both SOP-8 and DIP-8 packages.

## FEATURES

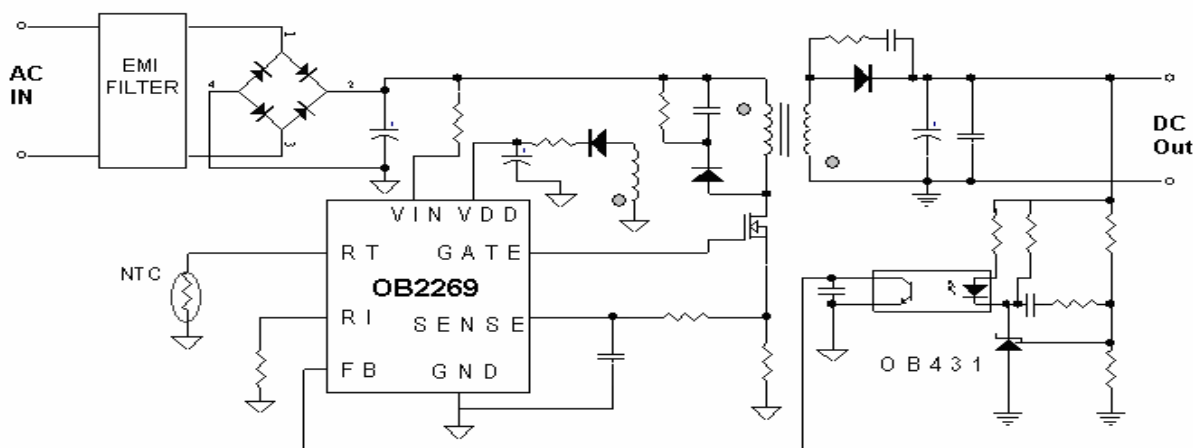
- On-Bright Proprietary Frequency Shuffling Technology for Improved EMI Performance
- Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design
- Audio Noise Free Operation
- External Programmable PWM Switching Frequency
- Internal Synchronized Slope Compensation
- Low VIN/VDD Startup Current(6.5uA) and Low Operating Current (2.3mA)
- Leading Edge Blanking on Current Sense Input
- Complete Protection Coverage With Auto Self-Recovery
  - External Programmable Over Temperature Protection (OTP)
  - With or Without On-chip VDD OVP for System OVP
  - Under Voltage Lockout with Hysteresis (UVLO)
  - Gate Output Maximum Voltage Clamp (18V)
  - Line Compensated Cycle-by-Cycle Over-current Threshold Setting For Constant Output Current Limiting Over Universal Input Voltage Range (OCP)
  - Over Load Protection. (OLP)

## APPLICATIONS

Offline AC/DC flyback converter for

- PC/TV/Set-Top Box Power Supplies
- Open-frame SMPS
- Battery Charger

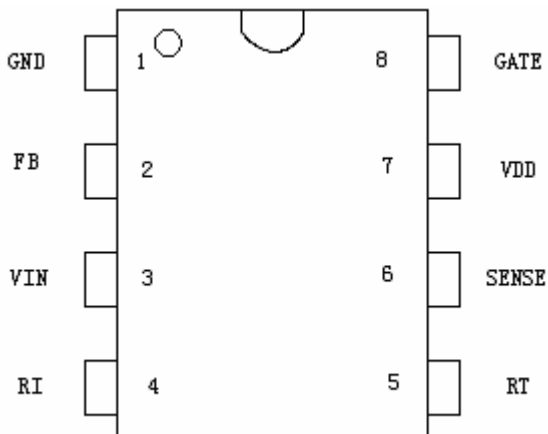
## TYPICAL APPLICATION



## GENERAL INFORMATION

### Pin Configuration

The OB2269C is offered in DIP and SOP packages shown as below.



### Ordering Information

| Part Number | Description                                     |
|-------------|-------------------------------------------------|
| OB2269CAP   | With Frequency Shuffling, DIP8, Pb-free         |
| OB2269CAPV  | With Frequency Shuffling, DIP8, Pb-free, no OVP |
| OB2269CCP   | With Frequency Shuffling, SOP8, Pb-free         |
| OB2269CCPV  | With Frequency Shuffling, SOP8, Pb-free, no OVP |

### Package Dissipation Rating

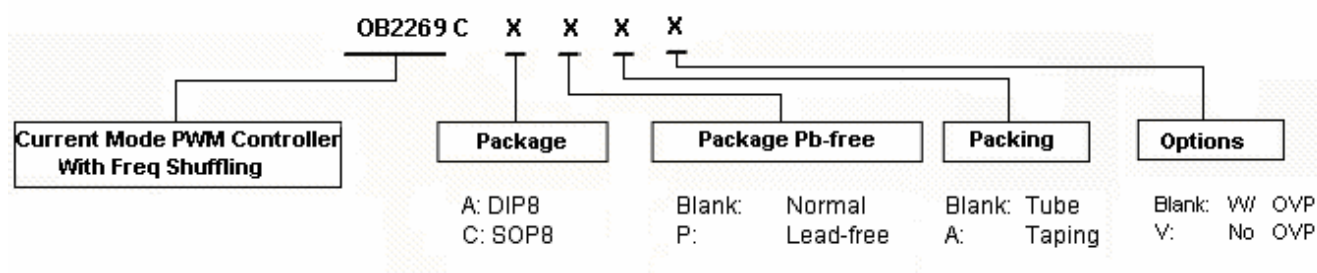
| Package | R $\theta$ JA (°C/W) |
|---------|----------------------|
| DIP8    | 90                   |
| SOP8    | 150                  |

### Absolute Maximum Ratings

| Parameter                                             | Value          |
|-------------------------------------------------------|----------------|
| VDD/VIN DC Supply Voltage                             | 30 V           |
| VDD Zener Clamp Voltage <sup>Note</sup>               | VDD_Clamp+0.1V |
| VDD Clamp Continuous Current                          | 10 mA          |
| V <sub>FB</sub> Input Voltage                         | -0.3 to 7V     |
| V <sub>SENSE</sub> Input Voltage to Sense Pin         | -0.3 to 7V     |
| V <sub>RT</sub> Input Voltage to RT Pin               | -0.3 to 7V     |
| V <sub>RI</sub> Input Voltage to RI Pin               | -0.3 to 7V     |
| Min/Max Operating Junction Temperature T <sub>J</sub> | -20 to 150 °C  |
| Min/Max Storage Temperature T <sub>stg</sub>          | -55 to 150 °C  |
| Lead Temperature (Soldering, 10secs)                  | 260 °C         |

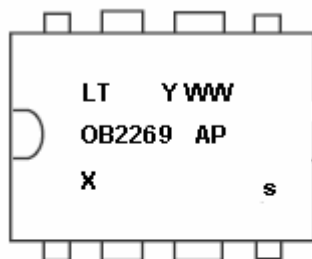
**Note:** VDD\_Clamp has a nominal value of 35V.

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



## Marking Information

DIP8



X: Version Num (X=C)  
A: DIP8 Package  
P: Pb-free Package (norm if left Blank)  
Y: Year Code(0-9)  
WW: Week Code(01-52)  
S: Internal Control Code(optional)

SOP8

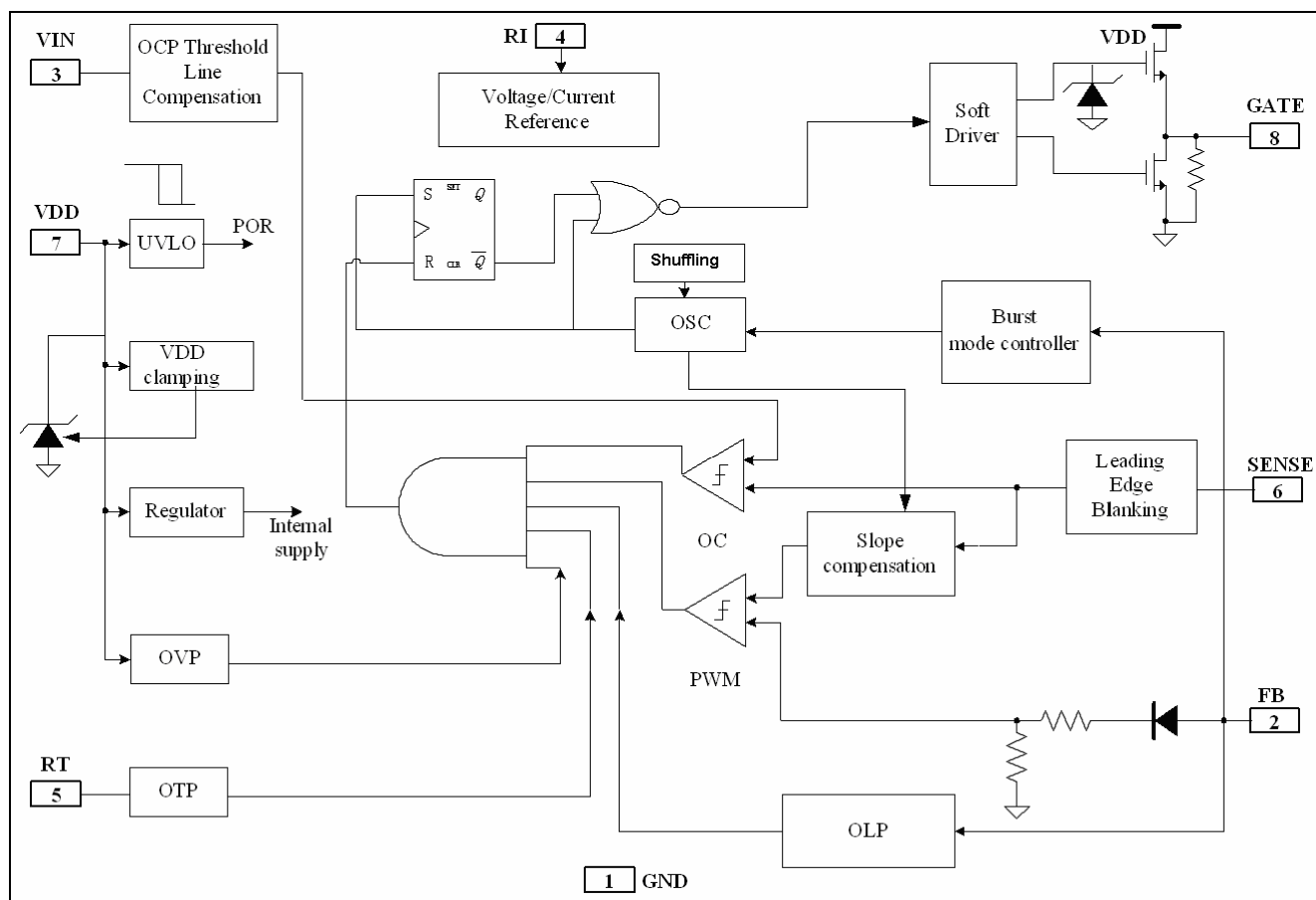


X: Version Num (X=C)  
C: SOP8 Package  
P: Pb-free Package (norm if left Blank)  
Y: Year Code(0-9)  
WW: Week Code(01-52)  
S: Internal Control Code(optional)

## TERMINAL ASSIGNMENTS

| Pin Num | Pin Name | I/O | Description                                                                                                              |
|---------|----------|-----|--------------------------------------------------------------------------------------------------------------------------|
| 1       | GND      | P   | Ground                                                                                                                   |
| 2       | FB       | I   | Feedback input pin. PWM duty cycle is determined by voltage level into this pin and current-sense signal level at Pin 6. |
| 3       | VIN      | I   | Connected through a large value resistor to rectified line input for Startup IC supply and line voltage sensing.         |
| 4       | RI       | I   | Internal Oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.               |
| 5       | RT       | I   | Temperature sensing input pin. Connected through a NTC resistor to GND.                                                  |
| 6       | SENSE    | I   | Current sense input pin. Connected to MOSFET current sensing resistor node.                                              |
| 7       | VDD      | P   | DC power supply pin.                                                                                                     |
| 8       | GATE     | O   | Totem-pole gate drive output for power MOSFET.                                                                           |

## BLOCK DIAGRAM



## RECOMMENDED OPERATING CONDITION

| Symbol         | Parameter                     | Min | Max | Unit |
|----------------|-------------------------------|-----|-----|------|
| VDD            | VDD Supply Voltage            | 12  | 23  | V    |
| RI             | RI Resistor Value             | 24  | 31  | Kohm |
| T <sub>A</sub> | Operating Ambient Temperature | -20 | 85  | °C   |

## ESD INFORMATION

| Symbol              | Parameter                                       | Test Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------------------|-----------------|-----|-----|-----|------|
| HBM <sup>Note</sup> | Human Body Model on All Pins Except VIN and VDD | MIL-STD         |     | 3   |     | KV   |
| MM                  | Machine Model on All Pins                       | JEDEC-STD       |     | 250 |     | V    |

**Note:** HBM all pins pass 3KV except High Voltage Input pin. The details are VIN passes 1kV, VDD passes 1.5KV, all other I/Os pass 3KV. In system application, High Voltage Input pin is either a high impedance input or connected to a cap. The lower rating has minimum impacts on system ESD performance.

## ELECTRICAL CHARACTERISTICS

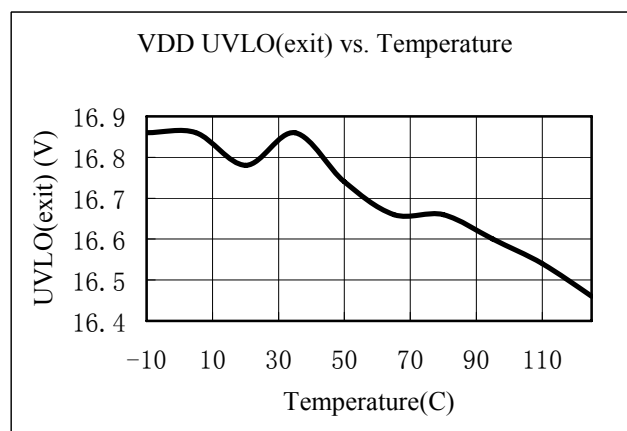
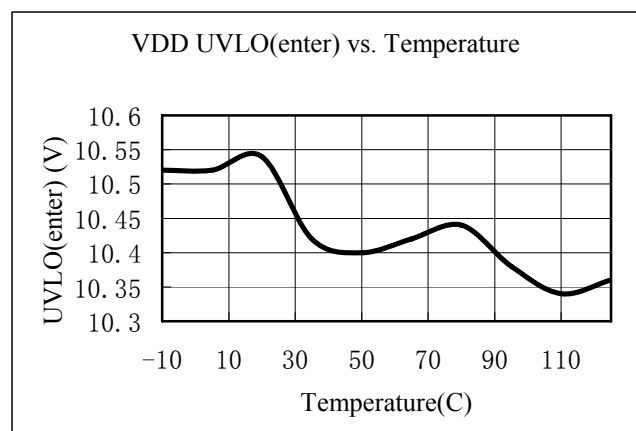
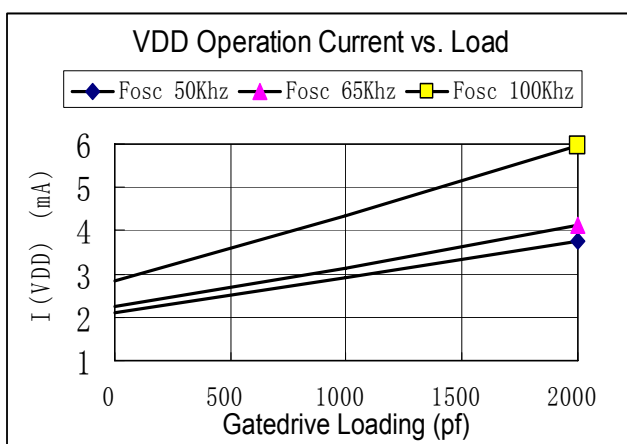
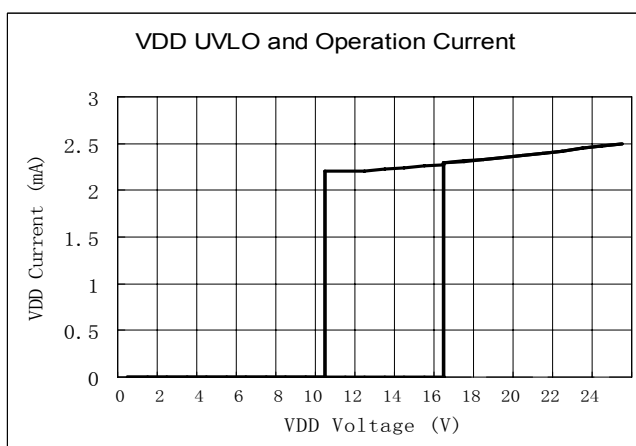
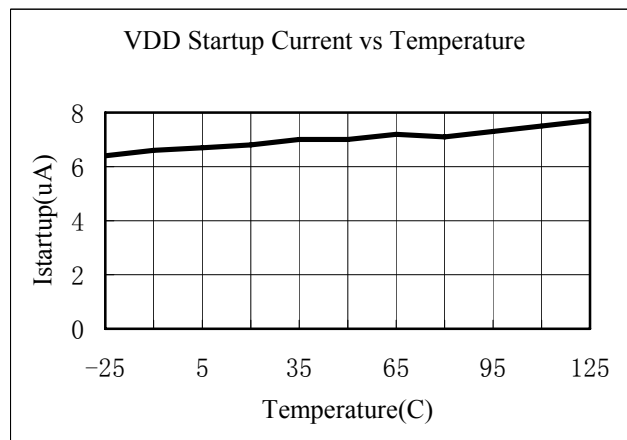
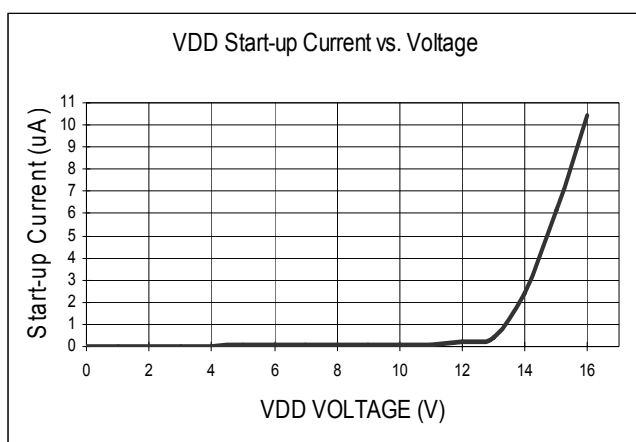
(T<sub>A</sub> = 25°C, VDD=16V, R<sub>I</sub>=24Kohm if not otherwise noted)

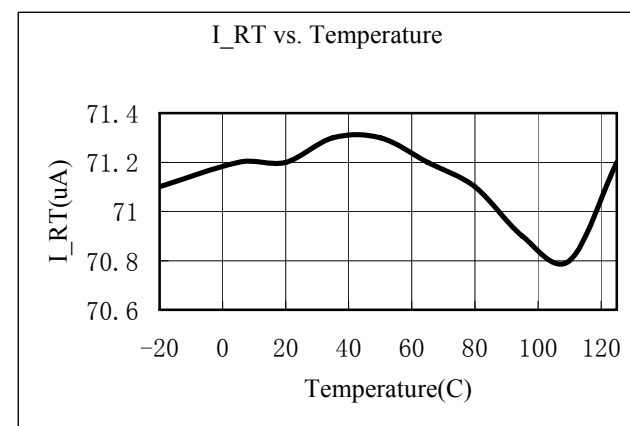
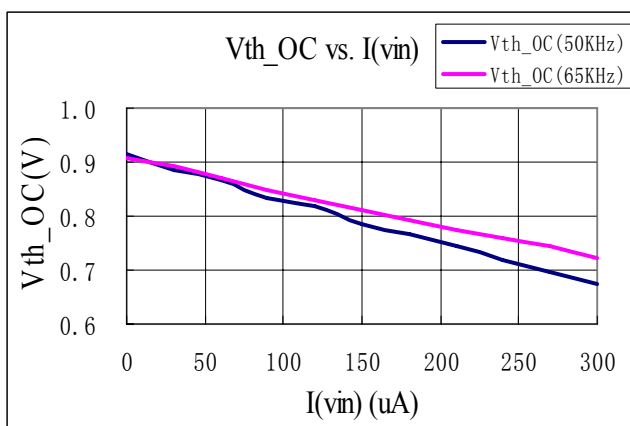
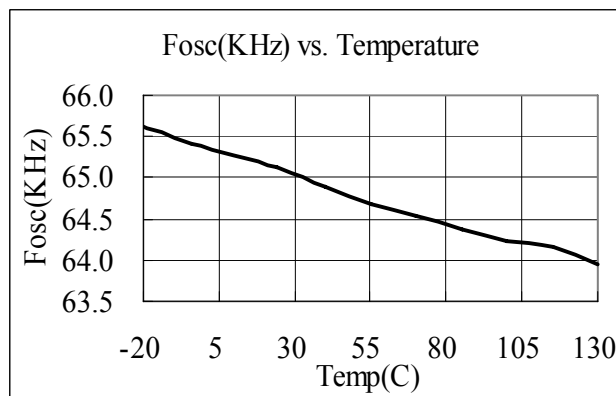
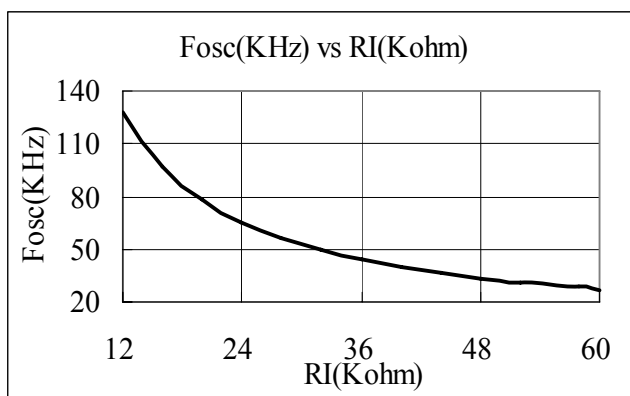
| Symbol                                | Parameter                                   | Test Conditions                      | Min  | Typ  | Max  | Unit |
|---------------------------------------|---------------------------------------------|--------------------------------------|------|------|------|------|
| <b>Supply Voltage (VDD)</b>           |                                             |                                      |      |      |      |      |
| I_VDD_Startup                         | VDD Start up Current                        | VDD=15V, Measure current into VDD    |      | 6.5  | 20   | uA   |
| I_VDD_Operation                       | Operation Current                           | V <sub>FB</sub> =3V                  |      | 2.3  |      | mA   |
| UVLO(Enter)                           | VDD Under Voltage Lockout Enter             |                                      | 9.5  | 10.5 | 11.5 | V    |
| UVLO(Exit)                            | VDD Under Voltage Lockout Exit (Startup)    |                                      | 15.5 | 16.5 | 17.5 | V    |
| OVP(ON) <sup>*Optional</sup>          | VDD Over Voltage Protection Enter           |                                      | 23.5 | 25   | 26.5 | V    |
| OVP(OFF) <sup>*Optional</sup>         | VDD Over Voltage Protection Exit (Recovery) |                                      | 21.5 | 23   | 24.5 | V    |
| OVP_Hys <sup>*Optional</sup>          | OVP Hysteresis                              | OVP(ON)-OVP(OFF)                     |      | 2    |      | V    |
| T <sub>D_OVP</sub>                    | VDD OVP Debounce time                       |                                      |      | 80   |      | uSec |
| V <sub>DD_Clamp</sub>                 | V <sub>DD</sub> Zener Clamp Voltage         | I(V <sub>DD</sub> ) = 5mA            |      | 35   |      | V    |
| <b>Feedback Input Section(FB Pin)</b> |                                             |                                      |      |      |      |      |
| A <sub>VCS</sub>                      | PWM Input Gain                              | $\Delta V_{FB} / \Delta V_{CS}$      |      | 2.8  |      | V/V  |
| V <sub>FB_Open</sub>                  | V <sub>FB</sub> Open Voltage                |                                      |      | 5.9  |      | V    |
| I <sub>FB_Short</sub>                 | FB pin short circuit current                | Short FB pin to GND, measure current |      | 0.80 |      | mA   |
| V <sub>TH_0D</sub>                    | Zero Duty Cycle FB Threshold Voltage        |                                      |      |      | 0.95 | V    |
| V <sub>TH_BM</sub>                    | Burst Mode FB Threshold Voltage             |                                      |      | 1.7  |      | V    |
| V <sub>TH_PL</sub>                    | Power Limiting FB Threshold Voltage         |                                      |      | 4.4  |      | V    |
| T <sub>D_PL</sub>                     | Power limiting Debounce Time                |                                      |      | 80   |      | mSec |
| Z <sub>FB_IN</sub>                    | Input Impedance                             |                                      |      | 7.2  |      | Kohm |
| <b>Current Sense Input(Sense Pin)</b> |                                             |                                      |      |      |      |      |
| T <sub>blanking</sub>                 | Sense Input Leading Edge Blanking Time      |                                      |      | 250  |      | nS   |
| Z <sub>SENSE_IN</sub>                 | Sense Input                                 |                                      |      | 30   |      | Kohm |

Current Mode PWM Controller<sup>Frequency Shuffling</sup>

|                                    |                                               |                         |       |       |       |      |
|------------------------------------|-----------------------------------------------|-------------------------|-------|-------|-------|------|
|                                    | Impedance                                     |                         |       |       |       |      |
| T <sub>D_OC</sub>                  | Over Current Detection and Control Delay      | CL=1nf at GATE,         |       | 120   |       | nSec |
| V <sub>TH_OC_0</sub>               | Current Limiting Threshold at No Compensation | I(VIN) = 0uA            | 0.85  | 0.90  | 0.95  | V    |
| V <sub>TH_OC_1</sub>               | Current Limiting Threshold at Compensation    | I(VIN) = 150uA          |       | 0.81  |       | V    |
| <b>Oscillator</b>                  |                                               |                         |       |       |       |      |
| F <sub>OSC</sub>                   | Normal Oscillation Frequency                  |                         | 60    | 65    | 70    | KHZ  |
| Δf_Temp                            | Frequency Temperature Stability               | -20°C to 100°C          |       | 2     |       | %    |
| Δf_VDD                             | Frequency Voltage Stability                   | VDD = 12-25V            |       | 2     |       | %    |
| RI_range                           | Operating RI Range                            |                         | 12    | 24    | 60    | Kohm |
| V <sub>RI_open</sub>               | RI open voltage                               |                         |       | 2.0   |       | V    |
| F <sub>BM</sub>                    | Burst Mode Base Frequency                     |                         |       | 22    |       | KHZ  |
| DC_max                             | Maximum Duty Cycle                            |                         | 75    | 80    | 85    | %    |
| DC_min                             | Minimum Duty Cycle                            |                         | -     | -     | 0     | %    |
| <b>Gate Drive Output</b>           |                                               |                         |       |       |       |      |
| VOL                                | Output Low Level                              | I <sub>o</sub> = -20 mA |       |       | 0.3   | V    |
| VOH                                | Output High Level                             | I <sub>o</sub> = +20 mA | 11    |       |       | V    |
| VG_Clamp                           | Output Clamp Voltage Level                    | VDD=20V                 |       | 18    |       | V    |
| T <sub>r</sub>                     | Output Rising Time                            | CL = 1nf                |       | 120   |       | nSec |
| T <sub>f</sub>                     | Output Falling Time                           | CL = 1nf                |       | 50    |       | nSec |
| <b>Over Temperature Protection</b> |                                               |                         |       |       |       |      |
| I <sub>RT</sub>                    | Output Current of RT pin                      |                         |       | 70    |       | uA   |
| V <sub>TH_OTP</sub>                | OTP Threshold Voltage                         |                         | 1.015 | 1.065 | 1.115 | V    |
| V <sub>TH_OTP_off</sub>            | OTP Recovery Threshold Voltage                |                         |       | 1.165 |       | V    |
| T <sub>D_OTP</sub>                 | OTP De-bounce Time                            |                         |       | 100   |       | uSec |
| V <sub>RT_Open</sub>               | RT Pin Open Voltage                           |                         |       | 3.5   |       | V    |
| <b>Frequency Shuffling</b>         |                                               |                         |       |       |       |      |
| Δf <sub>OSC</sub>                  | Frequency Modulation range /Base frequency    |                         | -3    |       | 3     | %    |
| Freq_Shuffling                     | Shuffling Frequency                           | RI = 24Kohm             |       | 32    |       | HZ   |

## CHARACTERIZATION PLOTS







## OPERATION DESCRIPTION

The OB2269C is a highly integrated PWM controller IC optimized for offline flyback converter applications. The extended burst mode control greatly reduces the standby power consumption and helps the design easily meet the international power conservation requirements.

### ● Startup Current and Start up Control

Startup current of OB2269C is designed to be very low so that VDD could be charged up above UVLO(exit) threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application. For a typical AC/DC adaptor with universal input range design, a 2 MΩ, 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and yet low power dissipation design solution.

### ● Operating Current

The Operating current of OB2269C is low at 2.3mA. Good efficiency is achieved with OB2269C low operating current together with extended burst mode control schemes.

### ● Frequency shuffling for EMI improvement

The frequency Shuffling/jittering (switching frequency modulation) is implemented in OB2269C. The oscillation frequency is modulated with a internally generated random source so that the tone energy is evenly spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design in meeting stringent EMI requirement.

### ● Burst Mode Operation

At zero load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy. OB2269C self adjusts the switching mode according to the loading condition. At from no load to light/medium load condition, the FB input drops below burst mode threshold level (1.8V). Device enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state

to minimize the switching loss thus reduce the standby power consumption to the greatest extend. The nature of high frequency switching also reduces the audio noise at any loading conditions.

### ● Oscillator Operation

A resistor connected between RI and GND sets the constant current source to charge/discharge the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation within the specified RI in Kohm range at nominal loading operational condition.

$$F_{osc} = \frac{1560}{RI(Kohm)} (Khz)$$

### ● Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in OB2269C current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber diode reverse recovery so that the external RC filtering on sense input is no longer required. The current limit comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

### ● Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

### ● Over Temperature Protection

A NTC resistor in series with a regular resistor should connect between RT and GND for temperature sensing and protection. NTC resistor value becomes lower when the ambient temperature rises. With the fixed internal current  $I_{RT}$  flowing through the resistors, the voltage at RT pin becomes lower at high temperature. The internal OTP circuit is triggered and shutdown the MOSFET when the sensed input voltage is lower than  $V_{TH\_OTP}$ .

### ● Gate Drive

OB2269C Gate is connected to the Gate of an external MOSFET for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI.

Good tradeoff is achieved through the built-in totem pole gate drive design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 18V clamp is added for MOSFET gate protection at higher than expected VDD input.

#### ● **Protection Controls**

Good system reliability is achieved with OB2269C's rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP), over temperature protection (OTP), on-chip VDD over voltage protection (OVP, optional) and under voltage lockout (UVLO).

The OCP threshold value is self adjusted lower at higher current into VIN pin. This OCP threshold slope adjustment helps to compensate the increased output power limit at higher AC voltage caused by inherent Over-Current sensing and control delay. A constant output power limit is achieved with recommended OCP compensation scheme on OB2269C.

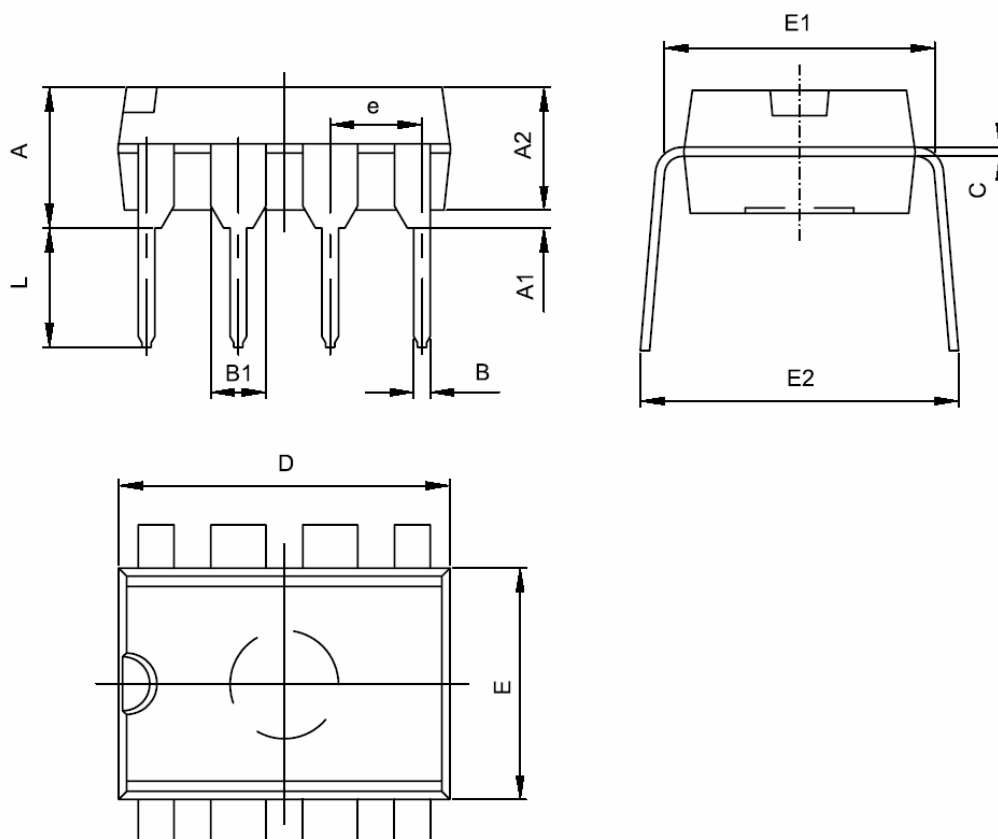
At output overload condition, FB voltage is biased higher. When FB input exceeds power limit threshold value for more than 80mS, control circuit reacts to turnoff the power MOSFET.

Similarly, control circuit shutdowns the power MOSFET when an Over Temperature condition is detected. OB2269C resumes the operation when temperature drops below the hysteresis value.

VDD is supplied with transformer auxiliary winding output. It is clamped when VDD is higher than 35V. MOSFET is shut down when VDD drops below UVLO(enter) limit and device enters power on startup sequence thereafter.

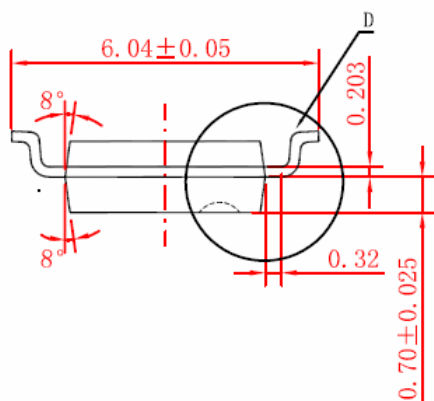
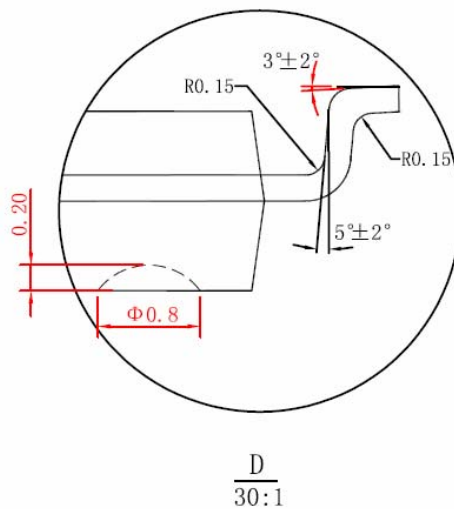
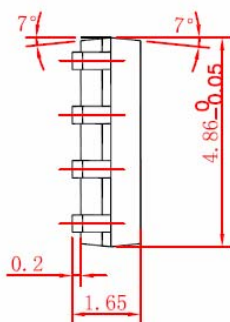
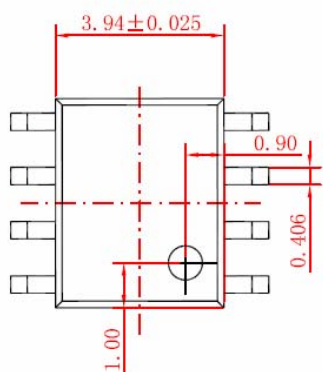
## PACKAGE MECHANICAL DATA

### 8-Pin Plastic DIP



| Symbol | Dimensions In Millimeters |       | Dimensions In Inches |       |
|--------|---------------------------|-------|----------------------|-------|
|        | Min                       | Max   | Min                  | Max   |
| A      | 3.710                     | 4.310 | 0.146                | 0.170 |
| A1     | 0.510                     |       | 0.020                |       |
| A2     | 3.200                     | 3.600 | 0.126                | 0.142 |
| B      | 0.360                     | 0.560 | 0.014                | 0.022 |
| B1     | 1.524(TYP)                |       | 0.060(TYP)           |       |
| C      | 0.204                     | 0.360 | 0.008                | 0.014 |
| D      | 9.000                     | 9.400 | 0.354                | 0.370 |
| E      | 6.200                     | 6.600 | 0.244                | 0.260 |
| E1     | 7.620(TYP)                |       | 0.300(TYP)           |       |
| e      | 2.540(TYP)                |       | 0.100(TYP)           |       |
| L      | 3.000                     | 3.600 | 0.118                | 0.142 |
| E2     | 8.200                     | 9.400 | 0.323                | 0.370 |

## 8-Pin Plastic SOP



## **IMPORTANT NOTICE**

### **RIGHT TO MAKE CHANGES**

On-Bright Electronics Corp. reserves the right to make corrections, modifications, enhancements, improvements and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

### **WARRANTY INFORMATION**

On-Bright Electronics Corp. warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with its standard warranty. Testing and other quality control techniques are used to the extent it deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

On-Bright Electronics Corp. assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using On-Bright's components, data sheet and application notes. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

### **LIFE SUPPORT**

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