PRODUCT DATA SHEET

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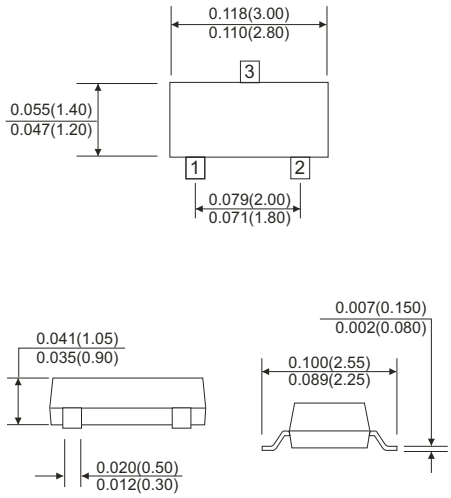
Datasheet Resources Samples

Please note: Please check the JINGAO Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.jg-semi.cn. Please email any questions regarding the system integration to JINGAO_questions@jgsemi.com.

$V_{(BR)DSS}$	$R_{DS(on)}$MAX	I_D
100V	234mΩ @ 10V	0.2A
	267mΩ @ 6V	
	278mΩ @ 4.5V	

SOT-23



Dimensions in inches and (millimeter)

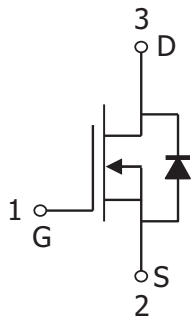
Features

- Low $R_{DS(ON)}$.
- Surface mount package.

Mechanical data

- Case: SOT-23, molded plastic.

Circuit diagram



1. GATE
2. SOURCE
3. DRAIN

Absolute Maximum Ratings (at Ta=25 °C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	100	V
Gate-source voltage	V_{GS}	±20	V
Continuous drain current	I_D	0.2	A
Pulsed drain current	I_{DM}*	0.8	A
Power dissipation	P_D	350	mW
Thermal resistance from junction to ambient	$R_{\Theta JA}$	357	°C/W
Junction temperature	T_J	-40 to +150	°C
Storage temperature	T_{STG}	-55 to +150	°C
Lead temperature for soldering purposes(1/8" form case for 10 s)	T_L	260	°C

* Repetitive rating: Pulse width limited by junction temperature.

Electrical Characteristics (at T_A=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	V_{GS} = 0V , I_D = 250μA	100			V
Zero gate voltage drain current	I_{DSS}	V_{DS} = 100V , V_{GS} = 0V			1	μA
Gate-body leakage current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
Gate threshold voltage (note 1)	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 250μA	-3.0		-1.8	V
Drain-source on-resistance (note 1)	$R_{DS(on)}$	V_{GS} = 10V , I_D = 1.5A			234	mΩ
		V_{GS} = 6V , I_D = 1A			267	
		V_{GS} = 4.5V , I_D = 0.5A			278	
Forward transconductance (note 1)	g_{FS}	V_{DS} = 20V , I_D = 1.5A		2		S
Diode forward voltage (note 1)	V_{SD}	I_S = 1.3A , V_{GS} = 0V			1.2	V
DYNAMIC PARAMETERS (note2)						
Input capacitance	C_{iss}	V_{DS}=50V , V_{GS}=0V, f=1MHz		190		pF
Output capacitance	C_{oss}			22		
Reverse transfer capacitance	C_{rss}			13		
Gate resistance	Rg	F=1MHz	0.3		2.8	Ω
SWITCHING PARAMETERS (note2)						
Turn-on delay time	$t_{d(on)}$	V_{DD}=50V, V_{GEN}=4.5V R_L=39Ω , R_G=1Ω, I_D=1.3A			45	nS
Turn-on rise time	t_r				39	
Turn-off delay time	$t_{d(off)}$				26	
Turn-on fall time	t_f				20	
Total gate charge	Q_g	V_{DS}=50V , V_{GS}=4.5V I_D=1.6A			5.8	nC
Gate-source charge	Q_{gs}			0.75		
Gate-drain charge	Q_{gd}			1.4		

Note:

1. Pulse test : Pulse width≤300μs, duty cycle≤0.5% .
2. Guaranteed by design, not subject to production testing.

Fig.1 - Output Characteristics

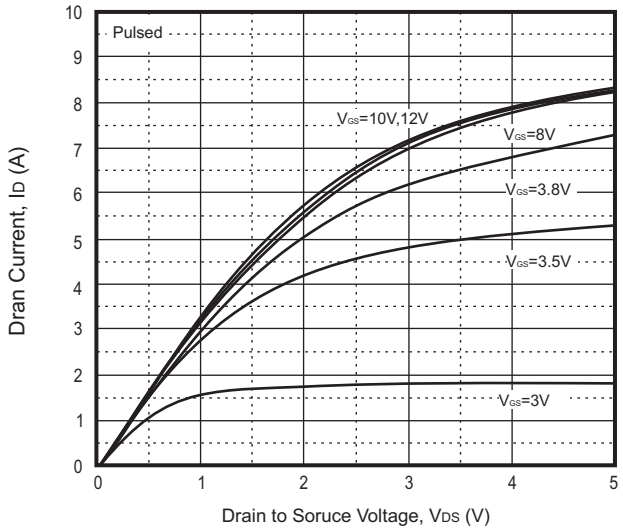


Fig.2 - Transfer Characteristics

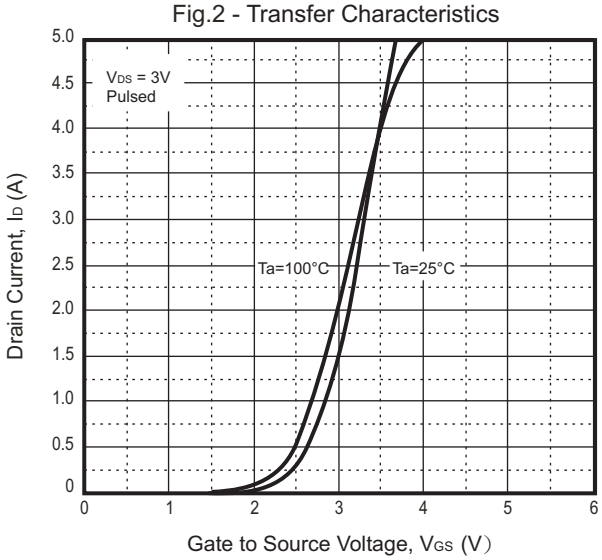


Fig.3 - $R_{DS(ON)}$ — I_D

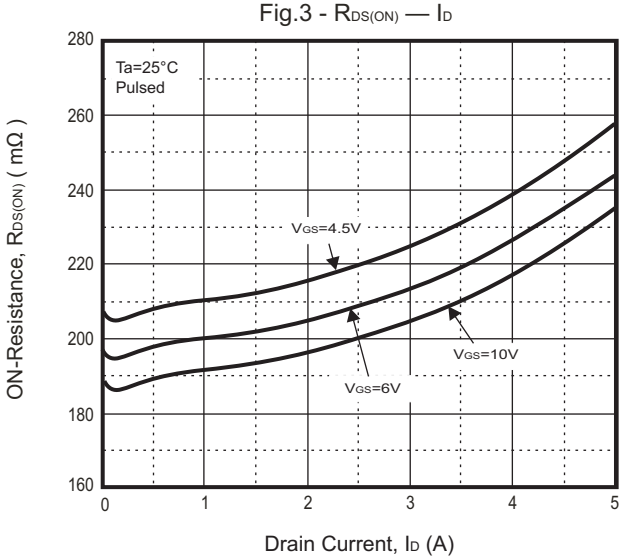


Fig.4 - $R_{DS(ON)}$ — V_{GS}

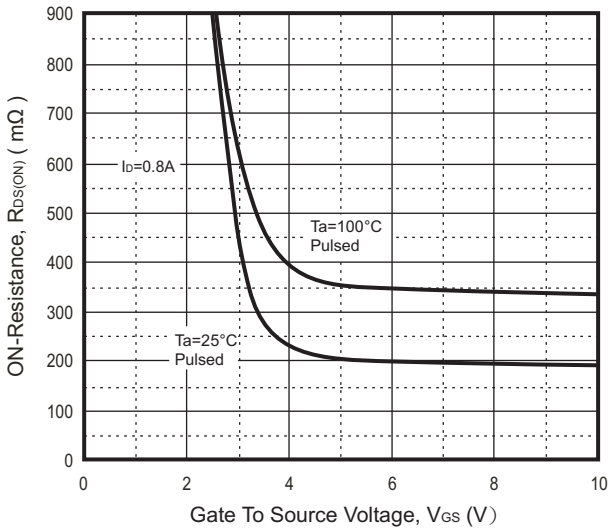


Fig.5 - I_S — V_{SD}

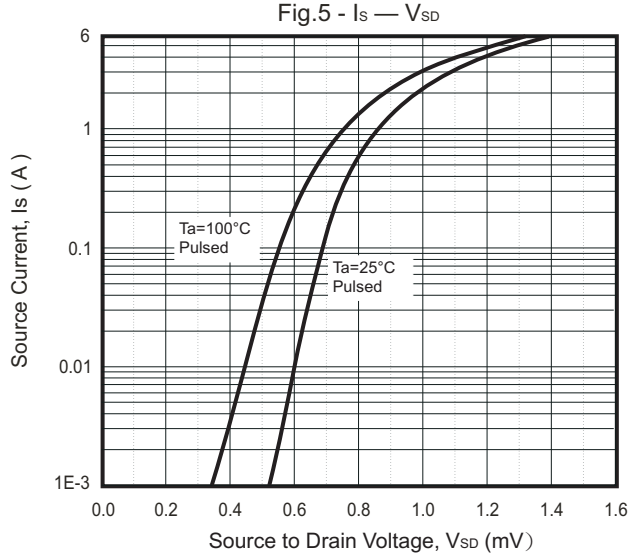
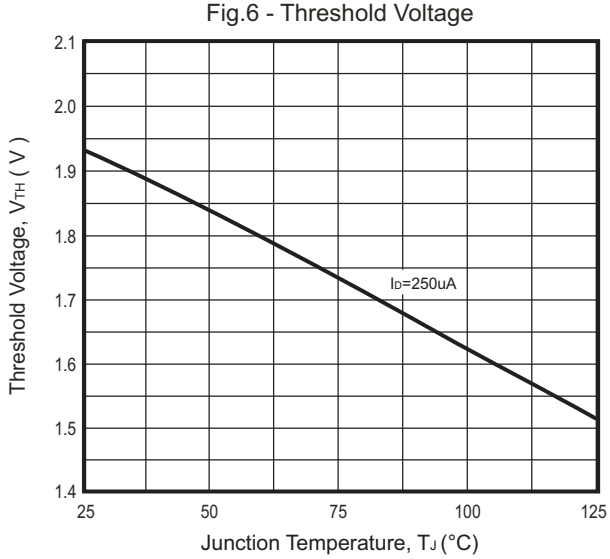


Fig.6 - Threshold Voltage



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