

Product Overview

The NSi814xS devices are small package quad-channel digital isolators. The NSi814xS device is safety certified by UL1577 support 3kVrms insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi814xS is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 150kV/us. The NSi814xS device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi814xS device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use. AEC-Q100 (Grade 1) option is provided for all devices.

Key Features

- Up to 3000VRMS Insulation voltage
- Data rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- AEC-Q100 Grade 1 available for All devices
- High CMTI: 150kV/us
- Chip level ESD: HBM: ±6kV
- High system level EMC performance:
- Enhanced system level ESD, EFT, Surge immunity
- Default output high level or low level option
- Isolation Barrier Life: >60 years
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <15ns
- Operation temperature: -40°C~125°C
- RoHS-compliant packages: SSOP16(150mil)

Safety Regulatory Approvals

- UL recognition: up to 3000VRMS for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A approval
- IEC60950-1 standard
- DIN VDE V 0884-10 (VDE V 0884-10): 2006-12

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Functional Block Diagrams

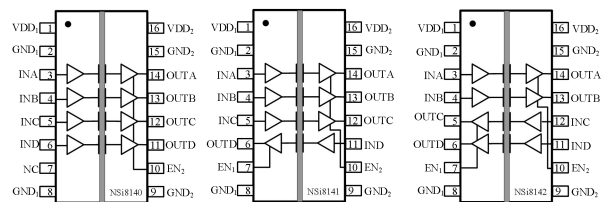


Figure 1. NSi814xS Block Diagram

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1.0 ABSOLUTE MAXIMUM RATINGS

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|------------------------------------|--|------|-----|---------|-------|---|
| Power Supply Voltage | VDD1, VDD2 | -0.5 | | 6.5 | V | |
| Maximum Input Voltage | VINA, VINB, VINC, VIND | -0.4 | | VDD+0.4 | V | |
| Maximum Output Voltage | VOUTA, VOUTB, VOUTC, VOUTD | -0.4 | | VDD+0.4 | V | |
| Maximum Input/Output Pulse Voltage | VINA, VINB, VINC, VIND, VOUTA, VOUTB, VOUTC, VOUTD | -0.8 | | VDD+0.8 | V | Pulse width should be less than 100ns, and the duty cycle should be less than 10% |
| Common-Mode Transients | CMTI | | | ±150 | kV/us | |
| Output current | I _o | -15 | | 15 | mA | |
| Maximum Surge Isolation Voltage | V _{IOSM} | | | 5.3 | kV | |
| Operating Temperature | T _{opr} | -40 | | 125 | °C | |
| Storage Temperature | T _{stg} | -40 | | 150 | °C | |
| Junction temperature | T _j | | | 150 | °C | |
| Electrostatic discharge | HBM | | | ±6000 | V | |
| | CDM | | | ±2000 | V | |

2.0 SPECIFICATIONS

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|---------------------------|---------------------|---------|-----|-----|------|----------------------------------|
| Power on Reset | VDD _{POR} | | 2.2 | | V | POR threshold as during power-up |
| | VDD _{HYS} | | 0.1 | | V | POR threshold Hysteresis |
| Input Threshold | V _{IT} | | 1.6 | | V | Input Threshold at rising edge |
| | V _{IT_HYS} | | 0.4 | | V | Input Threshold Hysteresis |
| High Level Input Voltage | V _{IH} | 2 | | | V | |
| Low Level Input Voltage | V _{IL} | | | 0.8 | V | |
| High Level Output Voltage | V _{OH} | VDD-0.3 | | | V | I _{OH} = -4mA |
| Low Level Output Voltage | V _{OL} | | | 0.3 | V | I _{OL} = 4mA |
| Output Impedance | R _{out} | | 50 | | ohm | |

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| | | | | | | |
|--------------------------------|------------|-----|----|-----|-------|--|
| Input Pull high or low Current | I_{pull} | | 8 | 15 | uA | |
| Start Up Time after POR | trbs | | 40 | | usec | |
| Common Mode Transient Immunity | CMTI | 100 | | 150 | kV/us | |

2.1. RECOMMENDED OPERATING CONDITIONS

| Parameters | Symbol | min | typ | max | unit |
|--------------------------|------------|-----|-----|-----|------|
| Power Supply Voltage | VDD1, VDD2 | 2.5 | | 5.5 | V |
| Operating Temperature | Topr | -40 | | 125 | °C |
| High Level Input Voltage | VIH | 2 | | | V |
| Low Level Input Voltage | VIL | | | 0.8 | V |
| Data rate | DR | | | 150 | Mbps |

2.2. THERMAL CHARACTERISTICS

| Parameters | Symbol | SSOP-16 | Unit |
|--|---------------|---------|-------|
| IC Junction-to-Air Thermal Resistance | θ_{JA} | 100 | ° C/W |
| Junction-to-case(top) thermal resistance | θ_{JB} | 54.4 | ° C/W |
| Junction-to-board thermal resistance | θ_{JC} | 51.9 | ° C/W |

2.3. ELECTRICAL CHARACTERISTICS

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|--------------------------------|---------------------|---------|-----|-----|------|----------------------------------|
| Power on Reset | VDD _{POR} | | 2.2 | | V | POR threshold as during power-up |
| | VDD _{HYS} | | 0.1 | | V | POR threshold Hysteresis |
| Input Threshold | V _{IT} | | 1.6 | | V | Input Threshold at rising edge |
| | V _{IT_HYS} | | 0.4 | | V | Input Threshold Hysteresis |
| High Level Input Voltage | V _{IH} | 2 | | | V | |
| Low Level Input Voltage | V _{IL} | | | 0.8 | V | |
| High Level Output Voltage | V _{OH} | VDD-0.3 | | | V | I _{OH} = -4mA |
| Low Level Output Voltage | V _{OL} | | | 0.3 | V | I _{OL} = 4mA |
| Output Impedance | R _{out} | | 50 | | ohm | |
| Input Pull high or low Current | I _{pull} | | 8 | 15 | uA | |

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| | | | | | | |
|--------------------------------|------|-----|----|-----|-------|--|
| Start Up Time after POR | trbs | | 40 | | usec | |
| Common Mode Transient Immunity | CMTI | 100 | | 150 | kV/us | |

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|----------------|-------------------------|-----|--------|-------|------|---|
| Supply current | NSi8140S | | | | | |
| | I _{DD1} (Q0) | | 0.894 | 1.34 | mA | All Input 0V for NSi8140S0 Or All Input at supply for NSi8140S1 |
| | I _{DD2} (Q0) | | 2.326 | 3.5 | mA | |
| | I _{DD1} (Q1) | | 5.316 | 7.8 | mA | All Input at supply for NSi8140S0 Or All Input 0V for NSi8140S1 |
| | I _{DD2} (Q1) | | 2.432 | 3.65 | mA | |
| | I _{DD1} (1M) | | 3.087 | 4.63 | mA | All Input with 1Mbps, C _L =15pF |
| | I _{DD2} (1M) | | 2.728 | 4.09 | mA | |
| | I _{DD1} (10M) | | 3.182 | 4.77 | mA | All Input with 10Mbps, C _L =15pF |
| | I _{DD2} (10M) | | 5.834 | 8.75 | mA | |
| | I _{DD1} (100M) | | 3.918 | 5.88 | mA | All Input with 100Mbps, C _L =15pF |
| | I _{DD2} (100M) | | 37.06 | 55.6 | mA | |
| | NSi8141S | | | | | |
| | I _{DD1} (Q0) | | 1.244 | 1.87 | mA | All Input 0V for NSi8141S0 Or All Input at supply for NSi8141S1 |
| | I _{DD2} (Q0) | | 2.164 | 3.25 | mA | |
| | I _{DD1} (Q1) | | 4.658 | 7 | mA | All Input at supply for NSi8141S0 Or All Input 0V for NSi8141S1 |
| | I _{DD2} (Q1) | | 3.416 | 5 | mA | |
| | I _{DD1} (1M) | | 3.07 | 4.6 | mA | All Input with 1Mbps, C _L =15pF |
| | I _{DD2} (1M) | | 3.064 | 4.6 | mA | |
| | I _{DD1} (10M) | | 3.82 | 5.7 | mA | All Input with 10Mbps, C _L =15pF |
| | I _{DD2} (10M) | | 5.496 | 8.2 | mA | |
| | I _{DD1} (100M) | | 10.708 | 16.06 | mA | All Input with 100Mbps, C _L = 15pF |
| | I _{DD2} (100M) | | 29.336 | 44 | mA | |
| | NSi8142S | | | | | |
| | I _{DD1} (Q0) | | 1.688 | 2.5 | mA | All Input 0V for NSi8142S0 Or All Input at supply for NSi8142S1 |
| | I _{DD2} (Q0) | | 1.704 | 2.56 | mA | |
| | I _{DD1} (Q1) | | 4.038 | 6.06 | mA | All Input at supply for NSi8142S0 |

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| | | | | | | |
|--|-------------------------|---|--------|------|------|---|
| | I _{DD2} (Q1) | | 4.1 | 6.15 | mA | Or All Input 0V for NSi8142S1 |
| | I _{DD1} (1M) | | 3.06 | 4.6 | mA | All Input with 1Mbps, C _L =15pF |
| | I _{DD2} (1M) | | 3.108 | 4.7 | mA | |
| | I _{DD1} (10M) | | 4.578 | 6.9 | mA | All Input with 10Mbps, C _L =15pF |
| | I _{DD2} (10M) | | 4.694 | 7 | mA | |
| | I _{DD1} (100M) | | 19 | 28.5 | mA | All Input with 100Mbps, C _L = 15pF |
| | I _{DD2} (100M) | | 20.868 | 31 | mA | |
| Data Rate | DR | 0 | | 150 | Mbps | |
| Minimum Pulse Width | PW | | | 5.0 | ns | |
| Propagation Delay | t _{PLH} | 5 | 8.20 | 15 | ns | See Figure 2.9 , C _L = 15pF |
| | t _{PHL} | 5 | 10.56 | 15 | ns | See Figure 2.9 , C _L = 15pF |
| Pulse Width Distortion t _{PHL} - t _{PLH} | PWD | | | 5.0 | ns | See Figure 2.9 , C _L = 15pF |
| Rising Time | t _r | | | 5.0 | ns | See Figure 2.9 , C _L = 15pF |
| Falling Time | t _f | | | 5.0 | ns | See Figure 2.9 , C _L = 15pF |
| Peak Eye Diagram Jitter | t _{JIT} (PK) | | 350 | | ps | |
| Channel-to-Channel Delay Skew | t _{SK} (c2c) | | | 2.5 | ns | |
| Part-to-Part Delay Skew | t _{SK} (p2p) | | | 5.0 | ns | |
| Disable high to Tri-State | t _{PHZ} | | 14.88 | | ns | See Figure 2.10 , C _L = 15pF, R _L =1k |
| Enable to Data high Valid | t _{PZH} | | 10.00 | | ns | See Figure 2.10 , C _L = 15pF, R _L =1k |
| Disable low to Tri-State | t _{PLZ} | | 17.25 | | ns | See Figure 2.10 , C _L = 15pF, R _L =1k |
| Enable to Data high Valid | t _{PZL} | | 10.85 | | ns | See Figure 2.10 , C _L = 15pF, R _L =1k |

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C)

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|-----------------------|-----------------------|------|-------|------|-----------------------|---|
| Supply current | NSi8140S | | | | | |
| | I _{DD1} (Q0) | | 0.832 | 1.25 | mA | All Input 0V for NSi8140S0 Or All Input at supply for NSi8140S1 |
| | I _{DD2} (Q0) | | 2.214 | 3.3 | mA | |
| | I _{DD1} (Q1) | | 5.23 | 7.9 | mA | All Input at supply for NSi8140S0 Or All Input 0V for NSi8140S1 |
| | I _{DD2} (Q1) | | 2.32 | 3.48 | mA | |
| I _{DD1} (1M) | | 3.01 | 4.5 | mA | All Input with 1Mbps, | |

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| | | | | | | |
|------------------------|-------------------------|---|--------|------|------|--|
| | I _{DD2} (1M) | | 2.486 | 3.73 | mA | C _L =15pF |
| | I _{DD1} (10M) | | 3.106 | 4.66 | mA | All Input with 10Mbps, C _L =15pF |
| | I _{DD2} (10M) | | 4.476 | 6.7 | mA | |
| | I _{DD1} (100M) | | 3.826 | 5.74 | mA | All Input with 100Mbps, C _L =15pF |
| | I _{DD2} (100M) | | 25.5 | 38 | mA | |
| NSi8141S | | | | | | |
| | I _{DD1} (Q0) | | 1.165 | 1.75 | mA | All Input 0V for NSi8141S0 Or All Input at supply for NSi8141S1 |
| | I _{DD2} (Q0) | | 2.062 | 3.1 | mA | |
| | I _{DD1} (Q1) | | 4.566 | 6.85 | mA | All Input at supply for NSi8141S0 Or All Input 0V for NSi8141S1 |
| | I _{DD2} (Q1) | | 3.306 | 5 | mA | |
| | I _{DD1} (1M) | | 2.954 | 4.4 | mA | All Input with 1Mbps, C _L =15pF |
| | I _{DD2} (1M) | | 2.862 | 4.3 | mA | |
| | I _{DD1} (10M) | | 3.452 | 5.2 | mA | All Input with 10Mbps, C _L =15pF |
| | I _{DD2} (10M) | | 4.368 | 6.5 | mA | |
| | I _{DD1} (100M) | | 8.084 | 12 | mA | All Input with 100Mbps, C _L = 15pF |
| | I _{DD2} (100M) | | 19.96 | 30 | mA | |
| NSi8142S | | | | | | |
| | I _{DD1} (Q0) | | 1.598 | 2.4 | mA | All Input 0V for NSi8142S0 Or All Input at supply for NSi8142S1 |
| | I _{DD2} (Q0) | | 1.618 | 2.43 | mA | |
| | I _{DD1} (Q1) | | 3.942 | 5.9 | mA | All Input at supply for NSi8142S0 Or All Input 0V for NSi8142S1 |
| | I _{DD2} (Q1) | | 4.004 | 6 | mA | |
| | I _{DD1} (1M) | | 2.901 | 4.3 | mA | All Input with 1Mbps, C _L =15pF |
| | I _{DD2} (1M) | | 2.9452 | 4.4 | mA | |
| | I _{DD1} (10M) | | 3.898 | 5.85 | mA | All Input with 10Mbps, C _L =15pF |
| | I _{DD2} (10M) | | 3.976 | 6 | mA | |
| | I _{DD1} (100M) | | 12.9 | 19 | mA | All Input with 100Mbps, C _L = 15pF |
| | I _{DD2} (100M) | | 14.868 | 22 | mA | |
| Data Rate | DR | 0 | | 150 | Mbps | |
| Minimum Pulse Width | PW | | | 5.0 | ns | |
| Propagation Delay | t _{PLH} | 5 | 9.20 | 15 | ns | See Figure 2.9 , C _L = 15pF |
| | t _{PHL} | 5 | 10.40 | 15 | ns | See Figure 2.9 , C _L = 15pF |
| Pulse Width Distortion | PWD | | | 5.0 | ns | See Figure 2.9 , C _L = 15pF |

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| | | | | | | |
|-------------------------------|---------------|--|-------|-----|----|---|
| $ t_{PHL} - t_{PLH} $ | | | | | | |
| Rising Time | t_r | | | 5.0 | ns | See Figure 2.9 , $C_L = 15\text{pF}$ |
| Falling Time | t_f | | | 5.0 | ns | See Figure 2.9 , $C_L = 15\text{pF}$ |
| Peak Eye Diagram Jitter | $t_{JIT(PK)}$ | | 350 | | ps | |
| Channel-to-Channel Delay Skew | $t_{SK(c2c)}$ | | | 2.5 | ns | |
| Part-to-Part Delay Skew | $t_{SK(p2p)}$ | | | 5.0 | ns | |
| Disable high to Tri-State | t_{PHZ} | | 17.85 | | ns | See Figure 2.10 , $C_L = 15\text{pF}$, $R_L = 1\text{k}$ |
| Enable to Data high Valid | t_{PZH} | | 13.37 | | ns | See Figure 2.10 , $C_L = 15\text{pF}$, $R_L = 1\text{k}$ |
| Disable low to Tri-State | t_{PLZ} | | 20.6 | | ns | See Figure 2.10 , $C_L = 15\text{pF}$, $R_L = 1\text{k}$ |
| Enable to Data high Valid | t_{PZL} | | 13.67 | | ns | See Figure 2.10 , $C_L = 15\text{pF}$, $R_L = 1\text{k}$ |

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25°C)

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|----------------|-----------------|-----|-------|------|------|---|
| Supply current | NSi8140S | | | | | |
| | $I_{DD1(Q0)}$ | | 0.802 | 1.2 | mA | All Input 0V for NSi8140S0 Or All Input at supply for NSi8140S1 |
| | $I_{DD2(Q0)}$ | | 2.161 | 3.24 | mA | |
| | $I_{DD1(Q1)}$ | | 5.17 | 7.8 | mA | All Input at supply for NSi8140S0 Or All Input 0V for NSi8140S1 |
| | $I_{DD2(Q1)}$ | | 2.282 | 3.4 | mA | |
| | $I_{DD1(1M)}$ | | 2.968 | 4.45 | mA | All Input with 1Mbps, $C_L = 15\text{pF}$ |
| | $I_{DD2(1M)}$ | | 2.384 | 3.58 | mA | |
| | $I_{DD1(10M)}$ | | 3.056 | 4.58 | mA | All Input with 10Mbps, $C_L = 15\text{pF}$ |
| | $I_{DD2(10M)}$ | | 3.862 | 5.8 | mA | |
| | $I_{DD1(100M)}$ | | 3.772 | 5.67 | mA | All Input with 100Mbps, $C_L = 15\text{pF}$ |
| | $I_{DD2(100M)}$ | | 19.54 | 29.3 | mA | |
| | NSi8141S | | | | | |
| | $I_{DD1(Q0)}$ | | 1.128 | 1.7 | mA | All Input 0V for NSi8141S0 Or All Input at supply for NSi8141S1 |
| | $I_{DD2(Q0)}$ | | 2.012 | 3 | mA | |
| | $I_{DD1(Q1)}$ | | 4.51 | 6.8 | mA | All Input at supply for NSi8141S0 Or All Input 0V for NSi8141S1 |
| | $I_{DD2(Q1)}$ | | 3.248 | 4.9 | mA | |
| | $I_{DD1(1M)}$ | | 2.894 | 4.3 | mA | All Input with 1Mbps, $C_L = 15\text{pF}$ |
| | $I_{DD2(1M)}$ | | 2.766 | 4.15 | mA | |
| | $I_{DD1(10M)}$ | | 3.272 | 4.9 | mA | All Input with 10Mbps, |

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| | | | | | | |
|---|-----------------|---|--------|-------|------|---|
| | $I_{DD2}(10M)$ | | 3.892 | 5.8 | mA | $C_L=15pF$ |
| | $I_{DD1}(100M)$ | | 6.95 | 10.4 | mA | All Input with 100Mbps, $C_L = 15pF$ |
| | $I_{DD2}(100M)$ | | 15.706 | 23.56 | mA | |
| NSi8142S | | | | | | |
| | $I_{DD1}(Q0)$ | | 1.556 | 2.3 | mA | All Input 0V for NSi8142S0 Or All Input at supply for NSi8142S1 |
| | $I_{DD2}(Q0)$ | | 1.574 | 2.4 | mA | |
| | $I_{DD1}(Q1)$ | | 3.884 | 5.8 | mA | All Input at supply for NSi8142S0 Or All Input 0V for NSi8142S1 |
| | $I_{DD2}(Q1)$ | | 3.942 | 5.9 | mA | |
| | $I_{DD1}(1M)$ | | 2.824 | 4.3 | mA | All Input with 1Mbps, $C_L=15pF$ |
| | $I_{DD2}(1M)$ | | 2.866 | 4.3 | mA | |
| | $I_{DD1}(10M)$ | | 3.574 | 5.36 | mA | All Input with 10Mbps, $C_L=15pF$ |
| | $I_{DD2}(10M)$ | | 3.642 | 5.46 | mA | |
| | $I_{DD1}(100M)$ | | 10.678 | 16 | mA | All Input with 100Mbps, $C_L = 15pF$ |
| | $I_{DD2}(100M)$ | | 11.618 | 17 | mA | |
| Data Rate | DR | 0 | | 150 | Mbps | |
| Minimum Pulse Width | PW | | | 5.0 | ns | |
| Propagation Delay | t_{PLH} | 5 | 10.0 | 15 | ns | See Figure 2.9 , $C_L = 15pF$ |
| | t_{PHL} | 5 | 10.0 | 15 | ns | See Figure 2.9 , $C_L = 15pF$ |
| Pulse Width Distortion $ t_{PHL} - t_{PLH} $ | PWD | | | 5.0 | ns | See Figure 2.9 , $C_L = 15pF$ |
| Rising Time | t_r | | | 5.0 | ns | See Figure 2.9 , $C_L = 15pF$ |
| Falling Time | t_f | | | 5.0 | ns | See Figure 2.9 , $C_L = 15pF$ |
| Peak Eye Diagram Jitter | $t_{JIT}(PK)$ | | 350 | | ps | |
| Channel-to-Channel Delay Skew | $t_{SK}(c2c)$ | | | 2.5 | ns | |
| Part-to-Part Delay Skew | $t_{SK}(p2p)$ | | | 5.0 | ns | |
| Disable high to Tri-State | t_{PHZ} | | 20.6 | | ns | See Figure 2.10 , $C_L = 15pF$, $R_L=1k$ |
| Enable to Data high Valid | t_{PZH} | | 18.12 | | ns | See Figure 2.10 , $C_L = 15pF$, $R_L=1k$ |
| Disable low to Tri-State | t_{PLZ} | | 21.85 | | ns | See Figure 2.10 , $C_L = 15pF$, $R_L=1k$ |
| Enable to Data high Valid | t_{PZL} | | 20.02 | | ns | See Figure 2.10 , $C_L = 15pF$, $R_L=1k$ |

2.4. TYPICAL PERFORMANCE CHARACTERISTICS

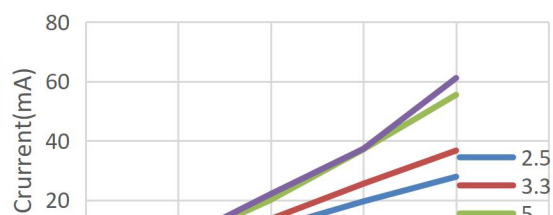
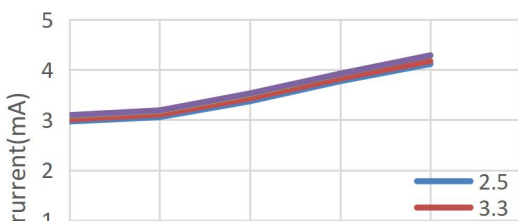


Figure 2.1 NSi8140S VDD1 Supply Current vs Data Rate

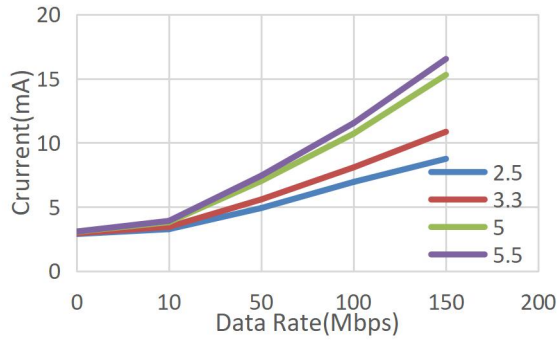


Figure 2.2 NSi8140S VDD2 Supply Current vs Data Rate

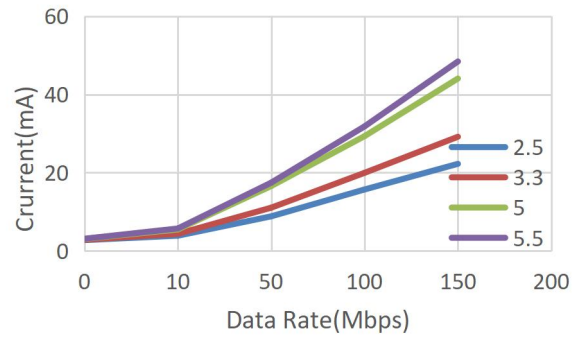


Figure 2.3 NSi8141S VDD1 Supply Current vs Data Rate

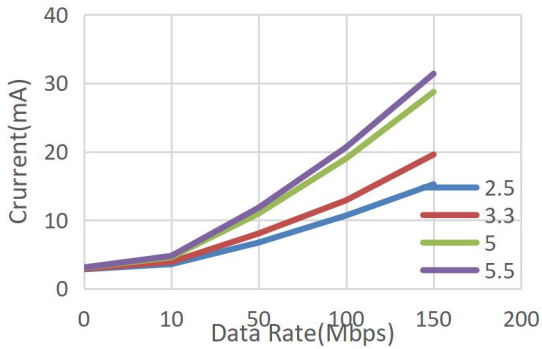


Figure 2.4 NSi8141S VDD2 Supply Current vs Data Rate

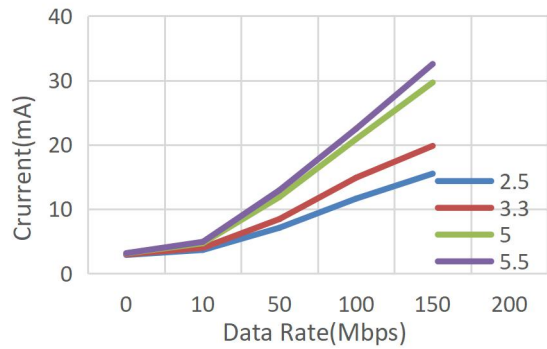


Figure 2.5 NSi8142S VDD1 Supply Current vs Data Rate

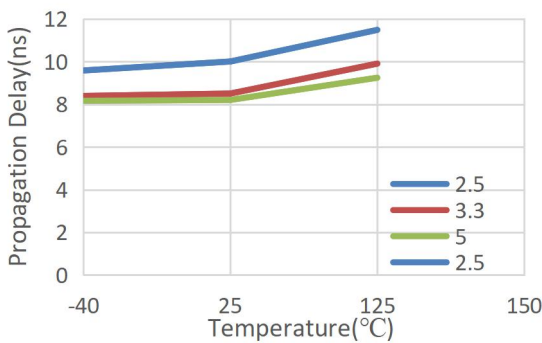


Figure 2.6 NSi8142S VDD2 Supply Current vs Data Rate

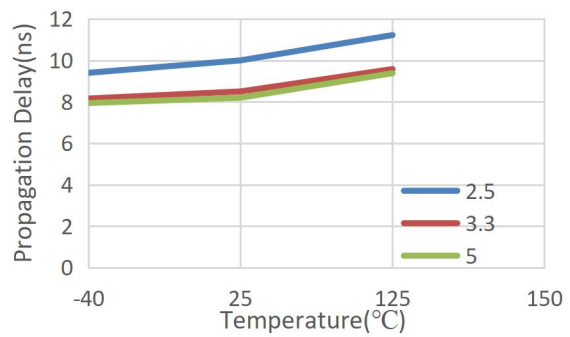


Figure 2.7 Rising Edge Propagation Delay Vs Temp

Figure 2.8 Falling Edge Propagation Delay Vs Temp

2.5. PARAMETER MEASUREMENT INFORMATION

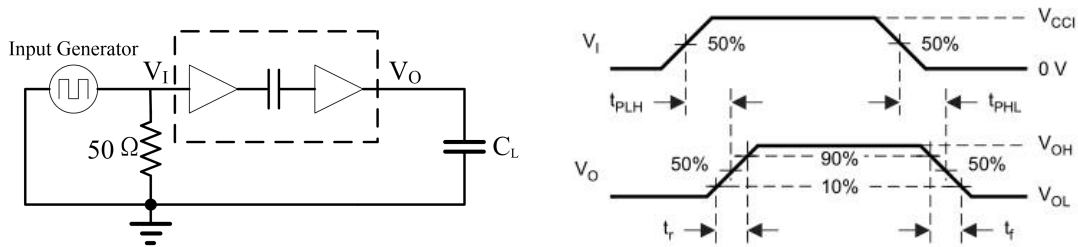


Figure 2.9 Switching Characteristics Test Circuit and Waveform

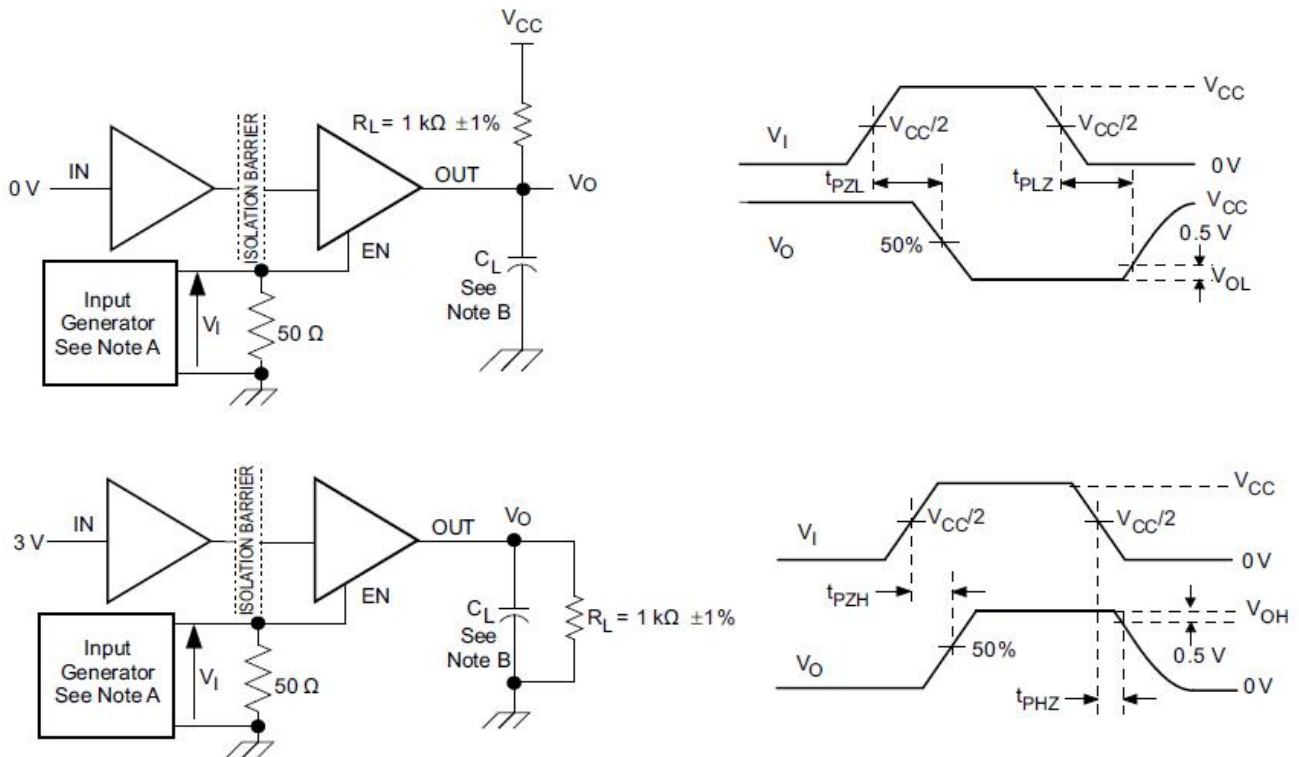


Figure 2.10 Enable/Disable Propagation Delay Time Test Circuit and Waveform

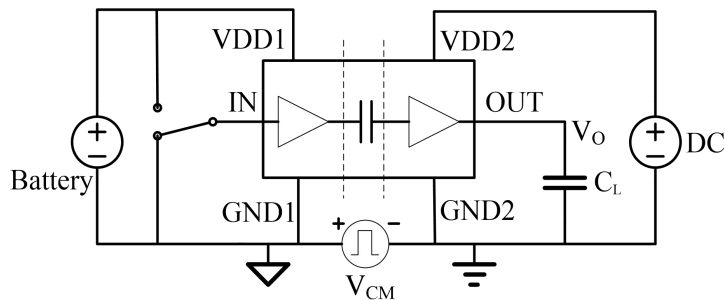


Figure 2.11 Common-Mode Transient Immunity Test Circuit

Note A :The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, tr ≤ 3 ns, tf ≤ 3 ns, Zo = 50 Ω . At the input, a 50-Ω resistor is required to terminate the Input Generator signal. It is not needed in actual application.

NoteB : CL = 15 pF and includes instrumentation and fixture capacitance within ±20%.

3.0 HIGH VOLTAGE FEATURE DESCRIPTION

3.1. INSULATION AND SAFETY RELATED SPECIFICATIONS

| Parameters | Symbol | Value | Unit | Comments |
|---|--------|---------|------|---|
| | | SSOP-16 | | |
| Minimum External Air Gap (Clearance) | L(I01) | 3.9 | mm | Shortest terminal-to-terminal distance through air |
| Minimum External Tracking (Creepage) | L(I02) | 3.9 | mm | Shortest terminal-to-terminal distance across the package surface |
| Minimum internal gap | DTI | 19 | um | Distance through insulation |
| Tracking Resistance(Comparative Tracking Index) | CTI | >400 | V | DIN EN 60112 (VDE 0303-11); IEC 60112 |
| Material Group | | II | | |

3.2. DIN VDE V 0884-11 (VDE V 0884-11) :2017-01 INSULATION CHARACTERISTICS

| Description | Test Condition | Symbol | SSOP-16 | Unit |
|--|--|-------------|---------------|-----------|
| Installation Classification per DIN VDE 0110 | | | | |
| For Rated Mains Voltage $\leq 150V_{rms}$ | | | I to IV | |
| For Rated Mains Voltage $\leq 300V_{rms}$ | | | I to III | |
| For Rated Mains Voltage $\leq 400V_{rms}$ | | | I to III | |
| Climatic Classification | | | 10/105/2 1 | |
| Pollution Degree per DIN VDE 0110, Table 1 | | | 2 | |
| Maximum repetitive peak isolation voltage | | V_{IORM} | 565 | Vpeak |
| Maximum working isolation voltage | AC voltage | V_{IOWM} | 400 | V_{RMS} |
| | DC voltage | | 565 | Vpeak |
| Input to Output Test Voltage, Method B1 | $V_{IORM} \times 1.5 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC | $V_{pd(m)}$ | 847 | Vpeak |

NSi8140S/NSi8141S/NSi8142S

| | | | | |
|---|--|-------------|---------|----------|
| Input to Output Test Voltage, Method A | | | | |
| After Environmental Tests Subgroup 1 | $V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC | $V_{pd(m)}$ | 678 | Vpeak |
| After Input and /or Safety Test Subgroup 2 and Subgroup 3 | $V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC | $V_{pd(m)}$ | 678 | Vpeak |
| Maximum transient isolation voltage | $t = 60$ sec | VIOTM | 5300 | Vpeak |
| Maximum Surge Isolation Voltage | Test method per IEC60065,1.2/50us waveform, $V_{TEST} = V_{IOSM} \times 1.3$ | VIOSM | 5384 | Vpeak |
| Isolation resistance | $V_{IO} = 500V$ | RIO | $>10^9$ | Ω |
| Isolation capacitance | $f = 1MHz$ | CIO | 0.6 | pF |
| Input capacitance | | CI | 2 | pF |
| Total Power Dissipation at 25°C | | Ps | | W |
| Safety input, output, or supply current | $\theta_{JA} = 140$ °C/W, $V_I = 5.5$ V, $T_J = 150$ °C, $T_A = 25$ °C | Is | 160 | mA |
| Case Temperature | | Ts | 150 | °C |

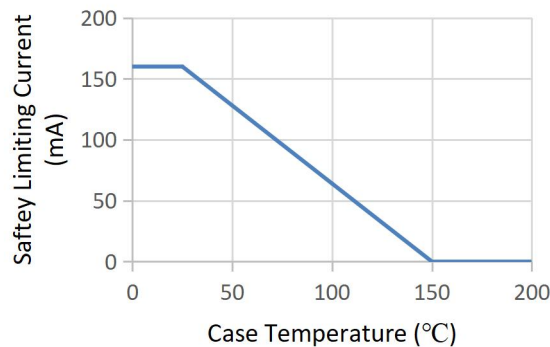


Figure 3.1 NSi8140S/NSi8141S /NSi8142S Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

3.3. REGULATORY INFORMATION

The NSi8140S/NSi8141S /NSi8142S are approved or pending approval by the organizations listed in table.

| | CUL | VDE | CQC |
|---|---|---|--|
| UL 1577 Component Recognition Program ¹ | Approved under CSA Component Acceptance Notice 5A | DIN VDE V 0884-11(VDE V 0884-11):2017-01 ² | Certified by CQC11-471543-2012 GB4943.1-2011 |
| Single Protection, 3000V _{rms} Isolation voltage | Single Protection, 3000V _{rms} Isolation voltage | Basic Insulation 565Vpeak, $V_{IOSM} = 5384V_{peak}$ | Basic insulation at 400V _{rms} (565Vpeak) |

NSi8140S/NSi8141S/NSi8142S

| | | | |
|----------------|----------------|--------------------------|----------------|
| File (E500602) | File (E500602) | File (5024579-4880-0001) | File (pending) |
|----------------|----------------|--------------------------|----------------|

¹ In accordance with UL 1577, each NSi8140S/NSi8141S/NSi8142S is proof tested by applying an insulation test voltage $\geq 3600 V_{rms}$ for 1 sec.

² In accordance with DIN VDE V 0884-11, each NSi8140S/NSi8141S/NSi8142S is proof tested by applying an insulation test voltage $\geq 847 V$ peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN VDE V 0884-11 approval.

4.0 FUNCTION DESCRIPTION

The NSi814xS is a Quad-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSi814xS devices are high reliability quad-channel digital isolator with AEC-Q100 qualified. The NSi814xS device is safety certified by UL1577 support several insulation withstand voltages ($3.75kV_{rms}$, $5kV_{rms}$), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi814xS is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 150kV/us. The NSi814xS device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi814xS device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSi814xS has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 4.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A within 1us after powering up.

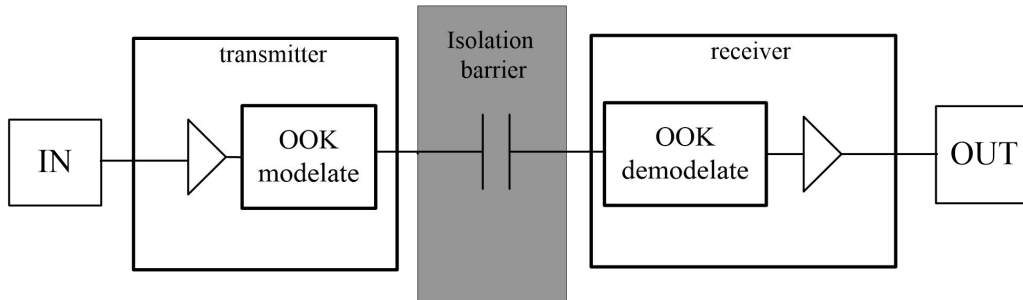


Figure 4.1 Simplified Channel Diagram

Table 4.1 Output status vs. power status

| Input | EN _x | VDD1 status | VDD2 status | Output | Comment |
|-------|-----------------|-------------|-------------|--------|---|
| H | H or NC | Ready | Ready | H | Normal operation. |
| L | H or NC | Ready | Ready | L | |
| X | L | Ready | Ready | Z | Output Disabled, the output is high impedance |
| X | H or NC | Unready | Ready | L H | The output follows the same status with the input within 60us after input side VDD1 is powered on. |
| X | L | Unready | Ready | Z | Output Disabled, the output is high impedance |
| X | X | Ready | Unready | X | The output follows the same status with the input within 60us after output side VDD2 is powered on. |

5.0 APPLICATION NOTE

5.1. PCB LAYOUT

The NSi814xS requires a 0.1 μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 5.1 show the recommended schematic diagram , Figure 5.2 to Figure 5.3 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω , $\pm 40\%$. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

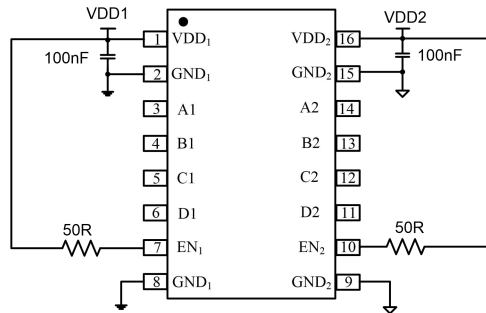


Figure5.1 Recommended schematic diagram

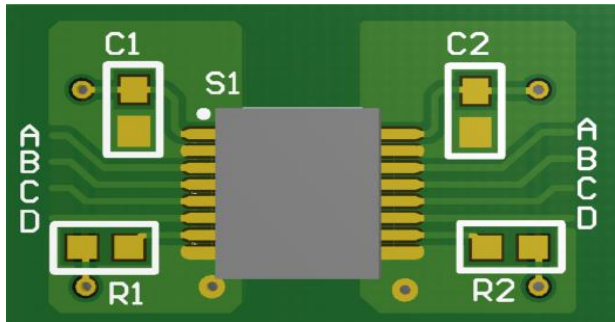


Figure5.2 Recommended PCB Layout — Top Layer

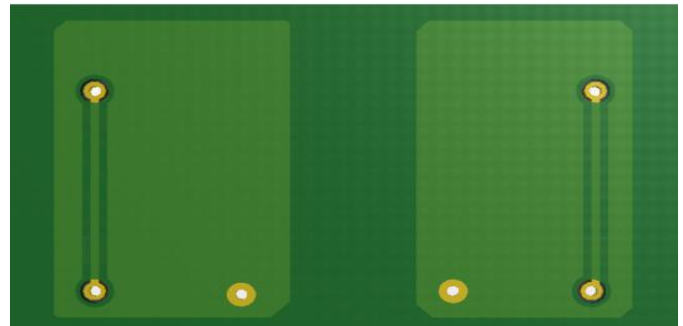


Figure5.3 Recommended PCB Layout — Bottom Layer

5.2. HIGH SPEED PERFORMANCE

Figure 5.4 shows the eye diagram of NSi814xS at 200Mbps data rate output. The result shows a typical measurement on the NSi814xS with 350ps p-p jitter.

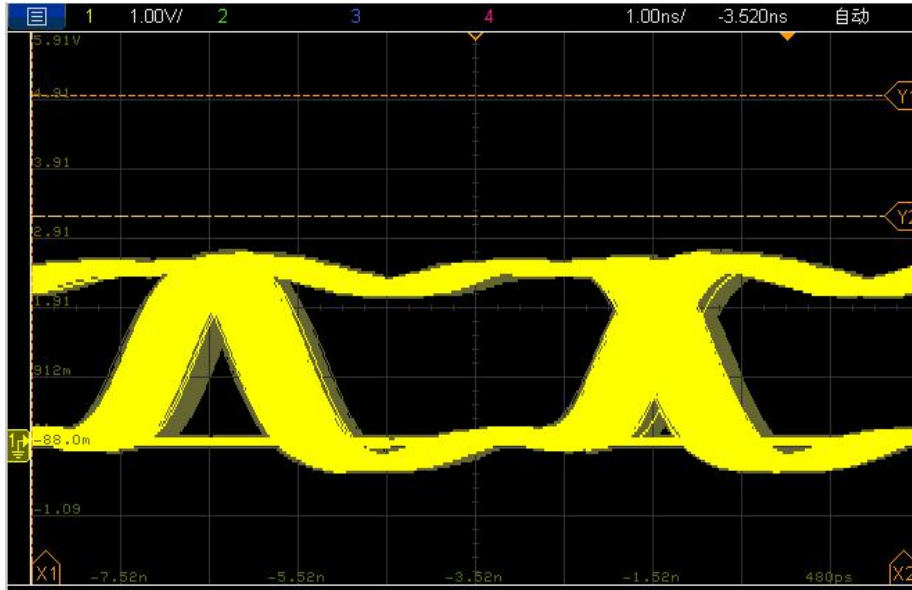


Figure5.4 NSi814xS Eye Diagram

5.3. TYPICAL SUPPLY CURRENT EQUATIONS

The typical supply current of NSi814xS can be calculated using below equations. I_{DD1} and I_{DD2} are typical supply currents measured in mA, f is data rate measured in Mbps, C_L is the capacitive load measured in pF

NSi8140S:

$$I_{DD1} = 0.19 * a1 + 1.45 * b1 + 0.82 * c1.$$

$$I_{DD2} = 1.36 + VDD1 * f * C_L * c1 * 10^{-9}$$

When $a1$ is the channel number of low input at side 1, $b1$ is the channel number of high input at side 1, $c1$ is the channel number of switch signal input at side 1.

NSi8141S:

$$I_{DD1} = 0.87 + 1.26 * b1 + 0.63 * c1 + VDD1 * f * C_L * c2 * 10^{-9}$$

$$I_{DD2} = 0.87 + 1.26 * b2 + 0.63 * c2 + VDD1 * f * C_L * c1 * 10^{-9}$$

When $b1$ is the channel number of high input at side 1, $c1$ is the channel number of switch signal input at side 1, $b2$ is the channel number of high input at side 2, $c2$ is the channel number of switch signal input at side 2.

NSi8142S:

$$I_{DD1} = 0.87 + 1.26 * b1 + 0.63 * c1 + VDD1 * f * C_L * c2 * 10^{-9}$$

$$I_{DD2} = 0.87 + 1.26 * b2 + 0.63 * c2 + VDD1 * f * C_L * c1 * 10^{-9}$$

When $b1$ is the channel number of high input at side 1, $c1$ is the channel number of switch signal input at side 1, $b2$ is the channel number of high input at side 2, $c2$ is the channel number of switch signal input at side 2.

6.0 PACKAGE INFORMATION

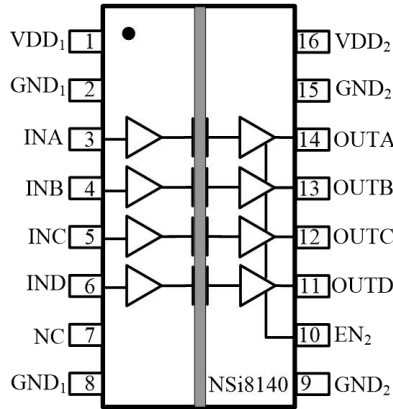


Figure 6.1 NSi8140S Package

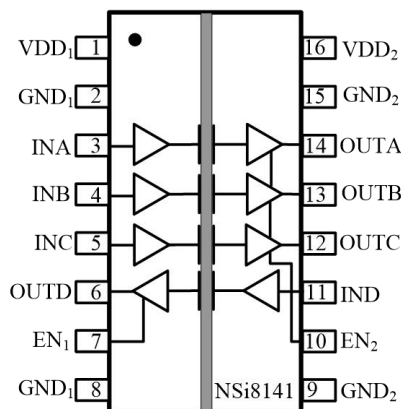


Figure 6.2 NSi8141S Package

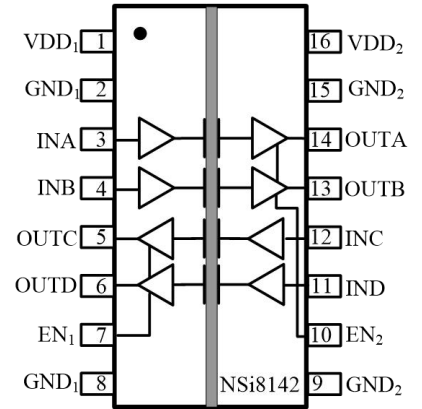


Figure 6.3 NSi8142S Package

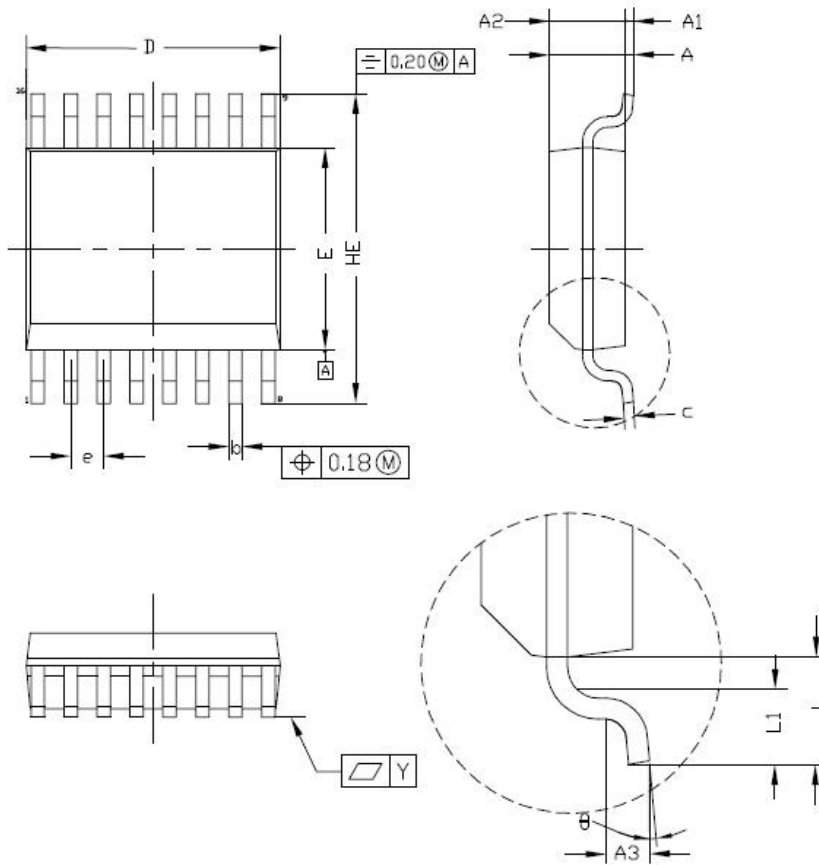


Figure 6.4 SSOP16 Package Shape and Dimension in millimeters (inches)

* CONTROLLING DIMENSION : MM

| SYMBOL | MILLIMETER | | | INCH | | |
|--------|------------|------|------|-----------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | --- | --- | 1.73 | --- | --- | 0.068 |
| A1 | 0.10 | --- | 0.25 | 0.004 | --- | 0.010 |
| A2 | 1.40 | --- | 1.55 | 0.055 | --- | 0.061 |
| b | 0.20 | --- | 0.31 | 0.008 | --- | 0.012 |
| c | 0.18 | --- | 0.25 | 0.007 | --- | 0.010 |
| D | 4.80 | --- | 5.00 | 0.189 | --- | 0.197 |
| E | 3.80 | --- | 4.00 | 0.150 | --- | 0.157 |
| HE | 5.80 | --- | 6.20 | 0.228 | --- | 0.244 |
| e | 0.635 bsc | | | 0.025 bsc | | |
| L | 1.00 bsc | | | 0.039 bsc | | |
| L1 | 0.41 | --- | 0.89 | 0.016 | --- | 0.035 |
| Y | --- | 0.09 | --- | --- | 0.004 | --- |
| A3 | --- | 0.25 | --- | --- | 0.010 | --- |
| theta | 0° | --- | 8° | 0° | --- | 8° |

Table6.1 NSi8140S/ NSi8141S/ NSi8142S Pin Configuration and Description

| NSi8140S | NSi8141S | NSi8142S | SYMBOL | FUNCTION |
|----------|----------|----------|--------|----------|
|----------|----------|----------|--------|----------|

NSi8140S/NSi8141S/NSi8142S

| PIN NO. | PIN NO. | PIN NO. | | |
|---------|---------|---------|---------------------|--|
| 1 | 1 | 1 | VDD ₁ | Power Supply for Isolator Side 1 |
| 2 | 2 | 2 | GND ₁ | Ground 1, the ground reference for Isolator Side 1 |
| 3 | 3 | 3 | INA | Logic Input A |
| 4 | 4 | 4 | INB | Logic Input B |
| 5 | 5 | 12 | INC | Logic Input C |
| 6 | 11 | 11 | IND | Logic Input D |
| 7 | 7 | 7 | NC/ EN ₁ | No Connection. or Output Enable 1. Active high logic input. When EN ₁ is high or NC, the output of Side 1 are enabled. When EN ₁ is low, the output of Side 1 are disabled to high impedance state. |
| 8 | 8 | 8 | GND ₁ | Ground 1, the ground reference for Isolator Side 1 |
| 9 | 9 | 9 | GND ₂ | Ground 2, the ground reference for Isolator Side 2 |
| 10 | 10 | 10 | EN ₂ | Output Enable 2. Active high logic input. When EN ₂ is high or NC, the output of Side 2 are enabled. When EN ₂ is low, the output of Side 2 are disabled to high impedance state. |
| 11 | 6 | 6 | OUTD | Logic Output D |
| 12 | 12 | 5 | OUTC | Logic Output C |
| 13 | 13 | 13 | OUTB | Logic Output B |
| 14 | 14 | 14 | OUTA | Logic Output A |
| 15 | 15 | 15 | GND ₂ | Ground 2, the ground reference for Isolator Side 2 |
| 16 | 16 | 16 | VDD ₂ | Power Supply for Isolator Side 2 |

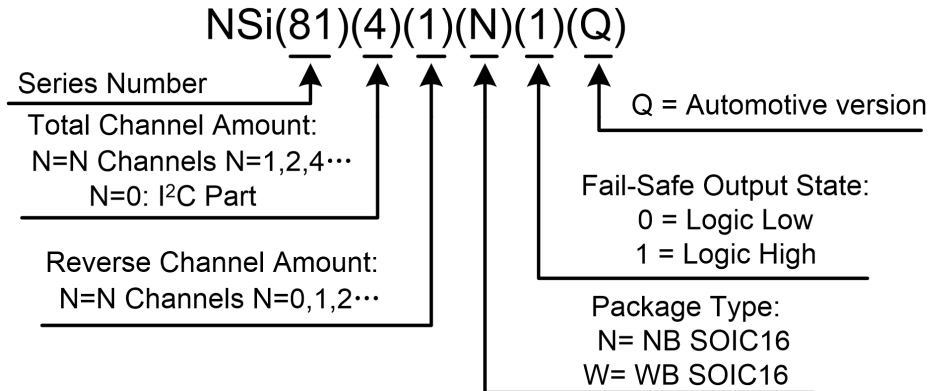
7.0 ORDER INFORMATION

| Part No. | Isolation Rating(kV) | Number of side 1 inputs | Number of side 2 inputs | Max Data Rate (Mbps) | Default Output State | MSL level | Temperature | Automotive | Package |
|--|----------------------|-------------------------|-------------------------|----------------------|----------------------|-----------|--------------|------------|---------|
| NSi8140S0 | 3 | 4 | 0 | 150 | Low | 1 | -40 to 125°C | NO | SSOP-16 |
| NSi8140S1 | 3 | 4 | 0 | 150 | High | 1 | -40 to 125°C | NO | SSOP-16 |
| NSi8141S0 | 3 | 3 | 1 | 150 | Low | 1 | -40 to 125°C | NO | SSOP-16 |
| NSi8141S1 | 3 | 3 | 1 | 150 | High | 1 | -40 to 125°C | NO | SSOP-16 |
| NSi8142S0 | 3 | 2 | 2 | 150 | Low | 1 | -40 to 125°C | NO | SSOP-16 |
| NSi8142S1 | 3 | 2 | 2 | 150 | High | 1 | -40 to 125°C | NO | SSOP-16 |
| NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures. | | | | | | | | | |

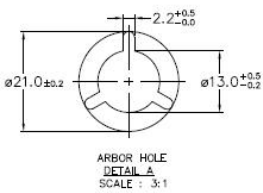
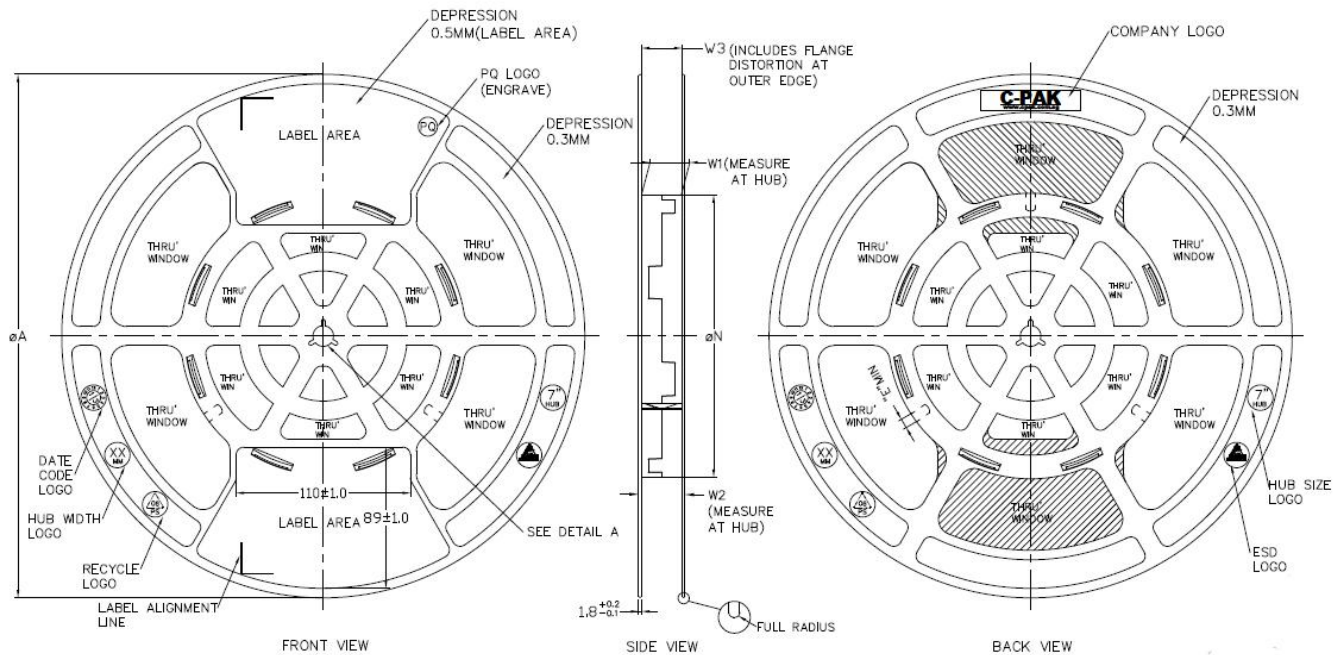
NSi8140S/NSi8141S/NSi8142S

All devices are AEC-Q100 qualified.

Part Number Rule:



8.0 TAPE AND REEL INFORMATION



| PRODUCT SPECIFICATION | | | | | | |
|-----------------------|---------|---------|----------------------|----------|--|---------|
| TAPE WIDTH | øA ±2.0 | øN ±2.0 | W1 | W2 (MAX) | W3 | E (MIN) |
| 08MM | 330 | 178 | 8.4 ^{+0.3} | 14.4 | | 5.5 |
| 12MM | 330 | 178 | 12.4 ^{+0.3} | 18.4 | SHALL ACCOMMODATE TAPE WITH HUB DISTORTION | 5.5 |
| 16MM | 330 | 178 | 16.4 ^{+0.3} | 22.4 | | 5.5 |
| 24MM | 330 | 178 | 24.4 ^{+0.3} | 30.4 | | 5.5 |
| 32MM | 330 | 178 | 32.4 ^{+0.3} | 38.4 | | 5.5 |

| SURFACE RESISTIVITY | | | |
|---------------------|---|----------------------|------------|
| LEGEND | SR RANGE | TYPE | COLOUR |
| A | BELOW 10 ⁹ | ANTISTATIC | ALL TYPES |
| B | 10 ⁹ TO 10 ¹⁰ | STATIC DISSIPATIVE | BLACK ONLY |
| C | 10 ⁹ & BELOW 10 ⁸ | CONDUCTIVE (GENERIC) | BLACK ONLY |
| E | 10 ⁹ TO 10 ¹⁰ | ANTISTATIC (COATED) | ALL TYPES |

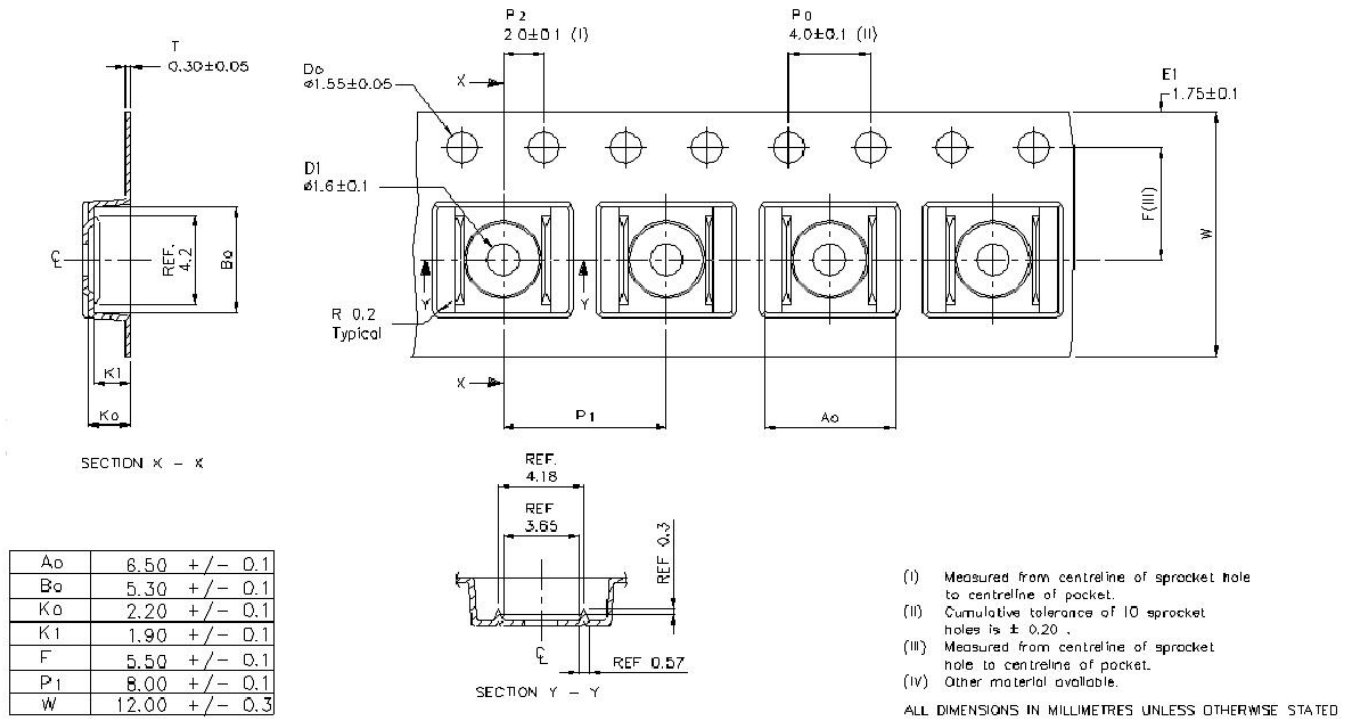


Figure 8.1 Tape and Reel Information of SSOP16

9.0 REVISION HISTORY

| Revision | Description | Date |
|----------|--|-----------|
| 1.0 | Initial version | 2019/7/15 |
| 1.1 | Added RecommEnded Operating Conditions AND Thermal Information | 2020/6/10 |