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RTL8363NB-VB-CG

LAYER 2 MANAGED 2+1-PORT 10/100/1000M SWITCH CONTROLLER

DRAFT DATASHEET

(CONFIDENTIAL: Development Partners Only)

Rev. 0.4
21 February 2017
Track ID: JATR-xxxx-xx

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek RTL8363NB-VB IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.1	2016/07/05	First Draft Version.
0.2	2016/07/19	
0.3	2016/09/02	Update Table 26.
0.4	2017/02/21	Update Table 12. Update Table 21. Update Table 27.

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1. General Description

The RTL8363NB-VB-CG is a QFN76, high-performance 2+1-port 10/100/1000M Ethernet switch featuring low-power integrated dual-port 10/100/1000M PHYs that support 1000Base-T, 100Base-TX, and 10Base-T.

For specific applications, the RTL8363NB-VB supports extra interface that can be configured as RGMII/MII interfaces. The RTL8363NB-VB integrates all the functions of a high-speed switch system; including SRAM for packet buffering, non-blocking switch fabric, and internal register management into a single CMOS device. Only a 25MHz crystal is required; an optional EEPROM is offered for internal register configuration.

The embedded packet storage SRAM in the RTL8363NB-VB features superior memory management technology to efficiently utilize memory space. The RTL8363NB-VB integrates a 2048-entry look-up table with a 4-way XOR Hashing algorithm for address searching and learning. The table provides read/write access from the Slave I^2C-like serial Interface, or Slave Media Independent Interface Management (MIIM) Interface. Each of the entries can be configured as a static entry. Normal entry aging time is between 200 and 400 seconds. Eight Filtering Databases are used to provide Independent VLAN Learning and Shared VLAN Learning (IVL/SVL) functions.

The Extension GMAC1 of the RTL8363NB-VB implements an RGMII/MII interface. This interface could be connected to an external PHY, MAC, CPU, or RISC for specific applications. In router applications, the RTL8363NB-VB supports Port VID (PVID) for each port to insert a PVID in the VLAN tag on egress. When using this function, VID information carried in the VLAN tag will be changed to PVID.

Note: The RTL8363NB-VB Extra Interface GMAC1 supports:

Reduced Gigabit Media Independent Interface (RGMII) (3.3V/2.5V/1.8V mode)
Media Independent Interface (MII)
Turbo Media Independent Interface (TMII)
Reduced Media Independent Interface (RMII)

The RTL8363NB-VB supports standard 802.3x flow control frames for full duplex, and optional backpressure for half duplex. It determines when to invoke the flow control mechanism by checking the availability of system resources, including the packet buffers and transmitting queues. The RTL8363NB-VB supports broadcast/multicast output dropping, and will forward broadcast/multicast packets to non-blocked ports only. For IP multicast applications, the RTL8363NB-VB supports trapping IPv4 IGMPv1/v2/v3 and IPv6 MLDv1/v2 to external CPU.

In order to support flexible traffic classification, the RTL8363NB-VB supports 48-entry ACL rule check and multiple actions options. Each port can optionally enable or disable the ACL rule check function. The ACL rule key can be based on packet physical port, Layer2, Layer3, and Layer4 information. When an ACL rule matches, the action taken is configurable to Drop/Permit/Redirect/Mirror, change priority value in 802.1q/Q tag, force output tag format and rate policing. The rate policing mechanism supports from 8Kbps to 1Gbps (in 8Kbps steps).

In Bridge operation the RTL8363NB-VB supports 16 sets of port configurations: disable, block, learning, and forwarding for Spanning Tree Protocol and Multiple Spanning Tree Protocol. To meet security and

management application requirements, the RTL8363NB-VB supports IEEE 802.1x Port-based/MAC-based Access Control. A 1-set Port Mirroring function is configured to mirror traffic (RX, TX, or both) appearing on one of the switch's ports. Support is provided on each port for multiple RFC MIB Counters, for easy debug and diagnostics.

To improve real-time and multimedia networking applications, the RTL8363NB-VB supports eight priority assignments for each received packet. These are based on (1) Port-based priority; (2) 802.1p/Q VLAN tag priority; (3) DSCP field in IPv4/IPv6 header; and (4) ACL-assigned priority. Each output port supports a weighted ratio of eight priority queues to fit bandwidth requirements in different applications. The input bandwidth control function helps limit per-port traffic utilization. There is one leaky bucket for average packet rate control for each queue of all ports. Queue scheduling algorithm can use Strict Priority (SP) or Weighted Fair Queue (WFQ) or Weighted Round Robin (WRR) or mixed.

The RTL8363NB-VB provides a 4K-entry VLAN table for 802.1Q port-based, tag-based, and protocol-based VLAN operation to separate logical connectivity from physical connectivity. The RTL8363NB-VB supports four Protocol-based VLAN configurations that can optionally select EtherType, LLC, and RFC1042 as the search key. Each port may be set to any topology via EEPROM upon reset, or Slave I^2C-like serial Interface, or Slave Media Independent Interface Management (MIIM) Interface after reset.

In router applications, the router may want to know the input port of the incoming packet. The RTL8363NB-VB supports an option to insert a VLAN tag with VID=Port VID (PVID) on each egress port. The RTL8363NB-VB also provides an option to admit VLAN tagged packets with a specific PVID only. If this function is enabled, the RTL8363NB-VB will drop all non-tagged packets and packets with an incorrect PVID.

2. Features

- Single-chip 2+1-port 10/100/1000M non-blocking switch architecture
- Embedded 2-port 10/100/1000Base-T PHY
- Each port supports full duplex 10/100/1000M connectivity (half duplex only supported in 10/100M mode)
- Extra Interface (Extension GMAC1) Supports
  - Media Independent Interface (MII)
  - Reduced 10/100/1000M Media Independent Interface (RGMII)
  - Turbo Media Independent Interface (TMII)
  - Reduced Media Independent Interface (RMII)
- Full-duplex and half-duplex operation with IEEE 802.3x flow control and backpressure
- Supports 9216-byte jumbo packet length forwarding at wire speed
- Supports Realtek Cable Test (RTCT) function
- Supports 48-entry ACL Rules
  - Search keys support physical port, Layer2, Layer3, and Layer4 information
  - Actions support mirror, redirect, dropping, priority adjustment, traffic policing, CVLAN decision, and SVLAN assignment
  - Supports 5 types of user defined ACL rule format for 48 ACL rules
  - Optional per-port enable/disable of ACL function
  - Optional setting of per-port action to take when ACL mismatch
- Supports IEEE 802.1Q VLAN
  - Supports 4096 VLANs and 32 Extra Enhanced VLANs
  - Supports Un-tag definition in each VLAN
  - Supports VLAN policing and VLAN forwarding decision
  - Supports Port-based, Tag-based, and Protocol-based VLAN
  - Up to 4 Protocol-based VLAN entries
  - Supports per-port and per-VLAN egress VLAN tagging and un-tagging
- Supports IVL, SVL, and IVL/SVL
  - Supports 2048-entry MAC address table with 4-way hash algorithm, and 64-entry CAM
  - Up to 2048 L2/L3 Filtering Database
  - Per-port MAC learning limitation
  - System base MAC learning limitation
- Supports Spanning Tree port behavior configuration
  - IEEE 802.1w Rapid Spanning Tree
  - IEEE 802.1s Multiple Spanning Tree with up to 16 Spanning Tree instances
- Supports IEEE 802.1x Access Control Protocol
  - Port-Based Access Control
  - MAC-Based Access Control

- Supports Auto protection from Denial-of-Service attacks
- Support trap IGMP/MLD packets to external CPU
- Supports Quality of Service (QoS)
  - Supports per port Input Bandwidth Control
  - Traffic classification based on IEEE 802.1p/Q priority definition, physical Port, IP DSCP field, ACL definition, VLAN based priority, MAC based priority, and SVLAN based priority
  - Eight Priority Queues per port
  - Per queue flow control
  - Min-Max Scheduling
  - Strict Priority and Weighted Fair Queue (WFQ), Weighted Round Robin (WRR) packet scheduling
  - One leaky bucket to constrain the average packet rate of each queue
- Supports rate limiting (12 shared meters, with 8kpbs granulation)
- Supports RFC MIB Counter
  - MIB-II (RFC 1213)
  - Ethernet-Like MIB (RFC 3635)
  - Interface Group MIB (RFC 2863)
  - RMON (RFC 2819)
  - Bridge MIB (RFC 1493)
  - Bridge MIB Extension (RFC 2674)
- Supports Stacking VLAN and Port Isolation with 8 Enhanced Filtering Databases
- Supports IEEE 802.1ad Stacking VLAN
  - Supports 64 SVLANs
  - Supports MAC-based 1:N VLAN
- Supports Port Mirror function for one monitor port for multiple mirroring ports
- Security Filtering
  - Disable learning for each port
  - Disable learning-table aging for each port
  - Drop unknown DA for each port
- Broadcast/Multicast/Unknown DA storm control protects system from attack by hackers
- Supports IEEE 802.3az Energy Efficient Ethernet (EEE)
- Supports Realtek Green Ethernet features
  - Link-On Cable Length Power Saving
  - Link-Down Power Saving
- Each port supports 3 parallel LED outputs
- Supports I^2C-like Slave interface or Slave MII Management interface to access configuration register
- Supports 32K-byte EEPROM space for configuration
- Build in 3.3V to 1.1V switch regulator with power MOS
- 25MHz crystal input or 3.3V OSC input
- 9x9 QFN 76-pin package

3. System Applications

3.1. 2-Port 1000Base-T Router with RGMII/TMII/RMII/MII

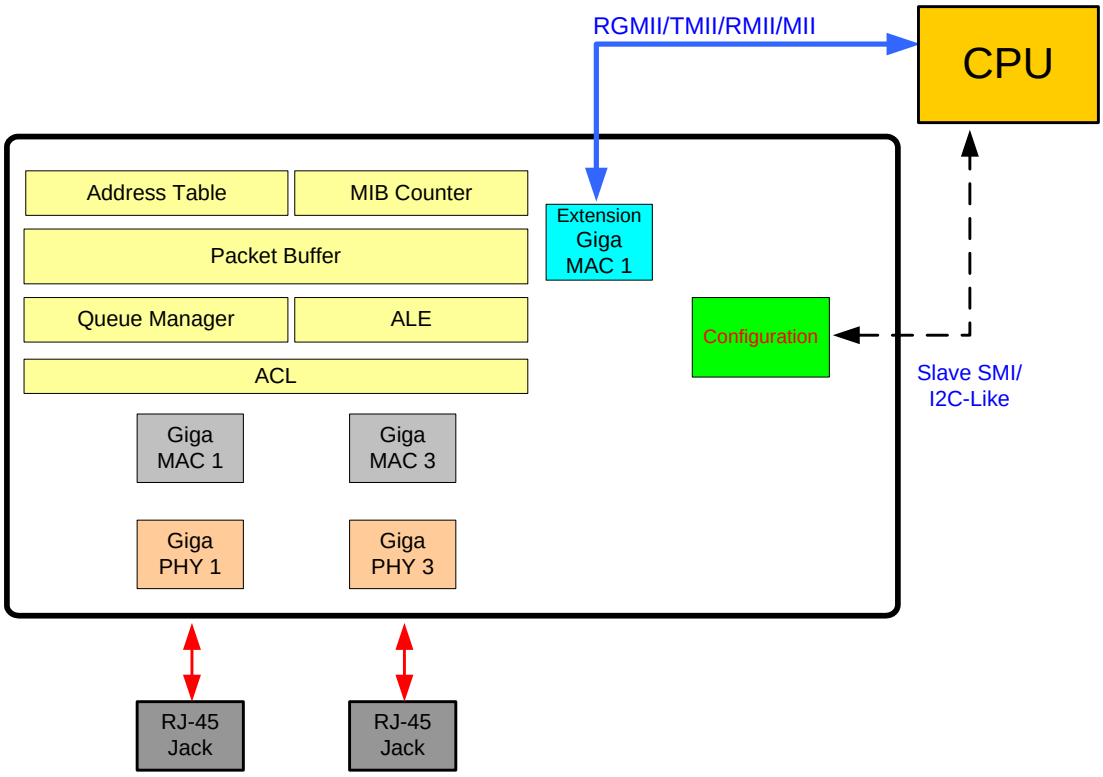


Figure 1. 2-Port 1000Base-T Router with RGMII/TMII/RMII/MII

4. Block Diagram

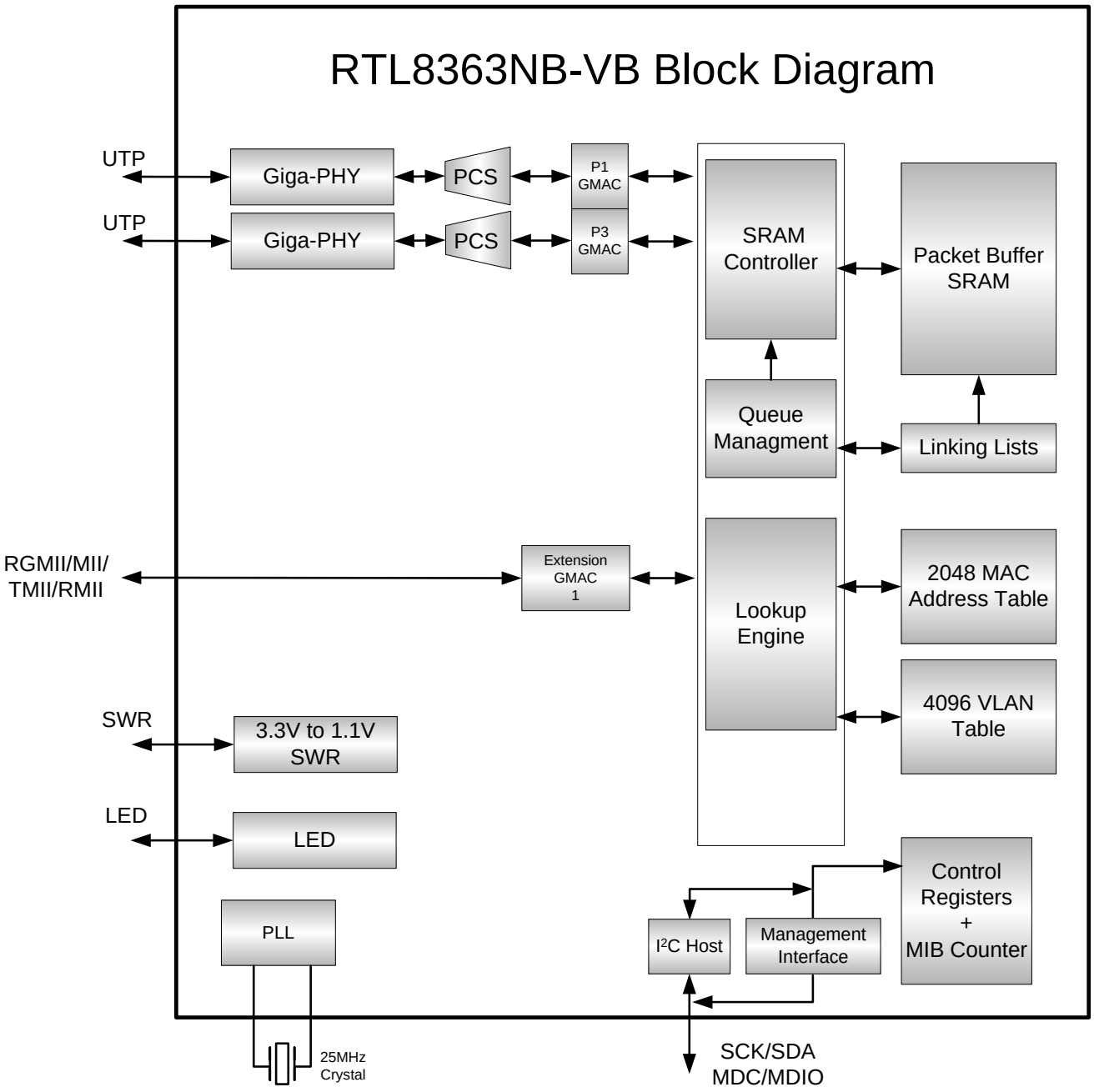


Figure 2. Block Diagram

5. Pin Assignments

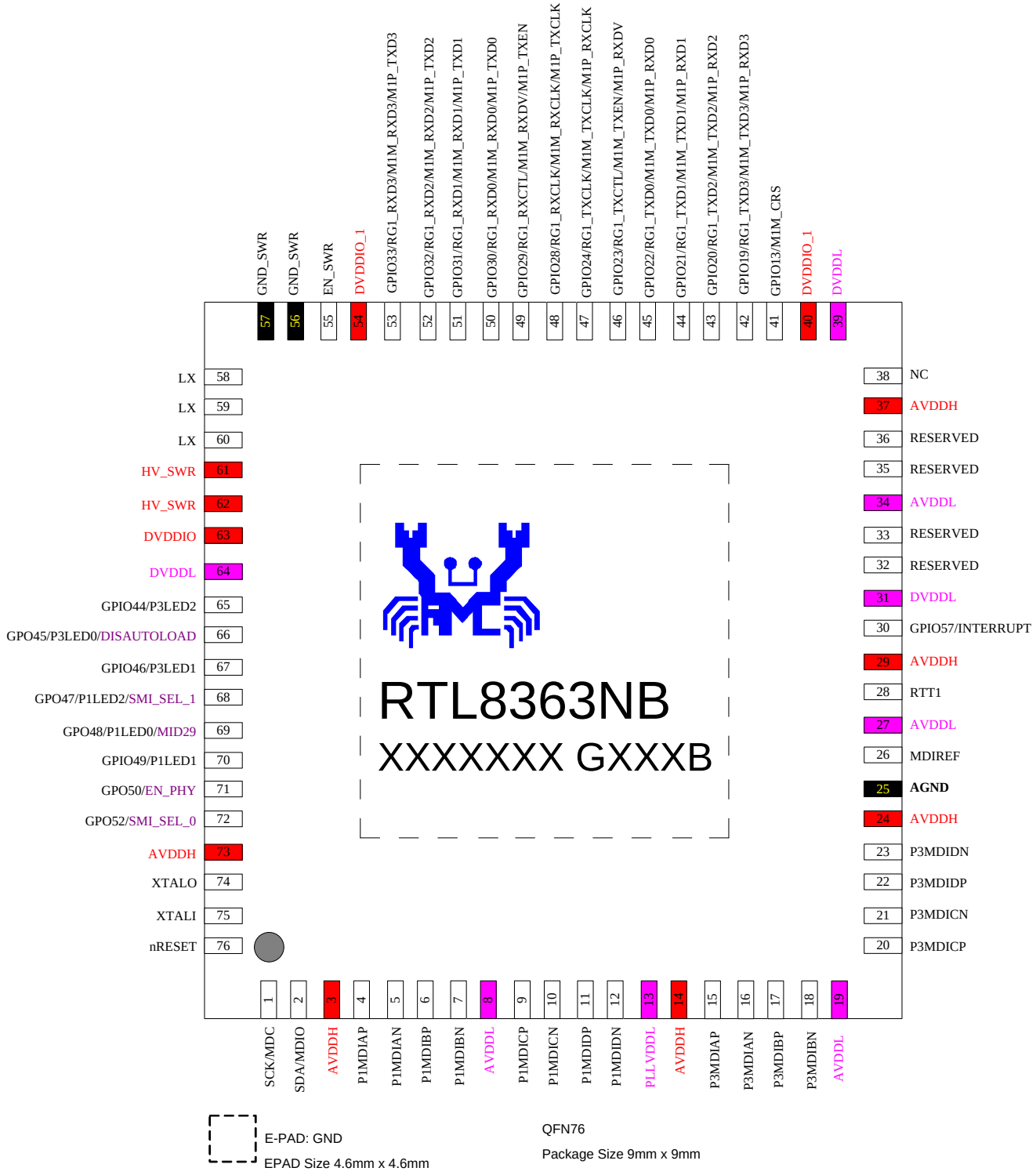


Figure 3. Pin Assignments (QFN-76)

5.1. Package Identification

Green package is indicated by the 'G' in GXXXX (Figure 3).

5.2. Pin Assignments Table

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Directional Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

I_{PU}: Input Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

AI: Analog Input Pin

AO: Analog Output Pin

AI/O: Analog Bi-Directional Input/Output Pin

AP: Analog Power Pin

AG: Analog Ground Pin

O_{PU}: Output Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

Table 1. Pin Assignment Table

Name	Pin No.	Type
SCK/MDC	1	I/O
SDA/MDIO	2	I/O
AVDDH	3	AP
P1MDIAP	4	AI/O
P1MDIAN	5	AI/O
P1MDIBP	6	AI/O
P1MDIBN	7	AI/O
AVDDL	8	AP
P1MDICP	9	AI/O
P1MDICN	10	AI/O
P1MDIDP	11	AI/O
P1MDIDN	12	AI/O
PLLVDDL	13	AP
AVDDH	14	AP
P3MDIAP	15	AI/O
P3MDIAN	16	AI/O
P3MDIBP	17	AI/O
P3MDIBN	18	AI/O
AVDDL	19	AP
P3MDICP	20	AI/O
P3MDICN	21	AI/O

Name	Pin No.	Type
P3MDIDP	22	AI/O
P3MDIDN	23	AI/O
AVDDH	24	AP
AGND	25	AG
MDIREF	26	AO
AVDDL	27	AP
RTT1	28	AO
AVDDH	29	AP
GPIO57/INTERRUPT	30	I/O_{PD}
DVDDL	31	P
RESERVED	32	-
RESERVED	33	-
AVDDL	34	AP
RESERVED	35	-
RESERVED	36	-
AVDDH	37	AP
NC	38	-
DVDDL	39	P
DVDDIO_1	40	P
GPIO13/M1M_CRS	41	I/O_{PD}

Name	Pin No.	Type
GPIO19/RG1_TXD3/ M1M_TXD3/M1P_RXD3	42	I/O
GPIO20/RG1_TXD2/ M1M_TXD2/M1P_RXD2	43	I/O
GPIO21/RG1_TXD1/ M1M_TXD1/M1P_RXD1	44	I/O
GPIO22/RG1_TXD0/ M1M_TXD0/M1P_RXD0	45	I/O
GPIO23/RG1_TXCTL/ M1M_TXEN/M1P_RXDV	46	I/O
GPIO24/RG1_TXCLK/ M1M_TXCLK/M1P_RXCLK	47	I/O
GPIO28/RG1_RXCLK/ M1M_RXCLK/M1P_TXCLK	48	I/O
GPIO29/RG1_RXCTL/ M1M_RXDV/M1P_TXEN	49	I/O
GPIO30/RG1_RXD0/ M1M_RXD0/M1P_TXD0	50	I/O
GPIO31/RG1_RXD1/ M1M_RXD1/M1P_TXD1	51	I/O
GPIO32/RG1_RXD2/ M1M_RXD2/M1P_TXD2	52	I/O
GPIO33/RG1_RXD3/ M1M_RXD3/M1P_TXD3	53	I/O
DVDDIO_1	54	P

Name	Pin No.	Type
EN_SWR	55	AI
GND_SWR	56	AG
GND_SWR	57	AG
LX	58	AO
LX	59	AO
LX	60	AO
HV_SWR	61	AI
HV_SWR	62	AI
DVDDIO	63	P
DVDDL	64	P
GPO44/P3LED2	65	I/O_{PU}
GPO45/P3LED0/DISAUTOLOAD	66	I/O_{PU}
GPIO46/P3LED1	67	I/O_{PU}
GPO47/ P1LED2/SMI_SEL_1	68	I/O_{PU}
GPO48/P1LED0/MID29	69	I/O_{PU}
GPIO49/P1LED1	70	I/O_{PU}
GPO50/EN_PHY	71	I/O_{PU}
GPO52/SMI_SEL_0	72	I/O_{PU}
AVDDH	73	AP
XTALO	74	AI/O
XTALI	75	AI
nRESET	76	I_{PU}

6. Pin Descriptions

6.1. Media Dependent Interface Pins

Table 2. Media Dependent Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
P1MDIAP/N P1MDIBP/N P1MDICP/N P1MDIDP/N	4 5 6 7 9 10 11 12	AI/O	10	Port 1 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P3MDIAP/N P3MDIBP/N P3MDICP/N P3MDIDP/N	15 16 17 18 20 21 22 23	AI/O	10	Port 3 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.

6.2. General Purpose Interfaces

The RTL8363NB-VB supports multi-function General Purpose Interfaces that can be configured as MII/RGMII mode for extension GMAC interface. The RTL8363NB-VB supports an extension interface (Extension GMAC1) for connecting with an external PHY, MAC, or CPU in specific applications. The extension interface supports RGMII, MII MAC mode, or MII PHY mode via register configuration.

Table 3. General Purpose Interfaces Pins

Pin No.	GPIO	RGMII	MII MAC Mode	MII PHY Mode	Other Function	Configuration Strapping
30	GPIO57	-	-	-	INTERRUPT	-
41	GPIO13	-	M1M_CRS	-	-	-
42	GPIO19	RG1_TXD3	M1M_TXD3	M1P_RXD3	-	-
43	GPIO20	RG1_TXD2	M1M_TXD2	M1P_RXD2	-	-
44	GPIO21	RG1_TXD1	M1M_TXD1	M1P_RXD1	-	-
45	GPIO22	RG1_TXD0	M1M_TXD0	M1P_RXD0	-	-
46	GPIO23	RG1_TXCTL	M1M_TXEN	M1P_RXDV	-	-
47	GPIO24	RG1_TXCLK	M1M_TXCLK	M1P_RXCLK	-	-
48	GPIO28	RG1_RXCLK	M1M_RXCLK	M1P_TXCLK	-	-
49	GPIO29	RG1_RXCTL	M1M_RXDV	M1P_TXEN	-	-
50	GPIO30	RG1_RXD0	M1M_RXD0	M1P_TXD0	-	-
51	GPIO31	RG1_RXD1	M1M_RXD1	M1P_TXD1	-	-
52	GPIO32	RG1_RXD2	M1M_RXD2	M1P_TXD2	-	-
53	GPIO33	RG1_RXD3	M1M_RXD3	M1P_TXD3	-	-
65	GPIO44	-	-	-	P3LED2	-
66	GPO45	-	-	-	P3LED0	DISAUTOLOAD
67	GPIO46	-	-	-	P3LED1	-
68	GPO47	-	-	-	P1LED2	SMI_SEL_1
69	GPO48	-	-	-	P1LED0	MID29
70	GPIO49	-	-	-	P1LED1	-
71	GPO50	-	-	-	-	EN_PHY
72	GPO52	-	-	-	-	SMI_SEL_0

6.2.1. RGMII Pins

The Extension GMAC1 of the RTL8363NB-VB supports RGMII interface connection to an external MAC or PHY device when register configuration is set to RGMII mode interface.

Table 4. Extension GMAC1 RGMII Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
RG1_TXD3 RG1_TXD2 RG1_TXD1 RG1_TXD0	42 43 44 45	O	-	RG1_TXD[3:0] Extension GMAC1 RGMII Transmit Data Output. Transmitted data is sent synchronously to RG1_TXCLK.
RG1_TXCTL	46	O	-	RG1_TXCTL Extension GMAC1 RGMII Transmit Control signal Output. The RG1_TXCTL indicates TX_EN at the rising edge of RG1_TXCLK, and TX_ER at the falling edge of RG1_TXCLK. At the RG1_TXCLK falling edge, RG1_TXCTL= TX_EN (XOR) TX_ER.
RG1_TXCLK	47	O	-	RG1_TXCLK Extension GMAC1 RGMII Transmit Clock Output. RG1_TXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG1_TXD[3:0] and RG1_TXCTL synchronization at RG1_TXCLK on both rising and falling edges.
RG1_RXCLK	48	I	-	RG1_RXCLK Extension GMAC1 RGMII Receive Clock Input. RG1_RXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG1_RXD[3:0] and RG1_RXCTL synchronization at both RG1_RXCLK rising and falling edges. This pin must be pulled low with a 1K ohm resistor when not used.
RG1_RXCTL	49	I	-	RG1_RXCTL Extension GMAC1 RGMII Receive Control signal input. The RG1_RXCTL indicates RX_DV at the rising of RG1_RXCLK and RX_ER at the falling edge of RG1_RXCLK. At RG1_RXCLK falling edge, RG1_RXCTL= RX_DV (XOR) RX_ER. This pin must be pulled low with a 1K ohm resistor when not used.
RG1_RXD0 RG1_RXD1 RG1_RXD2 RG1_RXD3	50 51 52 53	I	-	RG1_RXD[3:0] Extension GMAC1 RGMII Receive Data Input. Received data is received synchronously by RG1_RXCLK. These pins must be pulled low with a 1K ohm resistor when not used.

6.2.2. MII Pins

The Extension GMAC1 of the RTL8363NB-VB supports MII interface connection to an external MAC or PHY device when register configuration is set to MII mode interface. The MII interface can also be configured as MII MAC mode or MII PHY mode by register.

Table 5. Extension GMAC1 MII Pins (MII MAC Mode or MII PHY Mode)

Pin Name	Pin No.	Type	Drive (mA)	Description
M1M_CRS	41	I	-	M1M_CRS Extension GMAC1 MII MAC Mode Carrier Sense Input when operating in 10/100Mbps MII half duplex mode. This pin must be pulled low with a 1K ohm resistor when not used.
M1M_TXD3/ M1P_RXD3 M1M_TXD2/ M1P_RXD2 M1M_TXD1/ M1P_RXD1 M1M_TXD0/ M1P_RXD0	42 43 44 45	O	-	M1M_TXD[3:0] Extension GMAC1 MII MAC Mode Transmit Data Output. Transmitted data is sent synchronously at the rising edge of M1M_TXCLK. M1P_RXD[3:0] Extension GMAC1 MII PHY Mode Receive Data Output. Received data is received synchronously at the rising edge of M1P_RXCLK.
M1M_TXEN/ M1P_RXDV	46	O	-	M1M_TXEN Extension GMAC1 MII MAC Mode Transmit Data Enable Output. Transmit enable that is sent synchronously at the rising edge of M1M_TXCLK. M1P_RXDV Extension GMAC1 MII PHY Mode Receive Data Valid Output. Receive Data Valid signal that is sent synchronously at the rising edge of M1P_RXCLK.
M1M_TXCLK/ M1P_RXCLK	47	I/O	-	M1M_TXCLK Extension GMAC1 MII MAC Mode Transmit Clock Input. In MII 100Mbps, M1M_TXCLK is 25MHz Clock Input. In MII 10Mbps, M1M_TXCLK is 2.5MHz Clock Input. Used to synchronize M1M_TXD[3:0] and M1M_TXEN. M1P_RXCLK Extension GMAC1 MII PHY Mode Receive Clock Output. In MII 100Mbps, M1P_RXCLK is 25MHz Clock Output. In MII 10Mbps, M1P_RXCLK is 2.5MHz Clock Output. Used to synchronize M1P_RXD[3:0] and M1P_RXDV. This pin must be pulled low with a 1K ohm resistor when not used.
M1M_RXCLK/ M1P_TXCLK	48	I/O	-	M1M_RXCLK Extension GMAC1 MII MAC Mode Receive Clock Input. In MII 100Mbps, M1M_RXCLK is 25MHz Clock Input. In MII 10Mbps, M1M_RXCLK is 2.5MHz Clock Input. Used to synchronize M1M_RXD[3:0], M1M_RXDV, and M1M_CRS. M1P_TXCLK Extension GMAC1 MII PHY Mode Transmit Clock Output. In MII 100Mbps, M1P_TXCLK is 25MHz Clock Output. In MII 10Mbps, M1P_TXCLK is 2.5MHz Clock Output. Used to synchronize M1P_TXD[3:0] and M1P_TXEN. This pin must be pulled low with a 1K ohm resistor when not used.

Pin Name	Pin No.	Type	Drive (mA)	Description
M1M_RXDV/ M1P_TXEN	49	I	-	M1M_RXDV Extension GMAC1 MII MAC Mode Receive Data Valid Input. Receive Data Valid sent synchronously at the rising edge of M1M_RXCLK. M1P_TXEN Extension GMAC1 MII PHY Mode Transmit Data Enable Input. Transmit Data Enable is received synchronously at the rising edge of M1P_TXCLK. This pin must be pulled low with a 1K ohm resistor when not used.
M1M_RXD0/ M1P_TXD0 M1M_RXD1/ M1P_TXD1 M1M_RXD2/ M1P_TXD2 M1M_RXD3/ M1P_TXD3	50 51 52 53	I	-	M1M_RXD[3:0] Extension GMAC1 MII MAC Mode Receive Data Input. Received data that is received synchronously at the rising edge of M1M_RXCLK. M1P_TXD[3:0] Extension GMAC1 MII PHY Mode Transmit Data Input. Transmitted data is received synchronously at the rising edge of M1P_TXCLK. These pins must be pulled low with a 1K ohm resistor when not used.

6.3. LED Pins

The RTL8363NB-VB LED Pins can be configured to parallel mode LED or serial mode LED interface via Register configuration. LED0, LED1, and LED2 of Port n indicate information that can be defined via register or EEPROM.

In parallel LED mode, when the LED pin is pulled low, the LED output polarity will be high active. When the LED pin is pulled high, the LED output polarity will change from high active to low active. See section 8.17 LED Indicators, page 32 for more details.

Table 6. LED Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
P1LED0/ MID29	69	I/O_{PU}	-	LAN 1 LED0 Output Signal. P1LED0 indicates information is defined by register or EEPROM. See section 8.17, page 32 for more details.
P1LED1	70	I/O_{PU}	-	LAN 1 LED1 Output Signal. P1LED1 indicates information is defined by register or EEPROM. See section 8.17, page 32 for more details.
P1LED2/ SMI_SEL_1	68	I/O_{PU}	-	LAN 1 LED2 Output Signal. P1LED2 indicates information is defined by register or EEPROM. See section 8.17, page 32 for more details.
P3LED0/ DISAUTOLOAD	66	I/O_{PU}	-	LAN 2 LED0 Output Signal. P3LED0 indicates information is defined by register or EEPROM. See section 8.17, page 32 for more details.
P3LED1	67	I/O_{PU}	-	LAN 2 LED1 Output Signal. P3LED1 indicates information is defined by register or EEPROM. See section 8.17, page 32 for more details.
P3LED2	65	I/O_{PU}	-	LAN 2 LED2 Output Signal. P3LED2 indicates information is defined by register or EEPROM. See section 8.17, page 32 for more details.

6.4. Configuration Strapping Pins

Table 7. Configuration Strapping Pins

Pin Name	Pin No.	Type	Description
DISAUTOLOAD / P3LED0	66	I/O_{PU}	Disable EEPROM Auto-load. Pull Up: Disable EEPROM auto-load Pull Down: Enable EEPROM auto-load *Note 1: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active. See section 8.17 LED Indicators, page 32 for more details.*
SMI_SEL_1 / P1LED2	68	I/O_{PU}	External CPU Access Interface Selection. SMI_SEL[1:0]: 00：LSB I^2C mode 01：MSB I^2C mode 10：Slave MII Management MDC/MDIO 11：Realtek I^2C-like mode *Note: These pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active. See section 8.17 LED Indicators, page 32 for more details.*
SMI_SEL_0	72	I/O_{PU}	
MID29 / P1LED0	69	I/O_{PU}	Select .MID29. Pull Up: MII Management Interface PHY ID is 29 Pull Down: MII Management Interface PHY ID is 0 *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active. See section 8.17 LED Indicators, page 32 for more details.*
EN_PHY	71	I/O_{PU}	Enable Embedded PHY. Pull Up: Enable embedded PHY Pull Down: Disable embedded PHY *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*

6.5. Management Interface Pins

Table 8. Management Interface Pins

Pin Name	Pin No.	Type	Description
SCK/ MDC	1	I/O_{PU}	Master I2C Interface Clock for EEPROM auto-download. Slave I2C Interface Clock for external CPU to access DUT. Slave MII Management Interface Clock (selected via the hardware strapping SMI_SEL_1 & SMI_SEL_0).
SDA/ MDIO	2	I/O	Master I2C Interface Data for EEPROM auto-download. Slave I2C Interface Data for external CPU to access DUT. Slave MII Management Interface Data (selected via the hardware strapping SMI_SEL_1 & SMI_SEL_0).

Pin Name	Pin No.	Type	Description
INTERRUPT	30	O_{PD}	Interrupt output when Interrupt even occurs. Active High by pull-down to GND via a 1K resister. Active Low by pull-up to DVDDIO via a 4.7K resister.

6.6. Miscellaneous Pins

Table 9. Miscellaneous Pins

Pin Name	Pin No.	Type	Description
XTALO	74	AI/O	25MHz Crystal Clock Output Pin. 25MHz +/-50ppm tolerance crystal output. When using a crystal, connect a loading capacitor from each pad to ground.
XTALI	75	AI	25MHz Crystal Clock Input Pin. 25MHz +/-50ppm tolerance crystal reference.
nRESET	76	I_{PU}	System Reset Input Pin. When low active will reset the RTL8363NB-VB.
MDIREF	26	AO	Reference Resistor. A 2.49K ohm (1%) resistor must be connected between MDIREF and GND.
NC	38	-	Not Connected.
GPIO13	41	I/O_{PD}	General Purpose Input/Output Interface IO13.
GPIO19	42	I/O	General Purpose Input/Output Interface IO19.
GPIO20	43	I/O	General Purpose Input/Output Interface IO20.
GPIO21	44	I/O	General Purpose Input/Output Interface IO21.
GPIO22	45	I/O	General Purpose Input/Output Interface IO22.
GPIO23	46	I/O	General Purpose Input/Output Interface IO23.
GPIO24	47	I/O	General Purpose Input/Output Interface IO24.
GPIO28	48	I/O	General Purpose Input/Output Interface IO28.
GPIO29	49	I/O	General Purpose Input/Output Interface IO29.
GPIO30	50	I/O	General Purpose Input/Output Interface IO30.
GPIO31	51	I/O	General Purpose Input/Output Interface IO31.
GPIO32	52	I/O	General Purpose Input/Output Interface IO32.
GPIO33	53	I/O	General Purpose Input/Output Interface IO33.
GPIO44	65	I/O_{PU}	General Purpose Input/Output Interface IO44.
GPO45/ P3LED0/ DISAUTOLOAD	66	I/O_{PU}	General Purpose Output Interface IO45.
GPIO46/ P3LED1	67	I/O_{PU}	General Purpose Input/Output Interface IO46.
GPO47/ P1LED2/ SMI_SEL_1	68	I/O_{PU}	General Purpose Output Interface O47.
GPO48/ P1LED0/ MID29	69	I/O_{PU}	General Purpose Output Interface O48.

Pin Name	Pin No.	Type	Description
GPIO49/ P1LED1	70	I/O_{PU}	General Purpose Input/Output Interface IO49.
GPO50/ EN_PHY	71	I/O_{PU}	General Purpose Output Interface IO50.
GPO52/ SMI_SEL_0	72	I/O_{PU}	General Purpose Output Interface IO52.
GPIO57/ INTERRUPT	30	I/O_{PD}	General Purpose Input/Output Interface IO57.

6.7. Test Pins

Table 10. Test Pins

Pin Name	Pin No.	Type	Description
RTT1	28	AO	Reserved for Internal Use. Must be left floating.

6.8. Embedded Switch Regulator Pins

Table 11. Embedded Switch Regulator Pins

Pin Name	Pin No.	Type	Description
EN_SWR	55	AI	Enable embedded switch regulator. Pull Up: Enable embedded switch regulator. Pull Down: Disable embedded switch regulator. Note: pulled high or low via an external 4.7k ohm resistor to enable or disable embedded switch regulator.
GND_SWR	56, 57	AG	Regulator Ground.
LX	58, 59, 60	AO	Regulator output. It should connect to the external inductor.
HV_SWR	61, 62	AP	Regulator Power Supply Input.

6.9. Power and GND Pins

Table 12. Power and GND Pins

Pin Name	Pin No.	Type	Description
DVDDIO_1	40, 54	P	Digital I/O High Voltage Power for Extension Port 1 General Purpose Interface.
DVDDIO	63	P	Digital I/O High Voltage Power for LED, Management Interface, nRESET.
DVDDL	31, 39, 64	P	Digital Low Voltage Power.
AVDDH	3, 14, 24, 29, 37, 73	AP	Analog High Voltage Power. Including supply I/O power for INTERRUPT pin.
AVDDL	8, 19, 27, 34	AP	Analog Low Voltage Power.
PLLVDDL	13	AP	PLL Low Voltage Power.
AGND	25	AG	Analog GND.
GND	EPAD	G	Ground.

7. Physical Layer Functional Overview

7.1. MDI Interface

The RTL8363NB-VB embeds Dual 10/100/1000M Ethernet PHYs in one chip. Each port uses a single common MDI interface to support 1000Base-T, 100Base-TX, and 10Base-T. This interface consists of four signal pairs-A, B, C, and D. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors, and therefore reduces BOM cost and PCB complexity. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used.

7.2. 1000Base-T Transmit Function

The 1000Base-TX transmit function performs 8B/10B coding, scrambling, and 4D-PAM5 encoding. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

7.3. 1000Base-T Receive Function

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is then processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The RX MAC retrieves the packet data from the internal receive MII/GMII interface and sends it to the packet buffer manager.

7.4. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven onto the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.

7.5. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A de-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

7.6. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

7.7. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

7.8. Auto-Negotiation for UTP

The RTL8363NB-VB obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8363NB-VB advertises full capabilities (1000Full, 100Full, 100Half, 10Full, 10Half) together with flow control ability.

7.9. Crossover Detection and Auto Correction

The RTL8363NB-VB automatically determines whether or not it needs to crossover between pairs (see Table 13) so that an external crossover cable is not required. When connecting to another device that does not perform MDI crossover, when necessary, the RTL8363NB-VB automatically switches its pin pairs to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The crossover detection and auto correction function can be disabled via register configuration. The pin mapping in MDI and MDI Crossover mode is given below.

Table 13. Media Dependent Interface Pin Mapping

Pairs	MDI			MDI Crossover		
	1000Base-T	100Base-TX	10Base-T	1000Base-T	100Base-TX	10Base-T
A	A	TX	TX	B	RX	RX
B	B	RX	RX	A	TX	TX
C	C	Unused	Unused	D	Unused	Unused
D	D	Unused	Unused	C	Unused	Unused

7.10. Polarity Correction

The RTL8363NB-VB automatically corrects polarity errors on the receiver pairs in 1000Base-T and 10Base-T modes. In 100Base-TX mode, the polarity is irrelevant.

In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the de-scrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-T mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

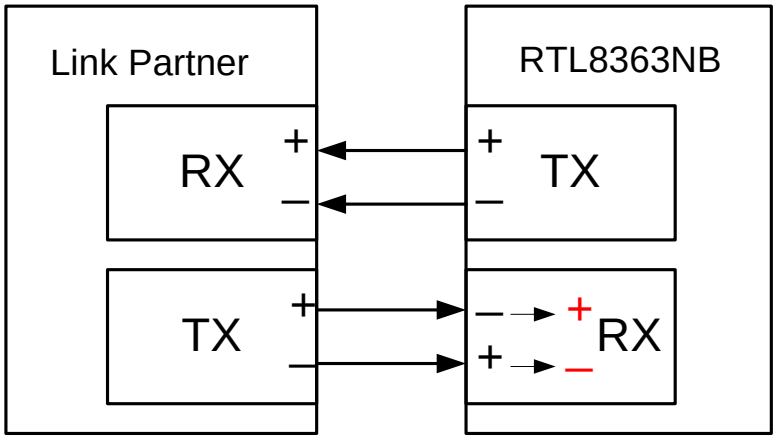


Figure 4. Conceptual Example of Polarity Correction

8. General Function Description

8.1. Reset

8.1.1. Hardware Reset

In a power-on reset, an internal power-on reset pulse is generated and the RTL8363NB-VB will start the reset initialization procedures. These are:

- Determine various default settings via the hardware strap pins at the end of the nRESET signal
- Auto-load the configuration from EEPROM if EEPROM is detected
- Complete the embedded SRAM BIST process
- Initialize the packet buffer descriptor allocation
- Initialize the internal registers and prepare them to be accessed by the external CPU

8.1.2. Software Reset

The RTL8363NB-VB supports two software resets; a chip reset and a soft reset.

8.1.2.1 CHIP_RESET

When CHIP_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Download configuration from strap pin and EEPROM
2. Start embedded SRAM BIST (Built-In Self Test)
3. Clear all the Lookup and VLAN tables
4. Reset all registers to default values
5. Restart the auto-negotiation process

8.1.2.2 SOFT_RESET

When SOFT_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Clear the FIFO and re-start the packet buffer link list
2. Restart the auto-negotiation process

8.2. IEEE 802.3x Full Duplex Flow Control

The RTL8363NB-VB supports IEEE 802.3x flow control in 10/100/1000M modes. Flow control can be decided in two ways:

- When Auto-Negotiation is enabled, flow control depends on the result of NWay
- When Auto-Negotiation is disabled, flow control depends on register definition

8.3. Half Duplex Flow Control

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. The scheduling of the retransmissions is determined by a controlled randomization process called 'Truncated Binary Exponential Backoff'. At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slot time (512 bit times). The number of slot times to delay before the nth retransmission attempt is chosen as a uniformly distributed random integer 'r' in the range:

$0 \leq r < 2k$

where:

k = min (n, backoffLimit). The backoffLimit for the RTL8363NB-VB is 9.

The half duplex back-off algorithm in the RTL8363NB-VB does not have the maximum retry count limitation of 16 (as defined in IEEE 802.3). This means packets in the switch will not be dropped if the back-off retry count is over 16.

8.3.1. Back-Pressure Mode

In Back-Pressure mode, the RTL8363NB-VB sends a 4-byte jam pattern (data=0xAA) to collide with incoming packets when congestion control is activated. The Jam pattern collides at the fourth byte counted from the preamble. The RTL8363NB-VB supports 48PASS1, which receives one packet after 48 consecutive jam collisions (data collisions are not included in the 48). Enable this function to prevent port partition after 63 consecutive collisions (data collisions + consecutive jam collisions).

8.4. Search and Learning

Search

When a packet is received, the RTL8363NB-VB uses the destination MAC address, Filtering Identifier (FID) and Enhanced Filtering Identifier (EFID) to search the 2K-entry look-up table. The 48-bit MAC address, 4-bit FID and 3-bit EFID use a hash algorithm, to calculate an 11-bit index value. The RTL8363NB-VB uses the index to compare the packet MAC address with the entries (MAC addresses) in the look-up table. This is the 'Address Search'. If the destination MAC address is not found, the switch will broadcast the packet according to VLAN configuration.

Learning

The RTL8363NB-VB uses the source MAC address, FID, and EFID of the incoming packet to hash into a 9-bit index. It then compares the source MAC address with the data (MAC addresses) in this index. If there is a match with one of the entries, the RTL8363NB-VB will update the entry with new information. If there is no match and the 2K entries are not all occupied by other MAC addresses, the RTL8363NB-VB will record the source MAC address and ingress port number into an empty entry. This process is called 'Learning'.

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The look-up engine will update the time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aged out) if its time stamp information is not refreshed by the address learning process during the aging time period. The aging time of the RTL8363NB-VB is between 200 and 400 seconds (typical is 300 seconds).

8.5. SVL and IVL/SVL

The RTL8363NB-VB supports a 16-group Filtering Identifier (FID) for L2 search and learning. In default operation, all VLAN entries belong to the same FID. This is called Shared VLAN Learning (SVL). If VLAN entries are configured to different FIDs, then the same source MAC address with multiple FIDs can be learned into different look-up table entries. This is called Independent VLAN Learning and Shared VLAN Learning (IVL/SVL).

8.6. Illegal Frame Filtering

Illegal frames such as CRC error packets, runt packets (length <64 bytes), and oversize packets (length >maximum length) will be discarded by the RTL8363NB-VB. The maximum packet length may be set from 1518 bytes to 16K bytes.

8.7. IEEE 802.3 Reserved Group Addresses Filtering Control

The RTL8363NB-VB supports the ability to drop/forward IEEE 802.3 specified reserved group MAC addresses: 01-80-C2-00-00-00 to 01-80-C2-00-00-2F. The default setting enables forwarding of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause) and 01-80-C2-00-00-02 (802.3ad LACP) will always be filtered. Table 14 shows the Reserved Multicast Address (RMA) configuration mode from 01-80-C2-00-00-00 to 01-80-C2-00-00-2F.

Table 14. Reserved Multicast Address Configuration Table

Assignment	Value
Bridge Group Address	01-80-C2-00-00-00
IEEE Std 802.3, 1988 Edition, Full Duplex PAUSE Operation	01-80-C2-00-00-01
IEEE Std 802.3ad Slow Protocols-Multicast Address	01-80-C2-00-00-02
IEEE Std 802.1X PAE Address	01-80-C2-00-00-03
Provider Bridge Group Address	01-80-C2-00-00-08
Undefined 802.1 Address	01-80-C2-00-00-04 ~ 01-80-C2-00-00-07 & 01-80-C2-00-00-09 ~ 01-80-C2-00-00-0C & 01-80-C2-00-00-0F
Provider Bridge MVRP Address	01-80-C2-00-00-0D
IEEE Std 802.1AB Link Layer Discovery Protocol Address	01-80-C2-00-00-0E
All LANs Bridge Management Group Address	01-80-C2-00-00-10
Load Server Generic Address	01-80-C2-00-00-11
Loadable Device Generic Address	01-80-C2-00-00-12
Undefined 802.1 Address	01-80-C2-00-00-13 ~ 01-80-C2-00-00-17 & 01-80-C2-00-00-19 & 01-80-C2-00-00-1B ~ 01-80-C2-00-00-1F
Generic Address for All Manager Stations	01-80-C2-00-00-18
Generic Address for All Agent Stations	01-80-C2-00-00-1a
GMRP Address	01-80-C2-00-00-20
GVRP Address	01-80-C2-00-00-21
Undefined GARP Address	01-80-C2-00-00-22 | 01-80-C2-00-00-2F
CDP(Cisco Discovery Protocol)	01-00-0C-CC-CC-CC
CSSTP(Cisco Shared Spanning Tree Protocol)	01-00-0C-CC-CC-CD
LLDP	(01:80:c2:00:00:0e or 01:80:c2:00:00:03 or 01:80:c2:00:00:00) && ethertype = 0x88CC

8.8. Broadcast/Multicast/Unknown DA Storm Control

The RTL8363NB-VB enables or disables per-port broadcast/multicast/unknown DA storm control by setting registers (default is disabled). After the receiving rate of broadcast/multicast/unknown DA packets exceeds a reference rate (number of Kbps per second or number of packets per second), all other broadcast/multicast/unknown DA packets will be dropped. The reference rate is set via register configuration.

8.9. Port Security Function

The RTL8363NB-VB supports three types of security function to prevent malicious attacks:

- Per-port enable/disable SA auto-learning for an ingress packet
- Per-port enable/disable look-up table aging update function for an ingress packet
- Per-port enable/disable drop all unknown DA packets

8.10. MIB Counters

The RTL8363NB-VB supports a set of counters to support management functions.

- MIB-II (RFC 1213)
- Ethernet-Like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)

8.11. Port Mirroring

The RTL8363NB-VB supports one set of port mirroring functions for all ports. The TX, or RX, or both TX/RX packets from multiple mirrored port can be mirrored to one monitor port.

8.12. VLAN Function

The RTL8363NB-VB supports 4K VLAN groups. These can be configured as port-based VLANs, IEEE 802.1Q tag-based VLANs, and Protocol-based VLANs. Two ingress-filtering and egress-filtering options provide flexible VLAN configuration:

Ingress Filtering

- The acceptable frame type of the ingress process can be set to 'Admit All', 'Admit only Untagged' or 'Admit only Tagged'
- 'Admit' or 'Discard' frames associated with a VLAN for which that port is not in the member set

Egress Filtering

- 'Forward' or 'Discard' Leaky VLAN frames between different VLAN domains
- 'Forward' or 'Discard' Multicast VLAN frames between different VLAN domains

The VLAN tag can be inserted or removed at the output port. The RTL8363NB-VB will insert a Port VID (PVID) for untagged frames, or remove the tag from tagged frames. The RTL8363NB-VB also supports a special insert VLAN tag function to separate traffic from the WAN and LAN sides in Router and Gateway applications.

In router applications, the router may want to know which input port this packet came from. The RTL8363NB-VB supports Port VID (PVID) for each port and can insert a PVID in the VLAN tag on egress. Using this function, VID information carried in the VLAN tag will be changed to PVID. The RTL8363NB-VB also provides an option to admit VLAN tagged packets with a specific PVID only. If this function is enabled, it will drop non-tagged packets and packets with an incorrect PVID.

8.12.1. Port-Based VLAN

This default configuration of the VLAN function can be modified via an attached serial EEPROM or EEPROM SMI Slave interface. The 4K-entry VLAN Table designed into the RTL8363NB-VB provides full flexibility for users to configure the input ports to associate with different VLAN groups. Each input port can join with more than one VLAN group.

Port-based VLAN mapping is the simplest implicit mapping rule. Each ingress packet is assigned to a VLAN group based on the input port. It is not necessary to parse and inspect frames in real-time to determine their VLAN association. All the packets received on a given input port will be forwarded to this port's VLAN members.

8.12.2. IEEE 802.1Q Tag-Based VLAN

The RTL8363NB-VB supports 4K VLAN entries to perform 802.1Q tag-based VLAN mapping. In 802.1Q VLAN mapping, the RTL8363NB-VB uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. The RTL8363NB-VB compares the explicit identifier in the VLAN tag with the 4K VLAN Table to determine the VLAN association of this packet, and then forwards this packet to the member set of that VLAN. Two VIDs are reserved for special purposes. One of them is all 1's, which is reserved and currently unused. The other is all 0's, which indicates a priority tag. A priority-tagged frame should be treated as an untagged frame.

When ‘802.1Q tag aware VLAN’ is enabled, the RTL8363NB-VB performs 802.1Q tag-based VLAN mapping for tagged frames, but still performs port-based VLAN mapping for untagged frames. If ‘802.1Q tag aware VLAN’ is disabled, the RTL8363NB-VB performs only port-based VLAN mapping both on non-tagged and tagged frames. The processing flow when ‘802.1Q tag aware VLAN’ is enabled is illustrated below.

Two VLAN ingress filtering functions are supported in registers by the RTL8363NB-VB. One is the ‘VLAN tag admit control, which provides the ability to receive VLAN-tagged frames only. Untagged or priority tagged (VID=0) frames will be dropped. The other is ‘VLAN member set ingress filtering’, which will drop frames if the ingress port is not in the member set.

8.12.3. Protocol-Based VLAN

The RTL8363NB-VB supports a 4-group Protocol-based VLAN configuration. The packet format can be RFC 1042, LLC, or Ethernet, as shown in Figure 5. There are 4 configuration tables to assign the frame type and corresponding field value. Taking IP packet configuration as an example, the user can configure the frame type to be ‘Ethernet’, and value to be ‘0x0800’. Each table will index to one of the entries in the 4K-entry VLAN table. The packet stream will match the protocol type and the value will follow the VLAN member configuration of the indexed entry to forward the packets.

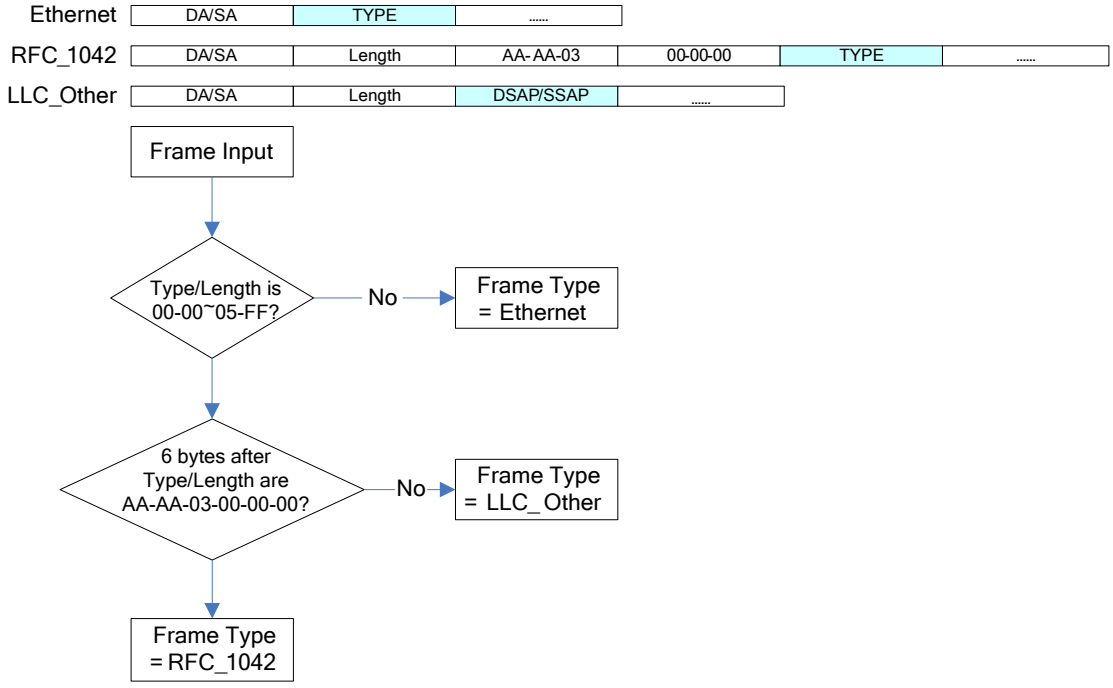


Figure 5. Protocol-Based VLAN Frame Format and Flow Chart

8.12.4. Port VID

In a router application, the router may want to know which input port this packet came from. The RTL8363NB-VB supports Port VID (PVID) for each port to insert a PVID in the VLAN tag for untagged or priority tagged packets on egress. When 802.1Q tag-aware VLAN is enabled, VLAN tag admit control is enabled, and non-PVID Discard is enabled at the same time. When these functions are enabled, the RTL8363NB-VB will drop non-tagged packets and packets with an incorrect PVID.

8.13. QoS Function

The RTL8363NB-VB supports 8 priority queues and input bandwidth control. Packet priority selection can depend on Port-based priority, 802.1p/Q Tag-based priority, IPv4/IPv6 DSCP-based priority, and ACL-based priority. When multiple priorities are enabled in the RTL8363NB-VB, the packet's priority will be assigned based on the priority selection table.

Each queue has one leaky bucket for Average Packet Rate. Per-queue in each output port can be set as Strict Priority (SP) or Weighted Fair Queue (WFQ) for packet scheduling algorithm.

8.13.1. Input Bandwidth Control

Input bandwidth control limits the input bandwidth. When input traffic is more than the RX Bandwidth parameter, this port will either send out a 'pause ON' frame, or drop the input packet depending on register setup. Per-port input bandwidth control rates can be set from 8Kbps to 1Gbps (in 8Kbps steps).

8.13.2. Priority Assignment

Priority assignment specifies the priority of a received packet according to various rules. The RTL8363NB-VB can recognize the QoS priority information of incoming packets to give a different egress service priority.

The RTL8363NB-VB identifies the priority of packets based on several types of QoS priority information:

- Port-based priority
- 802.1p/Q-based priority
- IPv4/IPv6 DSCP-based priority
- ACL-based priority
- VLAN-based priority
- MAC-based priority
- SVLAN-based priority

8.13.3. Priority Queue Scheduling

The RTL8363NB-VB supports MAX-MIN packet scheduling.

Packet scheduling offers two modes:

- Average Packet Rate (APR) leaky bucket, which specifies the average rate of one queue
- Weighted Fair Queue (WFQ), which decides which queue is selected in one slot time to guarantee the minimal packet rate of one queue
- Weighted Round Robin (WRR)

In addition, each queue of each port can select Strict Priority or WFQ or WRR packet scheduling according to packet scheduling mode.

8.13.4. IEEE 802.1p/Q and DSCP Remarking

The RTL8363NB-VB supports the IEEE 802.1p/Q and IP DSCP (Differentiated Services Code Point) remarking function. When packets egress from one of the 8 queues, the packet's 802.1p/Q priority and IP DSCP can optionally be remarked to a configured value. 802.1p/Q priority & IP DSCP value can be remarked based on internal priority or original 802.1p/Q priority & IP DSCP value in packets.

8.13.5. ACL-Based Priority

The RTL8363NB-VB supports 48-entry ACL (Access Control List) rules. When a packet is received, its physical port, Layer2, Layer3, and Layer4 information are recorded and compared to ACL entries.

If a received packet matches multiple entries, the entry with the lowest address is valid. If the entry is valid, the action bit and priority bit will be applied.

- If the action bit is 'Drop', the packet will be dropped. If the action bit is 'CPU', the packet will be trapped to the CPU instead of forwarded to non-CPU ports (except where it will be dropped by rules other than the ACL rule)
- If the action bit is 'Permit', ACL rules will override other rules
- If the action bit is 'Mirror', the packet will be forwarded to the mirror port and the L2 lookup result destination port. The mirror port indicates the port configured in the port mirror mechanism
- The priority bit will take effect only if the action bit is 'CPU', 'Permit', and 'Mirror'. The Priority bit is used to determine the packet queue ID according to the priority assignment mechanism

8.14. IEEE 802.1x Function

The RTL8363NB-VB supports IEEE 802.1x Port-based/MAC-based Access Control.

- Port-Based Access Control for each port
- Authorized Port-Based Access Control for each port
- Port-Based Access Control Direction for each port
- MAC-Based Access Control for each port
- MAC-Based Access Control Direction

- Optional Unauthorized Behavior

8.14.1. Port-Based Access Control

Each port of the RTL8363NB-VB can be set to 802.1x port-based authenticated checking function usage and authorized status. Ports with 802.1X unauthorized status will drop received/transmitted frames.

8.14.2. Authorized Port-Based Access Control

If a dedicated port is set to 802.1x port-based access control, and passes the 802.1x authorization, then its port authorization status can be set to authorized.

8.14.3. Port-Based Access Control Direction

Ports with 802.1X unauthorized status will drop received/transmitted frames only when port authorization direction is 'BOTH'. If the authorization direction of an 802.1X unauthorized port is IN, incoming frames to that port will be dropped, but outgoing frames will be transmitted.

8.14.4. MAC-Based Access Control

MAC-Based Access Control provides authentication for multiple logical ports. Each logical port represents a source MAC address. There are multiple logical ports for a physical port. When a logical port or a MAC address is authenticated, the relevant source MAC address has the authorization to access the network. A frame with a source MAC address that is not authenticated by the 802.1x function will be dropped or trapped to the CPU.

8.14.5. MAC-Based Access Control Direction

Unidirectional and Bi-directional control are two methods used to process frames in 802.1x. As the system cannot predict which port the DA is on, a system-wide MAC-based access control direction setup is provided for determining whether receiving or bi-direction should be authorized.

If MAC-based access control direction is BOTH, then received frames with unauthenticated SA or unauthenticated DA will be dropped. When MAC-based access control direction is IN, only received frames with unauthenticated SA will be dropped.

8.14.6. Optional Unauthorized Behavior

Both in Port-Based Network Access Control and MAC-Based Access Control, a whole system control setup is provided to determine unauthorized frame dropping, trapping to CPU, or tagging as belonging to a Guest VLAN (see the following 'Guest VLAN' section).

8.15. IEEE 802.1D Function

When using IEEE 802.1D, the RTL8363NB-VB supports 16 sets and four status' for each port for CPU implementation 802.1D (STP) and 802.1s (MSTP) function:

- Disabled: The port will not transmit/receive packets, and will not perform learning
- Blocking: The port will only receive BPDU spanning tree protocol packets, but will not transmit any packets, and will not perform learning
- Learning: The port will receive any packet, including BPDU spanning tree protocol packets, and will perform learning, but will only transmit BPDU spanning tree protocol packets
- Forwarding: The port will transmit/receive all packets, and will perform learning

The RTL8363NB-VB also supports a per-port transmission/reception enable/disable function. Users can control the port state via register.

8.16. Realtek Cable Test (RTCT)

The RTL8363NB-VB physical layer transceivers use DSP technology to implement the Realtek Cable Test (RTCT) feature. The RTCT function can be used to detect short, open, or impedance mismatch in each differential pair. The RTL8363NB-VB also provides LED support to indicate test status and results.

8.17. LED Indicators

The RTL8363NB-VB supports parallel LEDs for each port. Each port has three LED indicator pins, LED0, LED1, and LED2. Each pin may have different indicator information (defined in Table 15). Refer to section 6.3 LED Pins, page 15 for pin details. Upon reset, the RTL8363NB-VB supports chip diagnostics and LED operation test by blinking all LEDs once.

Table 15. LED Definitions

LED Statuses	Description
LED_Off	LED Pin Output Disable.
Dup/Col	Duplex/Collision Indicator. Blinking when collision occurs. Low for full duplex, and high for half duplex mode.
Link/Act	Link, Activity Indicator. Low for link established. Link/Act Blinking when the corresponding port is transmitting or receiving.
Spd1000	1000Mbps Speed Indicator. Low for 1000Mbps.
Spd100	100Mbps Speed Indicator. Low for 100Mbps.
Spd10	10Mbps Speed Indicator. Low for 10Mbps.
Spd1000/Act	1000Mbps Speed/Activity Indicator. Low for 1000Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd100/Act	100Mbps Speed/Activity Indicator. Low for 100Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd10/Act	10Mbps Speed/Activity Indicator. Low for 10Mbps. Blinking when the corresponding port is transmitting or receiving.

LED Statuses	Description
Spd100 (10)/Act	10/100Mbps Speed/Activity Indicator. Low for 10/100Mbps. Blinking when the corresponding port is transmitting or receiving.
Act	Activity Indicator. Act blinking when the corresponding port is transmitting or receiving.

The LED pin also supports pin strapping configuration functions. The PnLED0, PnLED1, and PnLED2 pins are dual-function pins: input operation for configuration upon reset, and output operation for LED after reset. When the pin input is pulled high upon reset, the pin output is active low after reset. When the pin input is pulled down upon reset, the pin output is active high after reset (see Figure 6 and Figure 7). Typical values for pull-up/pull-down resistors are 4.7KΩ.

The PnLED1 can be combined with PnLED0 or LANnLED2 as a Bi-color LED.

The PnLED1 should operate with the same polarity as other Bi-color LED pins. For example:

- P1LED1 should pull up upon reset if P1LED1 is combined with P1LED2 as a Bi-color LED, and P1LED2 input is pulled high upon reset. In this configuration, the output of these pins is active low after reset
- P1LED1 should be pulled down upon reset if P1LED1 is combined with P1LED2 as a Bi-color LED, and P1LED2 input is pulled down upon reset. In this configuration, the output of these pins is active high after reset

Upon reset, the RTL8363NB-VB supports chip diagnostics and LED functions by blinking all LEDs once. This function can be disabled by asserting EN_PWRLIGHT to 0b0 (pull down).

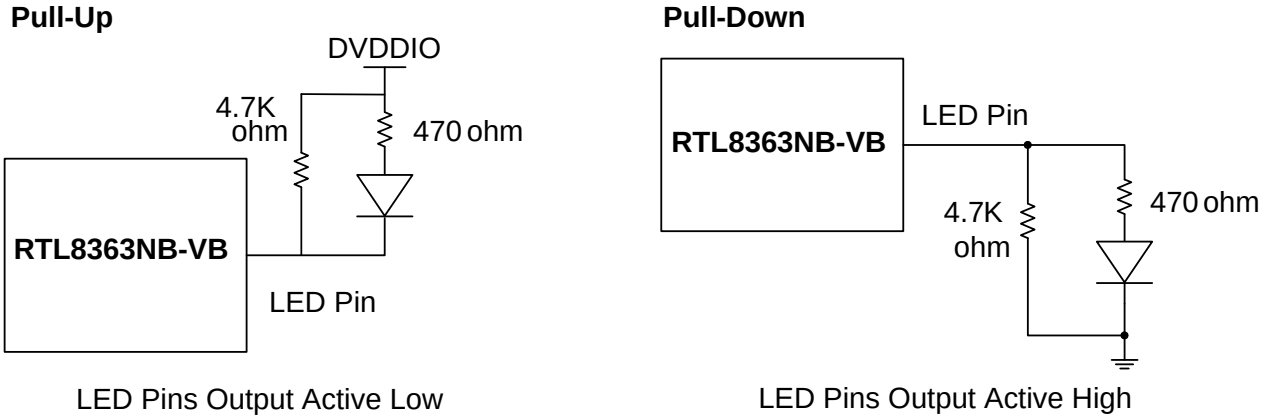


Figure 6. Pull-Up and Pull-Down of LED Pins for Single-Color LED

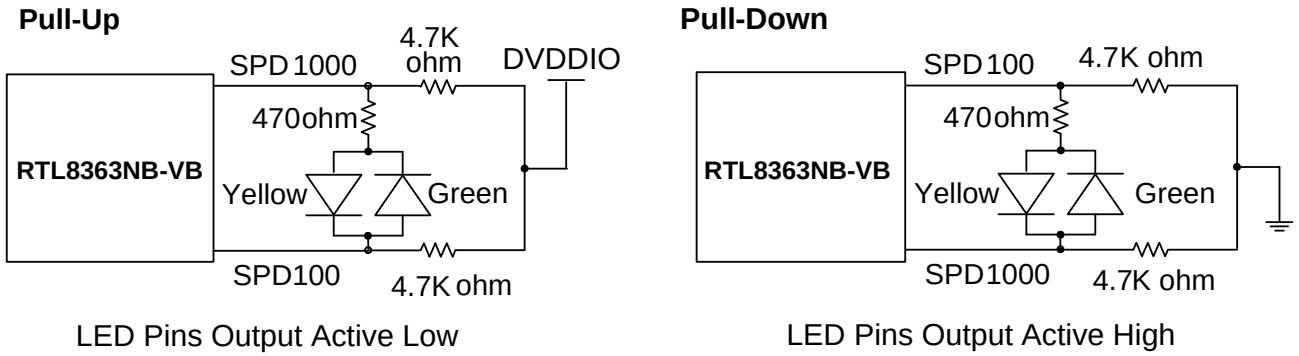


Figure 7. Pull-Up and Pull-Down of LED Pins for Bi-Color LED

8.18. Green Ethernet

8.18.1. Link-On and Cable Length Power Saving

The RTL8363NB-VB provides link-on and dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

8.18.2. Link-Down Power Saving

The RTL8363NB-VB implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected. After it detects an incoming signal, it wakes up from link-down power saving and operates in normal mode.

8.19. IEEE 802.3az Energy Efficient Ethernet (EEE) Function

The RTL8363NB-VB supports IEEE 802.3az Energy Efficient Ethernet ability for 1000Base-T and 100Base-TX in full duplex operation.

The Energy Efficient Ethernet (EEE) optional operational mode combines the IEEE 802.3 Media Access Control (MAC) sub-layer with 100Base-TX and 1000Base-T Physical Layers defined to support operation in Low Power Idle mode. When Low Power Idle mode is enabled, systems on both sides of the link can disable portions of the functionality and save power during periods of low link utilization.

- For 1000Base-T PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle
- For 100Base-TX PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle

The RTL8363NB-VB MAC uses Low Power Idle signaling to indicate to the PHY, and to the link partner, that a break in the data stream is expected, and components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it informs the LPI Client that the link partner has sent such an indication.

8.20. Interrupt Pin for External CPU

The RTL8363NB-VB provides one Interrupt output pin to interrupt an external CPU. The polarity of the Interrupt output pin can be configured via register access. In configuration registers, each port has link-up and link-down interrupt flags with mask.

When port link-up or link-down interrupt mask is enabled, the RTL8363NB-VB will raise the interrupt signal to alarm the external CPU. The CPU can read the interrupt flag to determine which port has changed to which status.

8.21. Regulator

The RTL8363NB-VB embeds a 3.3V-1.1V switch regulator to simplify the power solution. The 1.1V output power is used for the digital core and analog circuits. Do not use the regulator for other chips, even if the rating is enough.

9. Interface Descriptions

9.1. I²C Master for EEPROM Auto-load

The EEPROM interface of the RTL8363NB-VB uses the serial bus I²C to read the Serial EEPROM. When the RTL8363NB-VB is powered up, it drives SCK and SDA to read the configuration/code data from the EEPROM by strapping configuration.

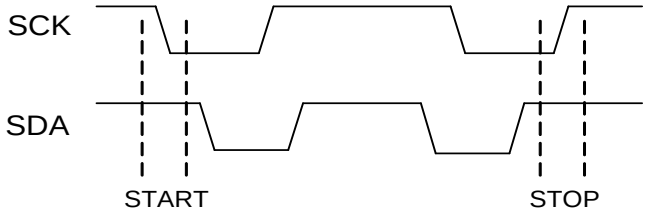


Figure 8. I2C Start and Stop Command

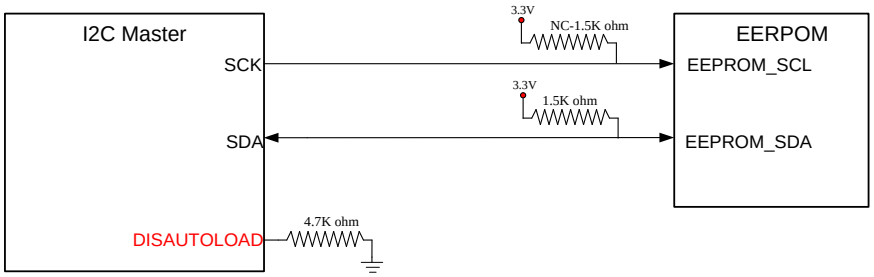


Figure 9. I2C Master for EEPROM Auto-load Interface Connection Example

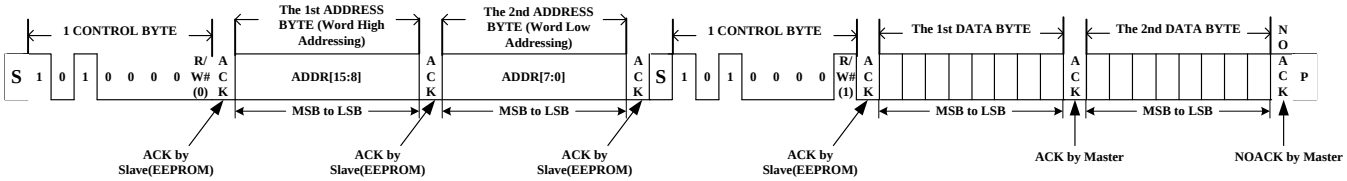


Figure 10. 16-Bit EEPROM Sequential Read

9.2. Realtek I²C-Like Slave Interface for External CPU to Access RTL8364NB-VB

When EEPROM auto-load is complete, the RTL8364NB-VB registers can be accessed through SCK and SDA via an external CPU. The device address of the RTL8364NB-VB is 0x4. For the start and end of a write/read command, SCK needs one extra clock before/after the start/stop signals.

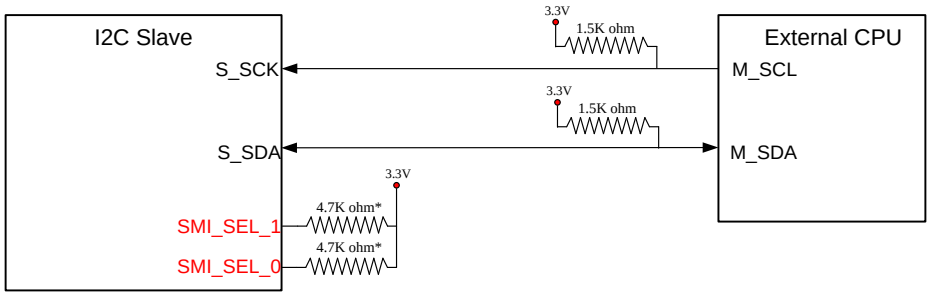


Figure 11. Realtek I2C-Like Slave for External CPU Access Interface Connection Example

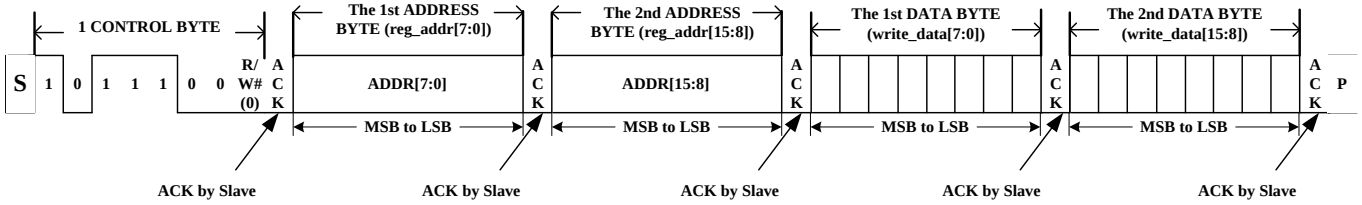


Figure 12. Realtek I2C-Like Slave Interface Write Command

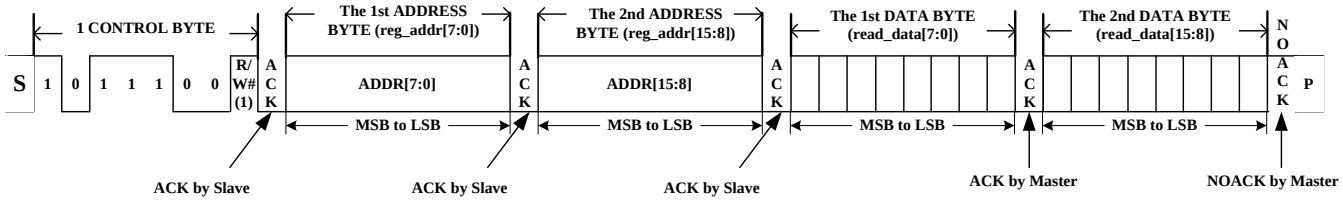


Figure 13. Realtek I2C-Like Slave Interface Read Command

9.3. LSB I²C Slave Interface for External CPU to Access RTL8364NB-VB

When EEPROM auto-load is complete, the RTL8364NB-VB registers can be accessed through SCK and SDA via an external CPU. The device address of the RTL8364NB-VB is 0x4. For the start and end of a write/read command, SCK needs one extra clock before/after the start/stop signals.

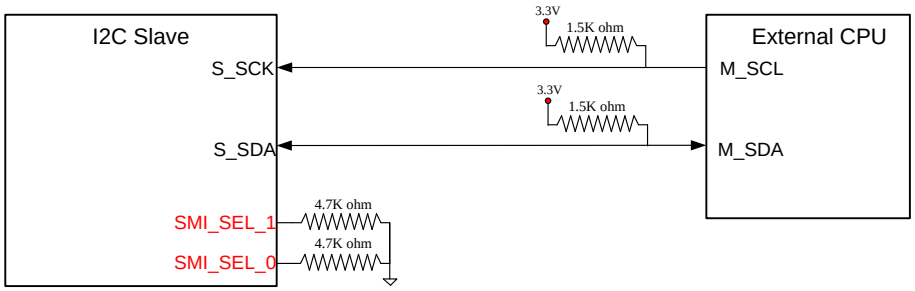


Figure 14. LSB I2C-like Slave for External CPU Access Interface Connection Example

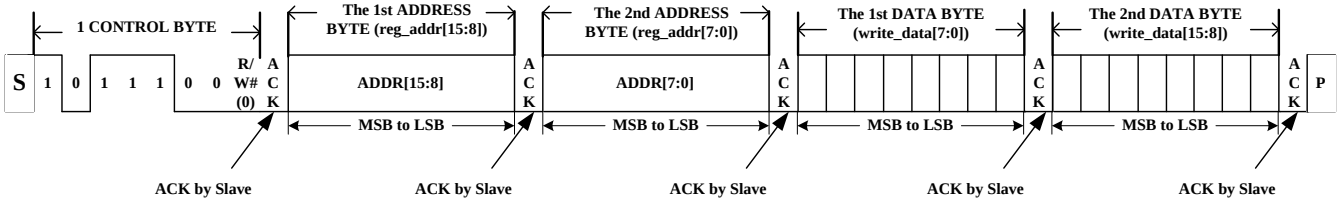


Figure 15. LSB I2C-like Slave Interface Write Command

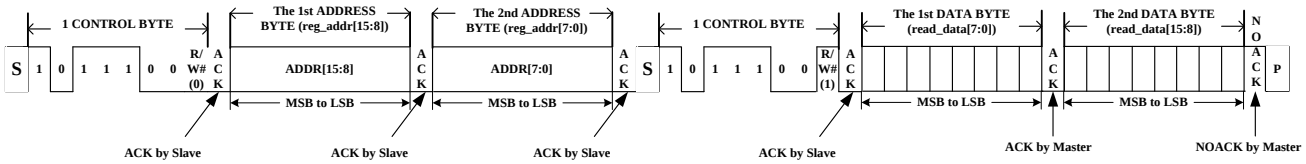


Figure 16. LSB I2C-like Slave Interface Read Command

9.4. MSB I²C-like Slave Interface for External CPU to Access RTL8364NB-VB

When EEPROM auto-load is complete, the RTL8364NB-VB registers can be accessed through SCK and SDA via an external CPU. The device address of the RTL8364NB-VB is 0x4. For the start and end of a write/read command, SCK needs one extra clock before/after the start/stop signals.

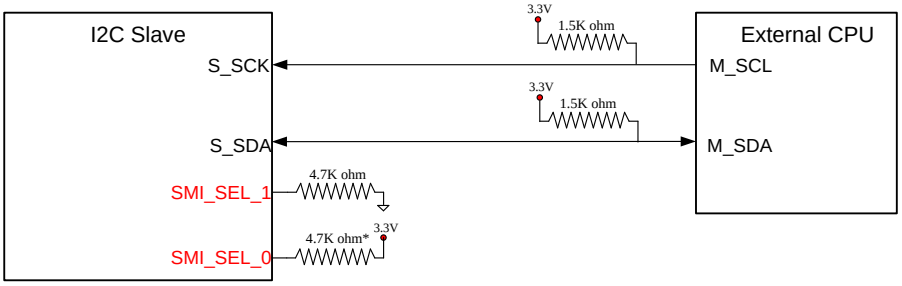


Figure 17. MSB I2C-like Slave for External CPU Access Interface Connection Example

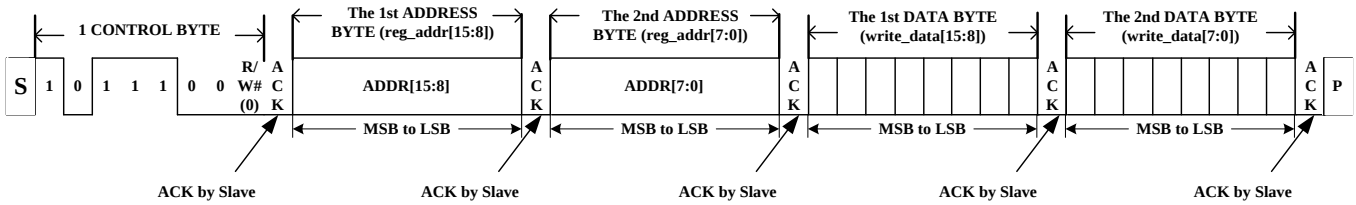


Figure 18. MSB I2C-like Slave Interface Write Command

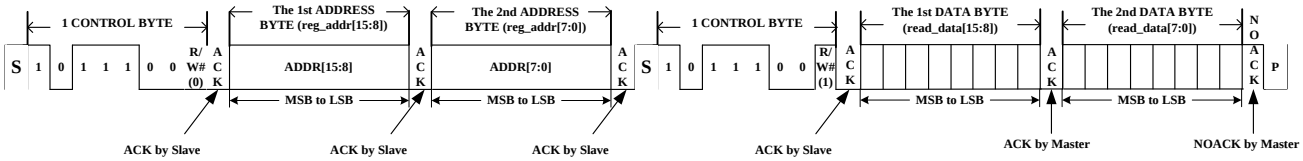


Figure 19. MSB I2C-like Slave Interface Read Command

9.5. Slave MII Management SMI Interface for External CPU to Access RTL8364NB-VB

The RTL8364NB-VB registers can be accessed via Slave MDC and MDIO via an external CPU (Decided by Strapping Configuration).

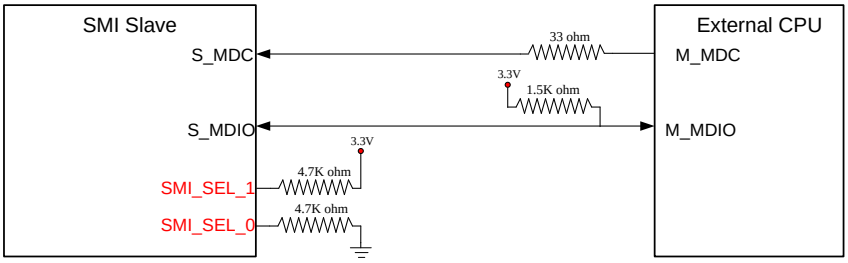


Figure 20. Slave MII Management SMI Interface Connection Example

Table 16. Slave MII Management SMI Access Format

	Management Frame Fields							
	PRE	**ST**	**OP**	**DEVAD**	**REGAD**	**TA**	**DATA**	**IDLE**
Read	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Note: The Slave needs no less than 32bit Preambles (PRE) for accessing slave by Slave SMI interface default. External CPU can configure the Slave to enable preamble suppression function, and then the Slave doesn't need preamble for accessing slave.

9.6. General Purpose Interface

The RTL8363NB-VB supports extension interface. The interface function mux is summarized in Table 17. The Extension GMAC1 of the RTL8363NB-VB supports RGMII, MII MAC mode, or MII PHY mode via register configuration.

Table 17. RTL8363NB-VB Extension Port 1 Pin Definitions

Pin No.	Extension Interface	Type	RGMII	MII MAC Mode	MII PHY Mode
41	E1_CRS	I_{PD}	-	M1M_CRS	-
42	E1_DO3	O	RG1_TXD3	M1M_TXD3	M1P_RXD3
43	E1_DO2	O	RG1_TXD2	M1M_TXD2	M1P_RXD2
44	E1_DO1	O	RG1_TXD1	M1M_TXD1	M1P_RXD1
45	E1_DO0	O	RG1_TXD0	M1M_TXD0	M1P_RXD0
46	E1_DOEN	O	RG1_TXCTL	M1M_TXEN	M1P_RXDV
47	E1_DOCLK	I/O	RG1_TXCLK	M1M_TXCLK	M1P_RXCLK
48	E1_DICLK	I/O	RG1_RXCLK	M1M_RXCLK	M1P_TXCLK
49	E1_DIDV	I	RG1_RXCTL	M1M_RXDV	M1P_TXEN
50	E1_DI0	I	RG1_RXD0	M1M_RXD0	M1P_TXD0
51	E1_DI1	I	RG1_RXD1	M1M_RXD1	M1P_TXD1

Pin No.	Extension Interface	Type	RGMII	MII MAC Mode	MII PHY Mode
52	E1_DI2	I	RG1_RXD2	M1M_RXD2	M1P_TXD2
53	E1_DI3	I	RG1_RXD3	M1M_RXD3	M1P_TXD3

9.6.1. Extension Ports RGMII Mode (1Gbps)

The Extension GMAC1 of the RTL8363NB-VB supports RGMII interface connection to an external CPU. The pin numbers and names are shown in Table 18. Figure 21 shows the signal diagram for Extension Port 1 in RGMII interface.

Table 18. Extension GMAC1 RGMII Pins

RTL8363NB-VB Pin No.	Type	Extension Port 1 RGMII
42, 43, 44, 45	O	RG1_TXD[3:0]
46	O	RG1_TXCTL
47	O	RG1_TXCLK
48	I	RG1_RXCLK
49	I	RG1_RXCTL
50, 51, 52, 53	I	RG1_RXD[0:3]

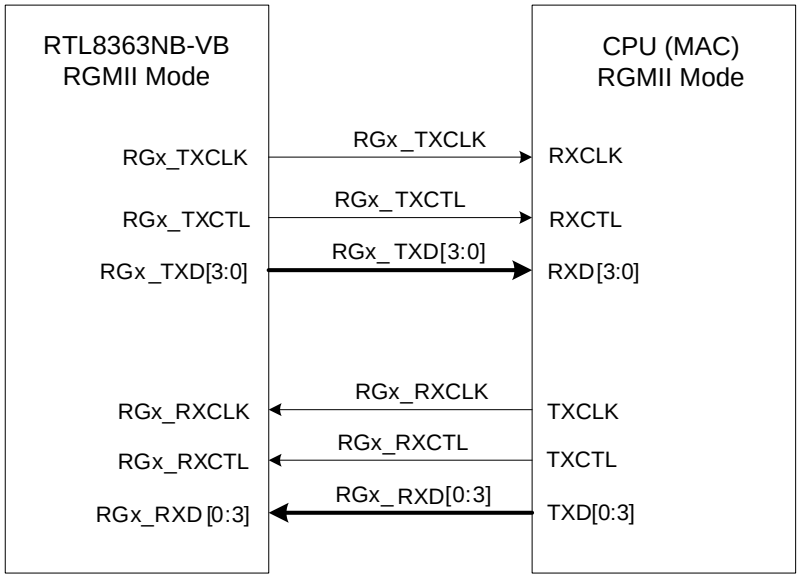


Figure 21. RGMII Mode Interface Signal Diagram

9.6.2. Extension Ports MII MAC/PHY Mode Interface (10/100Mbps)

The Extension GMAC1 of the RTL8363NB-VB supports MII MAC/PHY mode interface connection to an external CPU. The pin numbers and names are shown in Table 19.

Figure 22, page 43, shows the signal diagram for the MII PHY mode interface. Figure 23, page 44, shows the signal diagram for the MAC mode interface.

Table 19. Extension GMAC1 MII Pins

RTL8363NB-VB Pin No.	Type	Extension Port 1 MII MAC Mode	Type	Extension Port 1 MII PHY Mode
41	I_{PD}	M1M_CRS	-	-
42, 43, 44, 45	O	M1M_TXD[3:0]	O	M1P_RXD[3:0]
46	O	M1M_TXEN	O	M1P_RXDV
47	I	M1M_TXCLK	O	M1P_RXCLK
48	I	M1M_RXCLK	O	M1P_TXCLK
49	I	M1M_RXDV	I	M1P_TXEN
50, 51, 52, 53	I	M1M_RXD[0:3]	I	M1P_TXD[0:3]

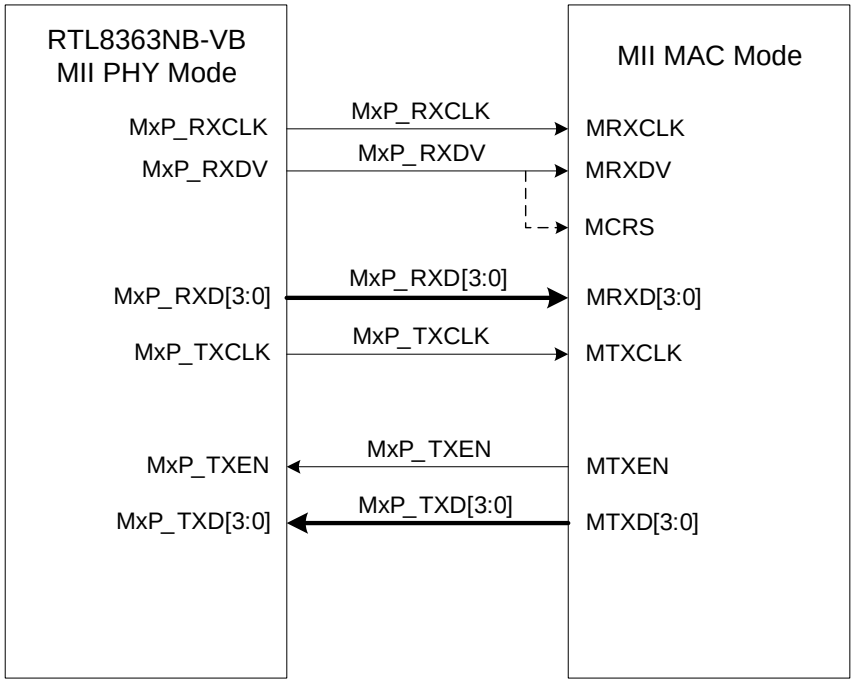


Figure 22. MII PHY Mode Interface (100Mbps) Signal Diagram

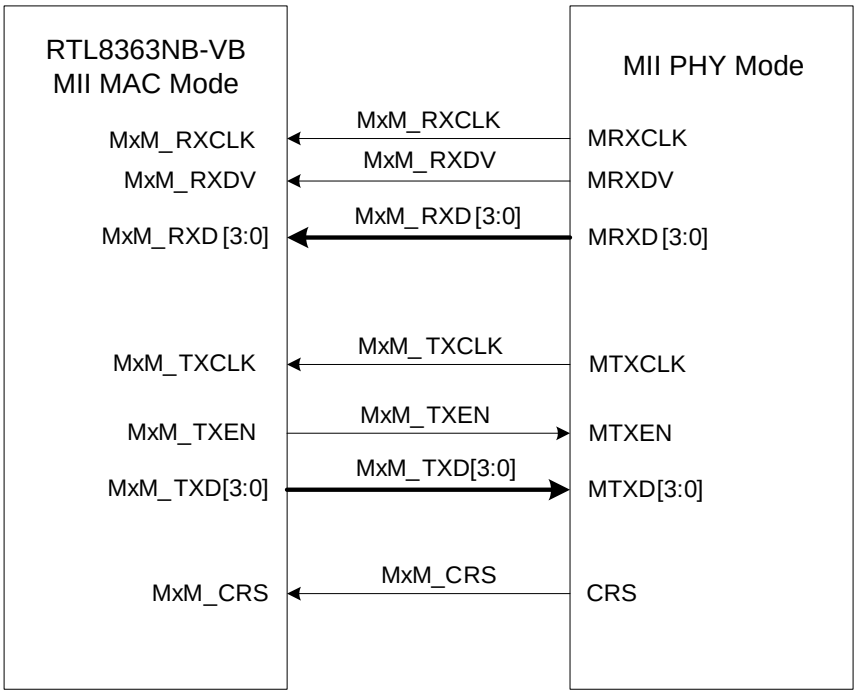


Figure 23. MII MAC Mode Interface (100Mbps) Signal Diagram

10. Electrical Characteristics

10.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 20. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature (Tj)	-	+125	°C
Storage Temperature	-45	+125	°C
DVDDIO, DVDDIO_1, AVDDH, HV_SWR Supply Referenced to GND, AGND and GND_SWR	GND-0.3	+3.63	V
DVDDL, AVDDL, PLLVDDL Supply Referenced to GND, AGND and GND_SWR	GND-0.3	+1.21	V
Digital Input Voltage	GND-0.3	VDDIO+0.3	V

10.2. Recommended Operating Range

Table 21. Recommended Operating Range

Parameter		Min	Typical	Max	Units
Ambient Operating Temperature (Ta)		0	-	70	°C
AVDDH, HV_SWR Supply Voltage Range		3.135	3.3	3.465	V
DVDDIO Supply Voltage Range	3.3V	3.135	3.3	3.465	V
	2.5V	2.375	2.5	2.626	V
	1.8V	1.710	1.8	1.890	
DVDDIO_1 Supply Voltage Range (DVDDIO_1: Extension Port 1 Supports 1.8V, 2.5V, or 3.3V)	3.3V	3.135	3.3	3.465	V
	2.5V	2.375	2.5	2.626	V
	1.8V	1.710	1.8	1.890	V
DVDDL, AVDDL, PLLVDDL Supply Voltage Range		1.045	1.1	1.155	V

10.3. Thermal Characteristics

10.3.1. Assembly Description

Table 22. Assembly Description

Package	Type	QFN-76
	Dimension (L×W)	9×9 mm^2
	Thickness	0.65 mm
PCB	PCB Dimension (L×W)	80×70 mm^2
	PCB Thickness	1.6 mm
	Number of Cu Layer-PCB	80×82 mm (4-Layer)

10.3.2. Material Properties

Table 23. Material Properties

Item		**Material**	**Thermal Conductivity K (W/m-k)**
Package	Die	Si	147
	Silver Paste	1033BF	2.5
	Lead Frame	CDA7025	168
	Mold Compound	7372	0.9
PCB		Cu	400
		FR4	0.2

10.3.3. Simulation Conditions

Table 24. Simulation Conditions

Input Power	1.0W
Test Board (PCB)	4L (2S2P)
Control Condition	Air Flow = 0 m/s

10.3.4. Thermal Performance of QFN-76 on PCB Under Still Air Convection

Table 25. Thermal Performance of QFN-76 on PCB Under Still Air Convection

	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JB}
4L PCB	25.8	9.9	5.1	4.7

Note:
θ_{JA}: Junction to ambient thermal resistance
θ_{JB}: Junction to board thermal resistance
θ_{JC}: Junction to case thermal resistance
Ψ_{JB}: Junction to bottom surface center of PCB thermal characterization

10.4. DC Characteristics

Table 26. DC Characteristics

Parameter	SYM	Min	Typical	Max	Units
System Idle (All UTP Ports Link Down, and 1 Extension Port is Configured as RGMII, without LEDs)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}	-	12	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, $I_{PLLVDDL}$	-	141	-	mA
1000M Active (All UTP Ports Link/Active, and 1 Extension Port is Configured as RGMII, without LEDs)					
Power Supply Current for VDDH	$I_{DVDDIO,}$ I_{AVDDH}	-	133	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, $I_{PLLVDDL}$	-	241	-	mA
Power Supply Current for RGMII1 DVDDIO_1 (3.3V)	I_{DVDDIO_1}	-	42	-	mA
Power Supply Current for RGMII1 DVDDIO_1 (2.5V)	I_{DVDDIO_1}	-	30	-	mA
Power Supply Current for RGMII1 DVDDIO_1 (1.8V)	I_{DVDDIO_1}	-	17	-	mA
VDDIO=3.3V					
TTL Input High Voltage	V_{ih}	2.0	-	-	V
TTL Input Low Voltage	V_{il}	-	-	0.7	V
Output High Voltage	V_{oh}	2.7	-	-	V
Output Low Voltage	V_{ol}	-	-	0.6	V
VDDIO=2.5V					
TTL Input High Voltage	V_{ih}	1.7	-	-	V
TTL Input Low Voltage	V_{il}	-	-	0.6	V
Output High Voltage	V_{oh}	2.25	-	-	V
Output Low Voltage	V_{ol}	-	-	0.4	V
VDDIO=1.8V					
TTL Input High Voltage	V_{ih}	1.2	-	-	V
TTL Input Low Voltage	V_{il}	-	-	0.6	V
Output High Voltage	V_{oh}	1.45	-	-	V
Output Low Voltage	V_{ol}	-	-	0.4	V

Note 1: DVDDIO=3.3V, AVDDH=3.3V, DVDDIO_1=3.3V, DVDDL=1.1V, AVDDL=1.1V, and PLLVDDL=1.1V.
Note 2: I_{DVDDIO_1} should be added to the total current consumption when the extension port of the RTL8363NB-VB is used.

10.5. Switch Regulator

Table 27. Switch Regulator

Symbol	Parameter	Min.	Typ.	Max.	Units
F_{SW}	Oscillator Frequency	-	2	-	MHz
T_{SS}	Soft-Start Time	-	1.5	-	ms

10.6. AC Characteristics

10.6.1. I²C Master for EEPROM Auto-load Interface Timing Characteristics

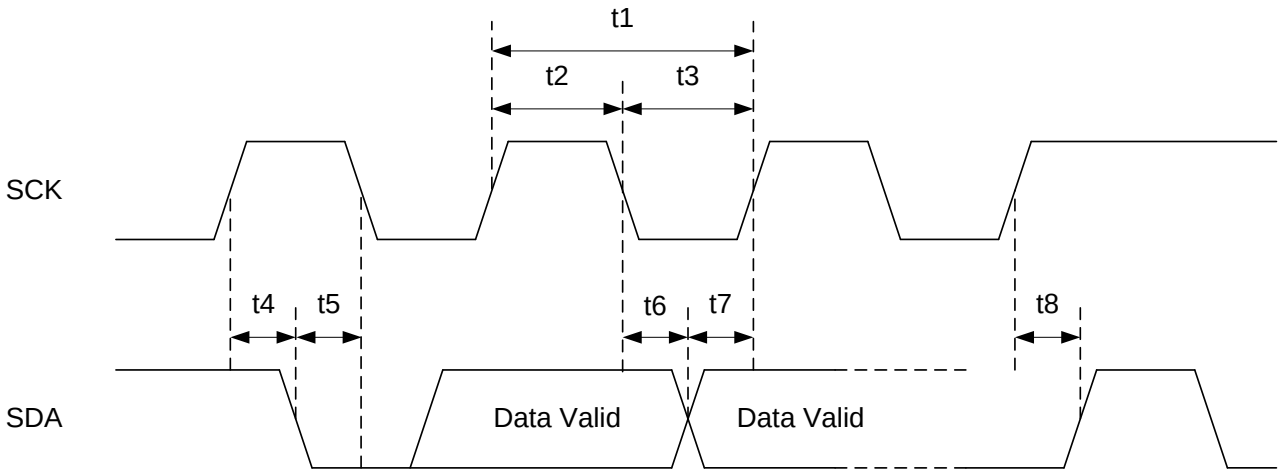


Figure 24. Master I2C for EEPROM Auto-load Timing Characteristics

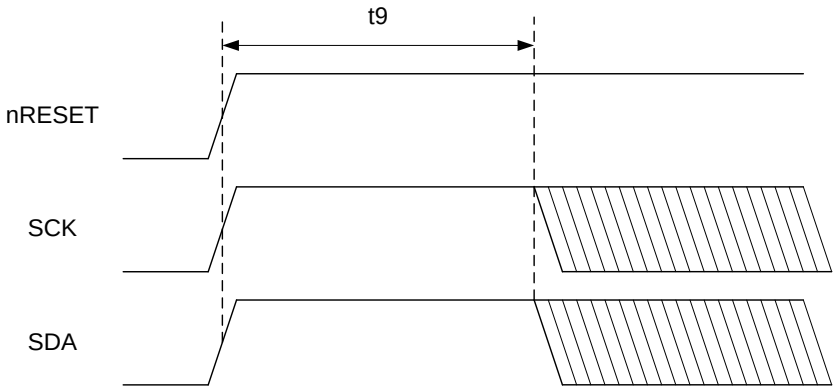


Figure 25. SCK/SDA Power on Timing

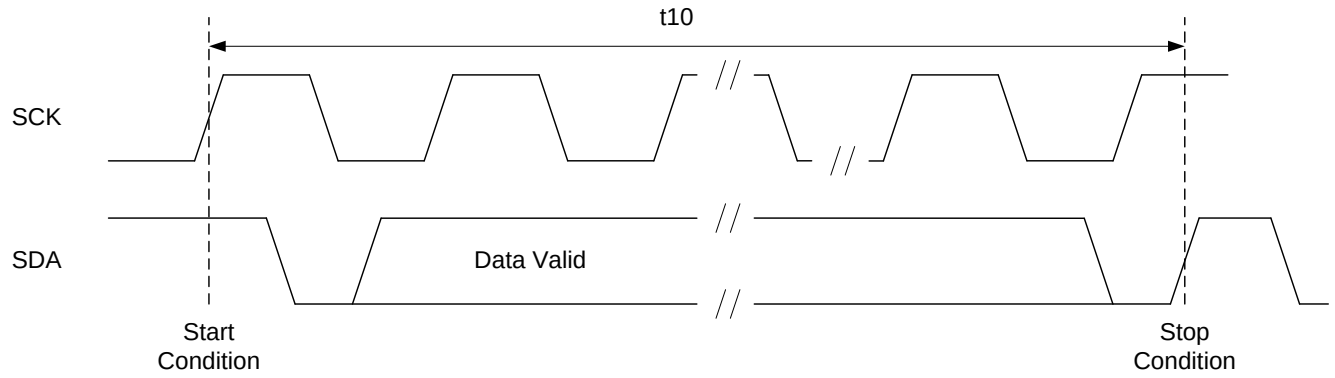


Figure 26. EEPROM Auto-Load Timing

Table 28. Master I2C for EEPROM Auto-load Timing Characteristics

Symbol	Description	Type	Min	Typical	Max	Units
t1	SCK Clock Period	O	9.7	10	-	µs
t2	SCK High Time	O	4.2	5	-	µs
t3	SCK Low Time	O	4.2	5	-	µs
t4	START Condition Setup Time	O	4.8	5.04	-	µs
t5	START Condition Hold Time	O	4.8	4.96	-	µs
t6	Data Hold Time	O	2.2	2.52	-	µs
t7	Data Setup Time	O	2.2	2.48	-	µs
t8	STOP Condition Setup Time	O	4.4	5.04	-	µs
t9	SCK/SDA Active from Reset Ready	O	75	78.4	-	ms
-	SCK Rise Time (10% to 90%)	O	-	320	-	ns
-	SCK Fall Time (90% to 10%)	O	-	320	-	ns
-	Duty Cycle	O	48.86	50	51.14	%

10.6.2. Realtek I²C-like Slave Mode Timing Characteristics

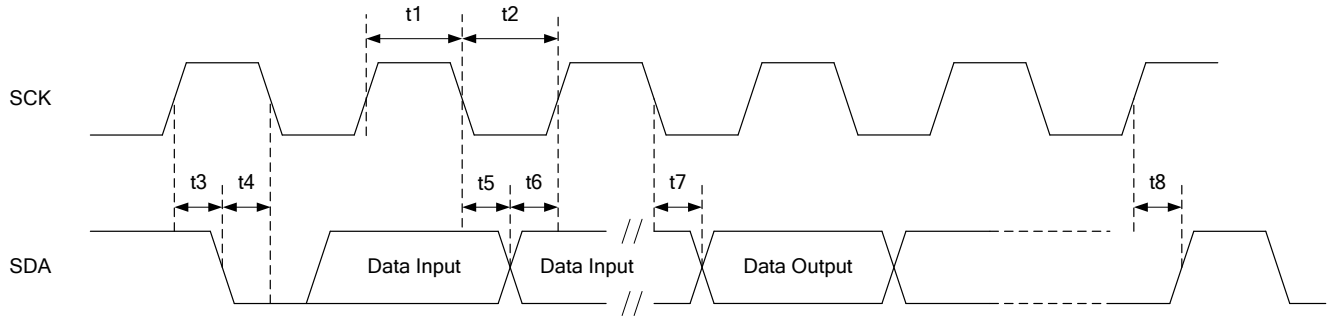


Figure 27. Realtek I2C-like Slave Mode Timing Characteristics

Table 29. Realtek I2C-like Slave Mode Timing Characteristics

Symbol	Description	Type	Min	Typical	Max	Units
t1	SCK High Time	I	250	-	-	ns

Symbol	Description	Type	Min	Typical	Max	Units
t2	SCK Low Time	I	250	-	-	ns
t3	START Condition Setup Time	I	150	-	-	ns
t4	START Condition Hold Time	I	150	-	-	ns
t5	Data Hold Time	I	150	-	-	ns
t6	Data Setup Time	I	150	-	-	ns
t7	Clock to Data Output Delay	O	-	100	-	ns
t8	STOP Condition Setup Time	I	150	-	-	ns

10.6.3. Slave MII Management SMI for External CPU Access Interface Timing Characteristics

The RTL8363NB-VB supports MDIO slave mode. The Master (CPU) can access the Slave (RTL8363NB-VB) registers via the MDIO interface. The MDIO is a bi-directional signal that can be sourced by the Master or the Slave. In a write command, the master sources the MDIO signal. In a read command, the slave sources the MDIO signal.

- The timing characteristics t1, t2, and t3 (Table 30) of the Master (the RTL8363NB-VB link partner CPU) are provided by the Master when the Master sources the MDIO signal (Write command)
- The timing characteristics t4 (Table 30) of the Slave (RTL8363NB-VB) are provided by the RTL8363NB-VB when the RTL8363NB-VB sources the MDIO signal (Read command)

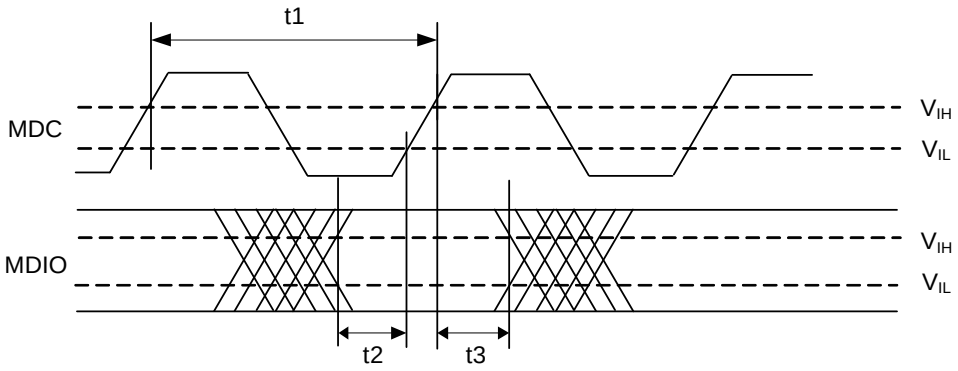


Figure 28. MDIO Sourced by the Master

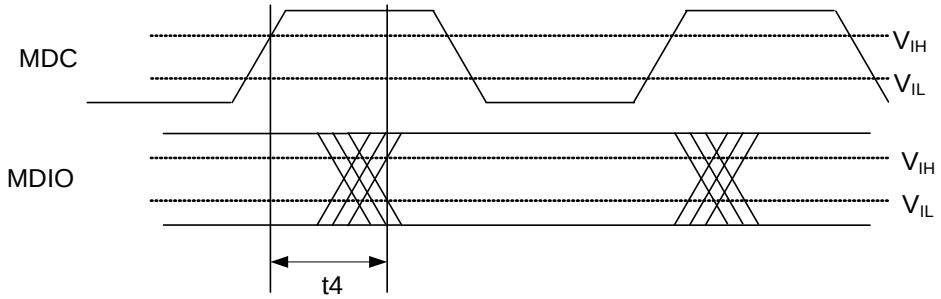


Figure 29. MDIO Sourced by the RTL8363NB-VB (Slave)

Table 30. MDIO Timing Characteristics and Requirement

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
MDC Clock Period	t1	Clock Period	I	125	-	-	ns
MDIO to MDC Rising Setup Time (Write Data)	t2	Input Setup Time	I	25	-	-	ns
MDIO to MDC Rising Hold Time (Write Data)	t3	Input Hold Time	I	25	-	-	ns
MDC to MDIO Delay Time (Read Data)	t4	Clock (Rising Edge) to Data Delay Time	O	0	-	80	ns

10.6.4. MII MAC Mode Timing

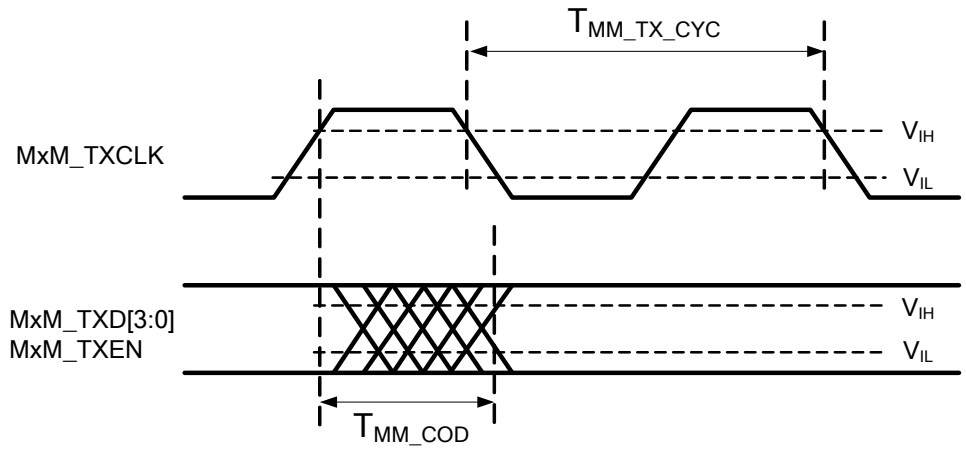


Figure 30. MII MAC Mode Clock to Data Output Delay Timing

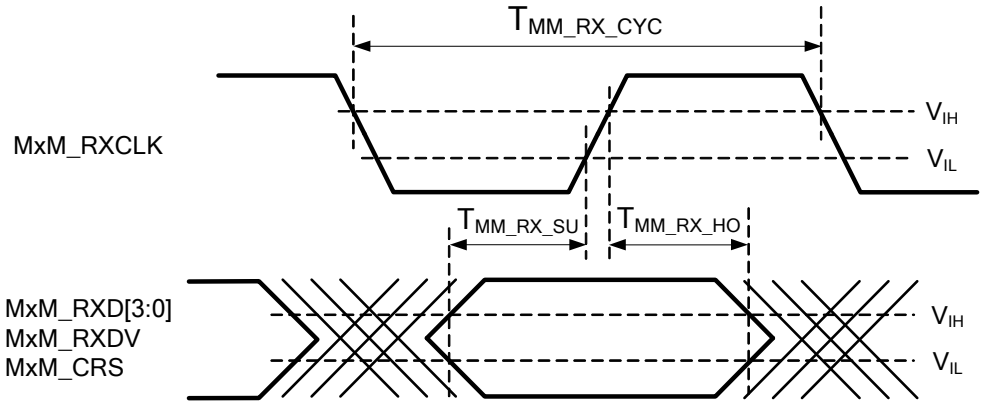


Figure 31. MII MAC Mode Input Timing

Table 31. MII MAC Mode Timing

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
100Base-TX MxM_TXCLK and MxM_RXCLK Input Cycle Time	$T_{MM\_TX\_CYC}$ $T_{MM\_RX\_CYC}$	25MHz Clock Input.	I	-	40	-	ns
10Base-T MxM_TXCLK and MxM_RXCLK Input Cycle Time	$T_{MM\_TX\_CYC}$ $T_{MM\_RX\_CYC}$	2.5MHz Clock Input.	I	-	400	-	ns
MxM_TXCLK to MxM_TXD[3:0] and MxM_TXEN Output Delay Time	T_{MM_COD}	-	O	3	5	7	ns
MxM_RXD[3:0], MxM_RXDV, and MxM_CRS Input Setup Time	$T_{MM\_RX\_SU}$	-	I	10	-	-	ns
MxM_RXD[3:0], MxM_RXDV, and MxM_CRS Input Hold Time	$T_{MM\_RX\_HO}$	-	I	10	-	-	ns

10.6.5. MII PHY Mode Timing

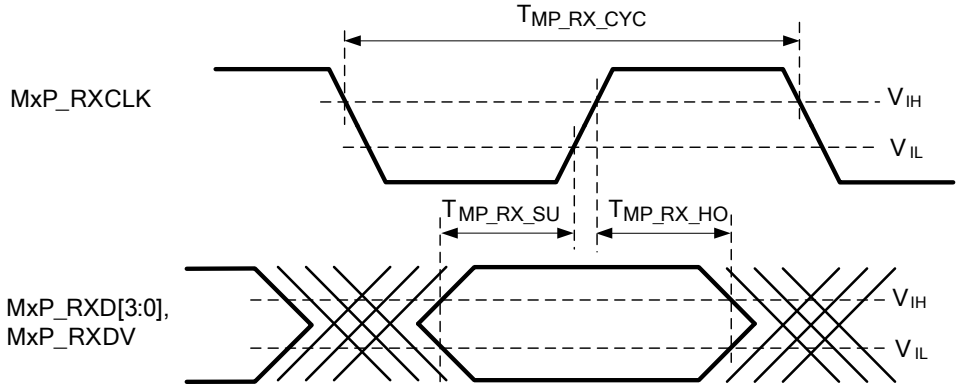


Figure 32. MII PHY Mode Output Timing

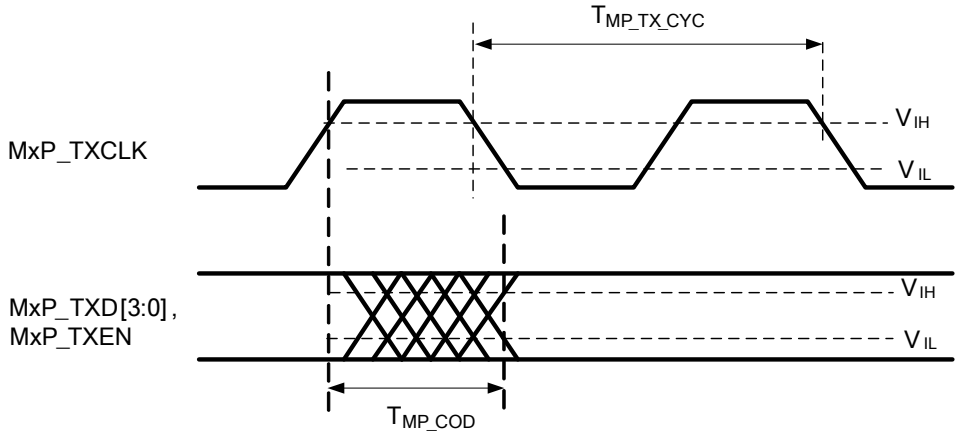


Figure 33. MII PHY Mode Clock Output to Data Input Delay Timing

Table 32. MII PHY Mode Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
100M MxP_RXCLK and MxP_TXCLK Output Cycle Time	$T_{MP\_RX\_CYC}$ $T_{MP\_TX\_CYC}$	25MHz Clock Output.	O	-	40	-	ns
10M MxP_RXCLK and MxP_TXCLK Output Cycle Time	$T_{MP\_RX\_CYC}$ $T_{MP\_TX\_CYC}$	2.5MHz Clock Output.	O	-	400	-	ns
100M MxP_RXD[3:0] and MxP_RXDV to MxP_RXCLK Output Setup Time	$T_{MP\_RX\_SU}$	-	O	14	18	-	ns
100M MxP_RXD[3:0] and MxP_RXDV to MxP_RXCLK Output Hold Time	$T_{MP\_RX\_HO}$	-	O	16	19.5	-	ns
100M MxP_TXCLK Clock Output to MxP_TXD[3:0] and MxP_TXEN Input Delay Time	T_{MP_COD}	-	I	0	-	25	ns

10.6.6. RGMII Timing Characteristics

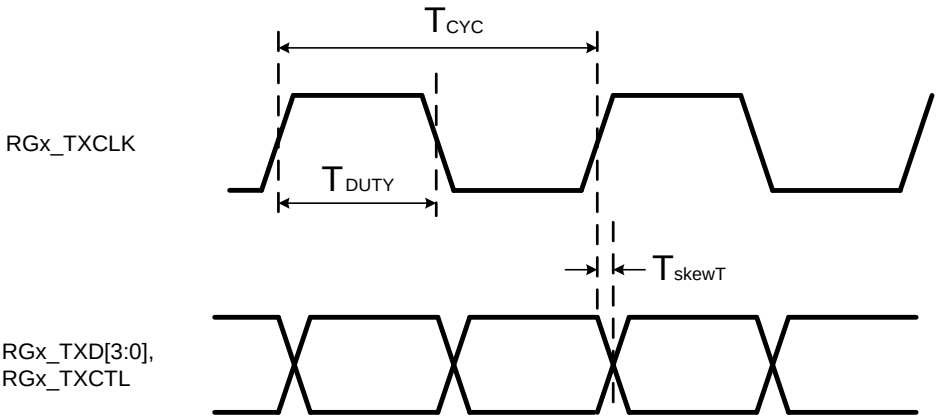


Figure 34. RGMII Output Timing Characteristics (RGx_TXCLK_DELAY=0)

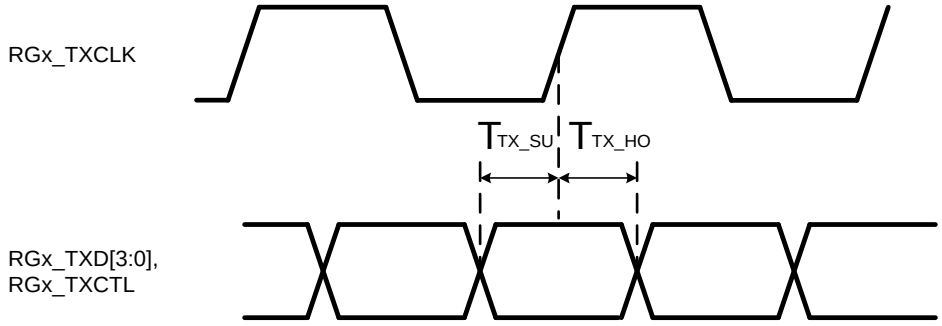


Figure 35. RGMII Output Timing Characteristics (RGx_TXCLK_DELAY=2ns)

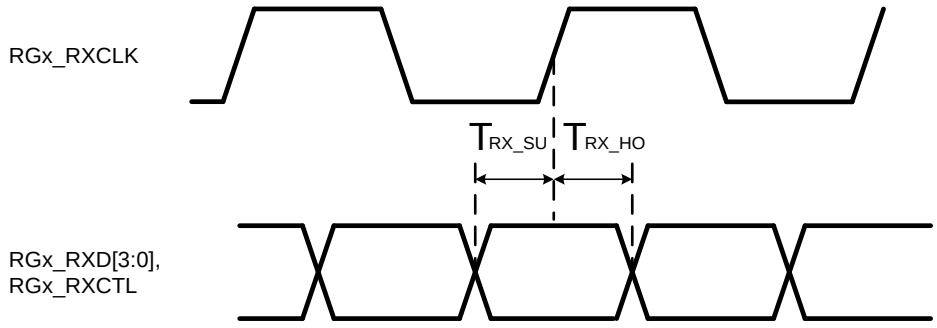


Figure 36. RGMII Input Timing Characteristics (RGx_RXCLK_DELAY=0)

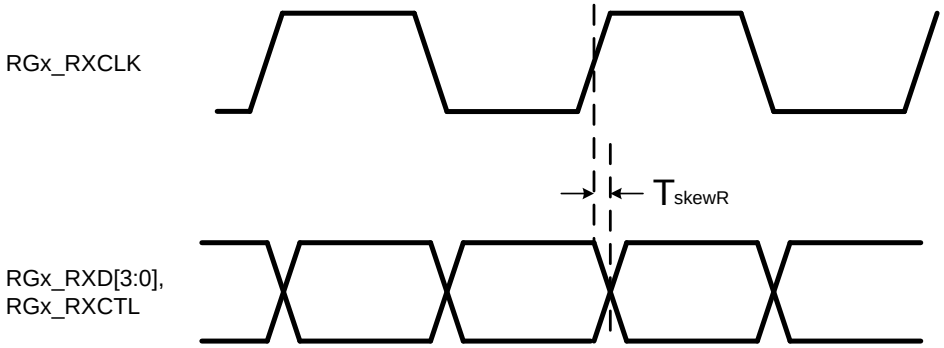


Figure 37. RGMII Input Timing Characteristics (RGx_RXCLK_DELAY=2ns)

Table 33. RGMII Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
1000M RGx_TXCLKc Output Cycle Time	T_{TX_CYC}	125MHz Clock Output. Refer to Figure 34, page 54.	O	7.6	8	8.6	ns
100M RGx_TXCLK Output Cycle Time	T_{TX_CYC}	25MHz Clock Output. Refer to Figure 34, page 54.	O	38	40	42	ns
10M RGx_TXCLK Output Cycle Time	T_{TX_CYC}	2.5MHz Clock Output. Refer to Figure 34, page 54.	O	380	400	420	ns
RGx_TXD[3:0] and RGx_TXCTL to RGx_TXCLK Output Skew	T_{skewT}	Disable Output Clock Delay. (RGx_TXCLK_DELAY=0). Refer to Figure 34, page 54.	O	-500	-	500	ps
RGx_TXD[3:0] and RGx_TXCTL to RGx_TXCLK Output Setup Time	T_{TX_SU}	Enable Output Clock Delay. (RGx_TXCLK_DELAY=1). Refer to Figure 35, page 54.	O	1.2	-	-	ns
RGx_TXD[3:0] and RGx_TXCTL to RGx_TXCLK Output Hold Time	T_{TX_HO}	Enable Output Clock Delay. (RGx_TXCLK_DELAY=1). Refer to Figure 35, page 54.	O	1.2	-	-	ns
RGx_RXD[3:0] and RGx_RXCTL to RGx_RXCLK Input Setup Time	T_{RX_SU}	Disable Input Clock Delay. (RGx_RXCLK_DELAY=0). Refer to Figure 36, page 54.	I	1.0	-	-	ns
RGx_RXD[3:0] and RGx_RXCTL to RGx_RXCLK Input Hold Time	T_{RX_HO}	Disable Input Clock Delay. (RGx_RXCLK_DELAY=0). Refer to Figure 36, page 54.	I	1.0	-	-	ns
RGx_RXD[3:0] and RGx_RXCTL to RGx_RXCLK Input Skew	T_{skewR}	Enable Input Clock Delay. (RGx_RXCLK_DELAY=1). Refer to Figure 37, page 55.	I	-600	-	600	ps

10.7. Power and Reset Characteristics

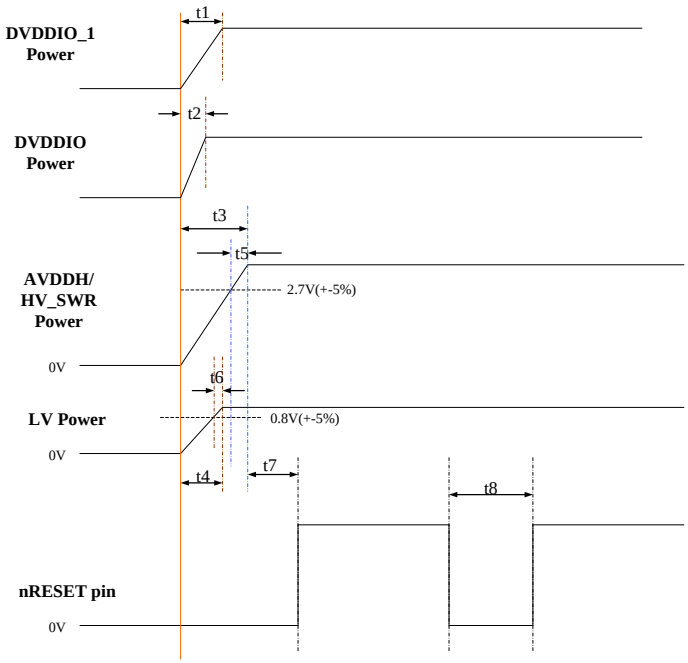


Figure 38. Power and Reset Characteristics

Table 34. Power and Reset Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
DVDDIO_1 Rising Time	t1	DVDDIO_1 power rise settling time	I	0.5	-	-	ms
DVDDIO Rising Time	t2	DVDDIO power rise settling time	I	0.5	-	-	ms
HV Power Rising Time	t3	AVDDH, HV_SWR(If embedded SWR be used) power rise settling time	I	0.5	-	-	ms
LV Power Rising Time	t4	DVDDL and AVDDL power rise settling time	I	0.5	-	-	ms
HV Power Ready Time after more than HV POR threshold	t5	The duration from HV power more than HV POR threshold to HV power ready	I	-	-	10	ms
LV Power Ready Time after more than LV POR threshold	t6	The duration from LV power more than LV POR threshold to LV power ready	I	-	-	10	ms
Reset Delay Time	t7	The duration from ‘all power steady’ to the reset signal released to high	I	10	-	-	ms
Reset Low Time	t8	The duration of reset signal remaining low time before issuing a reset to RTL8363NB-VB	I	10	-	-	ms

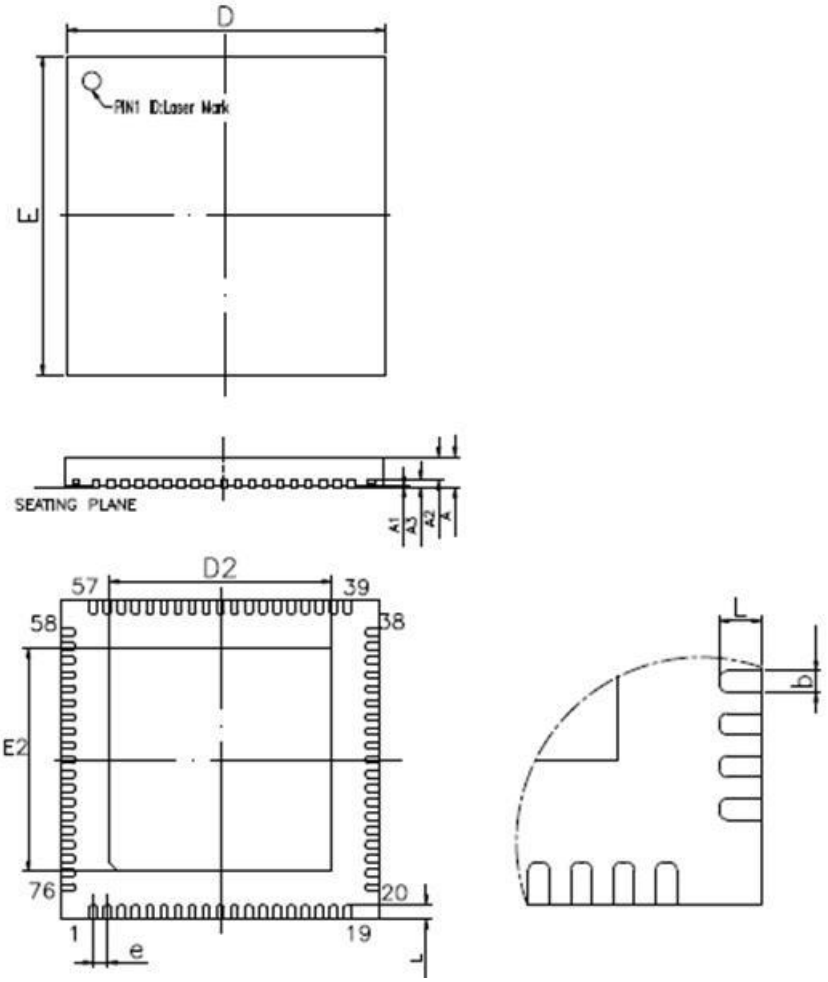
Note:

1) If the powers supply voltage of the RTL8363NB-VB lower than normal operation condition happened, the Power On Reset (POR) or Pin Reset be needed for normal operation of the RTL8363NB-VB.

2) AVDDH power must be ready no later than HV_SWR power.

11. Mechanical Dimensions

Low Profile Plastic Quad Flat Package 76 Leads 9×9mm Outline



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	-	0.65	0.70	-	0.026	0.028
A_3	0.2 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	9.00 BSC			0.354 BSC		
D_2/E_2	6.05	6.30	6.55	0.238	0.248	0.258
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

12. Ordering Information

Table 35. Ordering Information

Part Number	Package	Status
RTL8363NB-VB-CG	QFN 76-Pin ‘Green’ Package	-

Note: See page 7 for package identification.

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