High Frequency Quasi-Resonant Flyback Converter With GaN Integrated

1 Descriptions

SC3057B is a high frequency, quasi-resonant flyback PWM converter with 700V GaN integrated (QR/DCM), which can achieve high efficiency and reliability. The converter with x-cap discharge function built-in high voltage start-up circuit through HV pin. Therefore, extremely low standby power consumption and super-fast start-up time can be obtained by HV pin.

SC3057B provides an adaptive switching frequency fold-back to achieve higher efficiency in the whole loading range. It operates in QR and DCM with valley switching for high efficiency. And at no load, the IC will operate in burst mode to reduce power consumption.

SC3057B provides functions of low start-up current, fast start-up, low standby power consumption. The burst mode with extremely low operation current (350uA) can significantly reduce standby power consumption to meet the efficiency regulations.

The converter integrates a segment power supply circuit for VDD power supply, which is especially suitable for applications with wide output voltage range.

SC3057B offers comprehensive protections to prevent the circuit from damage under abnormal conditions.

Furthermore, the features of frequency jittering and smart driving function can minimize the noise and improve EMI performance.

2 Features

- Integrated 700V GaN
- Integrated high-voltage startup circuit with brown in/out detection
- With x-cap discharge function.
- Internal Soft Start
- Integrated segment power supply circuit for extra-wide output range
- Ultra-low operation current @Burst mode/Fault Mode
- Up to 175KHz Switching Frequency
- Frequency Jitter for EMI improvement
- Valley switching operation @QR/DCM
- Burst Mode @ Light Load & No Load
- Internal over temperature protection
- Comprehensive Protection
  - VDD over voltage protection
  - VDD under voltage lock out
  - Cycle by cycle current limiting
  - Two level over current protection
  - Output over voltage protection
  - Output short protection
  - Over Load protection
- QFN6*8 package available

3 Applications

- USB-PD and QC Chargers
- AC-DC adapters for Portable Devices

4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC3057BQDSR	QFN6*8	6.0mm x 8.0mm x 0.9mm

SC3057BQDSR Functional Table

ORDER NUMBER	SC3057B
Maximum Frequency	175kHz
ZCD OVP	A
X-Cap Discharge	Y
OLP	A
Brown In/Out	A
Internal OTP	A

A: Auto-recovery;

/: Without this function;

5 Typical Application Circuit

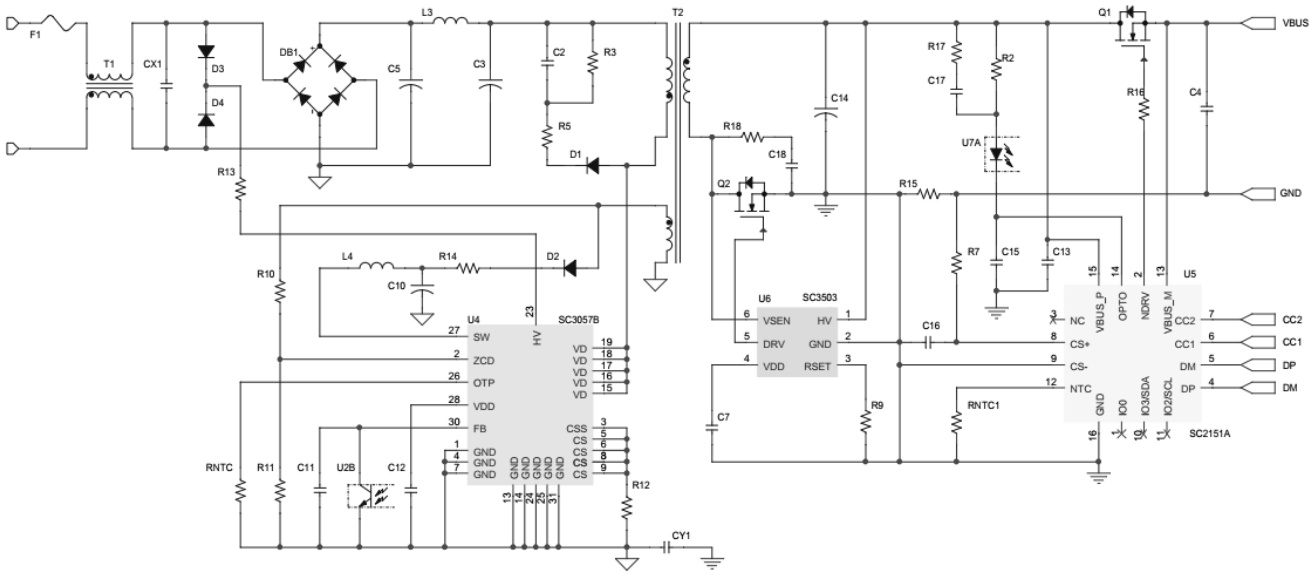


Fig. 1 Typical application circuit

6 Terminal Configuration and Functions

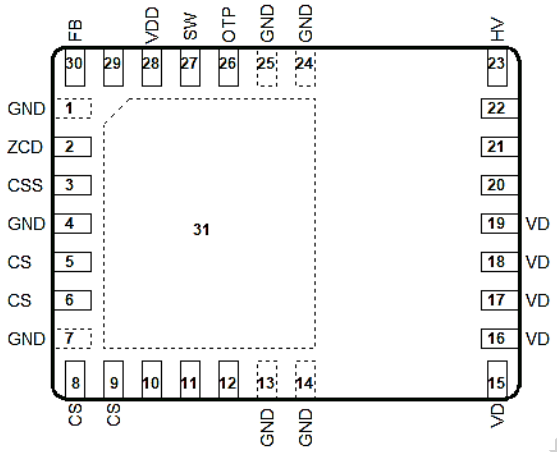


Fig. 2 Top view

TERMINAL		I/O	DESCRIPTION
SC3057B	NAME		
1,4,7,13, 14,24,25,31	GND	PWR	Power Ground.
2	ZCD	I	Output voltage sense. The ZCD voltage is used to detect resonant valleys for quasi-resonant switching. This pin detects the output voltage information and diode current discharge time based on the auxiliary winding voltage.
3	CSS	I	The controller current sense for peak-current-mode control.
5,6,8,9	CS	O	Internal GaN FET source terminal. This pin connects to a current-sense resistor to sense the GaN current.
10,11,12	NC		No connection. These pins are recommended to be connected to GND to increase heat dissipation.
20,21,22	NC		No connection. In order to increase the safety distance, the pads of these pins in the layout are not recommended.
26	OTP	O	External OTP pin. This pin is typically connected to an NTC resistor.
29	NC		No connection.
15,16,17, 18,19	VD	PWR	Internal GaN FET drain terminal.
23	HV	PWR	Connected to the line via resistors and diodes for startup and x-cap discharge, this pin allows the brown in/out detection as well.
27	SW	PWR	Segment power supply circuit control.
28	VDD	PWR	Power Supply.
30	FB	I	Secondary side voltage feedback input pin. Connect to an opto-coupler directly.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

Item	Description	Min.	Typ.	Max.	UNIT
Voltage range at terminals (2)	HV to GND			700	V
	VD, max to GND			700	V
	VD, transient to GND			800	V
	VDD、SW to GND	-0.3		44	V
	Other Pins to GND	-0.3		6.5	V
T_J	Operating Junction temperature range	-40		150	°C
T_{stg}	Storage temperature range	-65		150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Thermal Information

THERMAL RESISTANCE (1)		QFN6*8 (6.0mmx8.0mm)	UNIT
θ_{JA}	Junction to ambient thermal resistance	50	°C/W
θ_{JC}	Junction to case resistance	2.2	°C/W

(1) Measured on JESD51-7, 2-layer PCB.

7.3 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD (1)	Human body model (HBM) ESD stress voltage (2) (HV pin)	-1	+1	kV
	Human body model (HBM) ESD stress voltage (2) (All pins except HV)	-2	+2	kV
	Charged device model (CDM) ESD stress voltage (3)	-1	+1	kV

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operating Conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD to GND	VDD voltage range to GND	10		V_{DDOVP}	V
VD to GND	VD voltage range to GND	0		650	V
C_{VDD}	VDD Capacitor	2.2		22	uF
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C

7.5 Electrical Characteristics

VDD=15V, T_J= -40°C~125°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Hight Voltage Supply and X-cap Discharge (HV)						
I_{HV_VDD1}	HV Start-up current-1	V_{DD} ≤ 0.5V, V_{HV}>150V			1.0	mA
I_{HV_VDD2}	HV Start-up current-2	V_{DD} = V_{DDON} - 0.5V, V_{HV}>150V		2.9		mA
I_{HVLK}	HV pin leakage current after startup	VDD> V_{DDON}, HV = 400V			15	μA
V_{HVBIN}	Brown-in threshold voltage	DC input voltage	97	105	113	V
V_{HVBOUT}	Brown-out threshold voltage	DC input voltage	84	90	96	V
T_{BOUT}	Debounce time of brown out	V_{TH} < V_{TH_BOUT}		64		ms
T_{XDET}	X-Cap discharge Detection Delay time			80		ms
I_{DHGX}	X-Cap discharge current			5		mA
Voltage Supply (VDD)						
V_{DDON}	VDD on threshold voltage		14.2	15.0	15.8	V
V_{DDOFF}	VDD off threshold voltage		7.9	8.4	8.9	V
$V_{DDHOLDL}$	VDD holding entry point voltage			8.9		V
$V_{DDHOLDH}$	VDD holding exit point voltage			9.7		V
$V_{DDBSTOFF}$	Booster regulation voltage			11.2		V
$V_{DDBSTON}$	The booster circuit starts to work			9.7		V
I_{VDD}	Operating current	Fsw=175KHz		1.6		mA
I_{VDDBT}	Burst mode current	V_{FB} < 0.5V		350		μA
$I_{VDDFAULT}$	Hold up current in fault mode			80		μA
T_{DFAULT}	Hold on time in fault mode			2		s
$I_{VDDFAULT1}$	VDD sink current, BO	After T_{DFAULT} 2S		1.6		mA
V_{DDOVP}	VDD OVP			40.0		V
I_{VDDOVP}	VDD OVP sink current	V_{DD} > V_{DDOVP}		5		mA
T_{VDDOVP}	VDD OVP debounce time			160		μs
Zero Voltage Detection (ZCD)						
V_{ZCDOVP}	ZCD OVP		4.27	4.45	4.63	V
N_{ZCDOVP}	ZCD OVP debounce counter			4		cycles
I_{ZCDMAX}	Maximum ZCD Clamp source current		1			mA
$V_{ZCDCLAMP}$	ZCD Clamp voltage	$I_{ZCDCLAMP}$=1.0mA		-120		mV
T_{LEBOVP}	Leading edge blanking time		0.69	0.77	0.85	μs
V_{ZCDH}	ZCD valley detection rising edge	V_{DRV} = low		0.40		V
$I_{LINECOMPST}$	Line voltage compensation threshold ZCD clamp current			135		μA
$K_{LINECOMP}$	The ratio of line voltage compensation			0.3		
$R_{LINECOMP}$	Line voltage compensation resistor			2.5		kΩ

Feedback Voltage (FB)						
V_{FBOPEN}	Open Loop Voltage	I_{FB} = 0		3.0		V
R_{FB}	FB pull-up resistor			10		kΩ
V_{FBOLP}	OLP or FB open loop			2.5		V
T_{FBOLP}	Debounce time of FB open loop protection	V_{FB} > 2.8V		64		ms
V_{FBBST}	FB voltage when DRV stops pulsing		0.4			V
$V_{FBBSTHYS}$	V_{FBBSTH} hysteresis voltage			0.1		V
Current Sense (CS)						
T_{SSCS}	Soft start time of CS threshold	After start up and no trigger protection		4.1		ms
$V_{CSLIMIT}$	Cycle by cycle current limited		0.47	0.495	0.52	V
T_{LEBCBC}	Leading edge blanking time			275		ns
V_{CS_SSCP}	Secondary rectifier short protection			0.9		V
N_{CS_SSCP}	Secondary rectifier short circuit protection debounce counter			3		cycles
$T_{LEBSSCP}$	Leading edge blanking time			165		ns
V_{CSMIN}	CS minimum voltage			0.1		V
ΔV_{CS}	CS jitter			±5		%
T_{JIT}	CS jitter cycle			240		cycles
GaN Section						
R_{DS_ON}	Drain-source On-state Resistance	V_{GS} = 6V, I_D = 3A, T_j = 25 °C		165	240	mΩ
		V_{GS} = 6V, I_D = 3A, T_j = 150 °C		360		mΩ
C_{OSS}	Output capacitance	V_{GS} = 0V, V_{DS} = 400V; f = 100kHz		25		pF
Q_{OSS}	Output charge	V_{GS} = 0V, V_{DS} = 0 to 400V		21		nC
External OTP (OTP)						
I_{OTP}	Current source for OTP		95	110	123	uA
V_{OTP}	External OTP trigger voltage		0.47	0.5	0.53	V
T_{OTPP}	External OTP detection period			10		ms
T_{OTPDEB}	OTP debounce time			560		us
Internal Boost Circuit (SW)						
I_{SWOFF}	Boost circuit turn off current			0.1	0.12	A
$T_{SWONMAX}$	Boost maximum on time			1.30		μs
$T_{SWOFFMIN}$	Boost minimum off time			0.50		μs
Oscillator for Switching Frequency						
F_{SW}	Switching frequency		165	175	185	kHz
F_{SWMIN}	Minimum frequency			25		kHz
T_{OFFMAX}	Maximum off time			35		μs
T_{ONMAX}	Maximum on time			25		μs
Internal Over-Temperature Protection (OTP)						
OTP_H	OTP Temperature			150		℃

OTP_{HYS}	OTP Hysteresis		20	℃

8 Functional Block Diagram

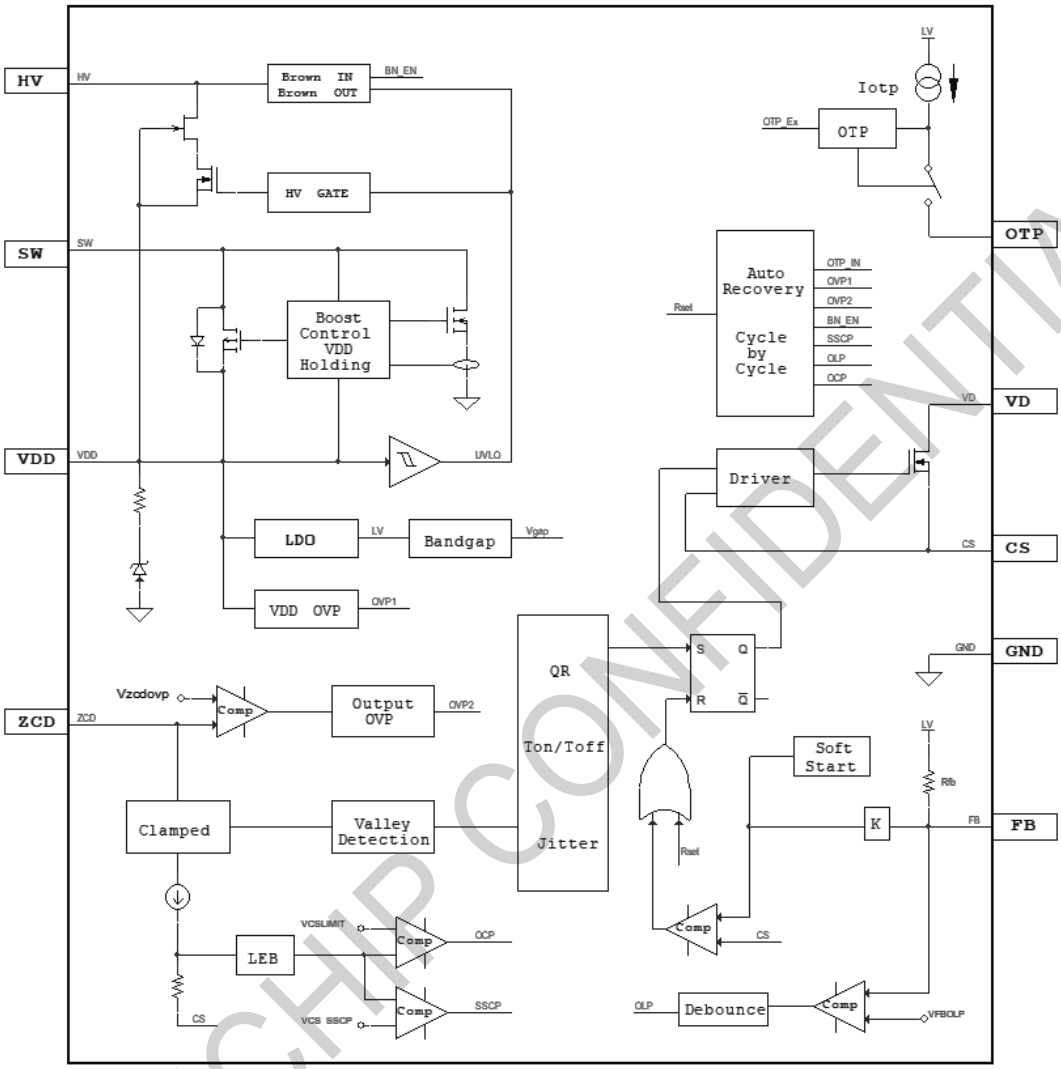


Fig.3 Function Block Diagram

9 Feature Description

SC3057B is designed for USB-PD solutions, together with PD converter, such as SC21xx series. It integrates GaN FET, so that the high efficiency and power density can be achieved. SC3057B provides an adaptive switching frequency fold-back to achieve higher efficiency in the whole loading range.

The converter integrates a segment power supply circuit for VDD, which is especially suitable for applications with a wide output voltage range, saving power consumption and greatly reducing peripheral devices. The built-in high voltage start-up circuit can achieve short start-up time, and extremely low standby power.

It operates in DCM or QR mode in full load range. The controller operates in green mode with valley switching for high efficiency when the valley counter is below 7. And at no load, the IC will operate in Burst mode to reduce power consumption.

9.1 Start-up

After AC power on, the VDD will be charged by HV pin with 1mA current until VDD voltage higher than 0.5V. After VDD voltage rise above 0.5V, the charging current rise to I_{HV_VDD2} until VDDon.

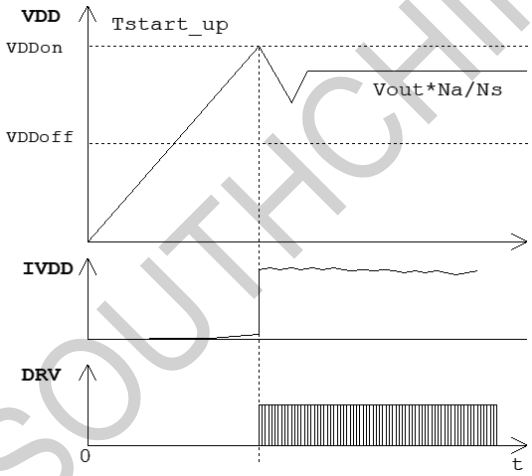


Fig. 3 VDD start-up waveform

The maximum start-up time can be estimated by the following equation:

$$T_{START-UP} = \frac{C_{VDD*}0.5V}{IHV\_VDD1} + \frac{C_{VDD*}(VDDon - 0.5)V}{IHV\_VDD2}$$

Where, C_{VDD} is VDD cap, VDDon is VDD on threshold voltage.

9.2 VDD UVLO

A hysteresis of UVLO (Under Voltage Lock Out) comparator is implemented in SC3057B. The turn-on and turn-off thresholds are fixed at V_{DDON} and V_{DDOFF} respectively. This hysteresis ensures that the VDD capacitor can be small enough during start-up. A large hysteresis is essential to ensure the IC works properly during the start-up period, even for a small VDD capacitor.

9.3 VDD Holding Mode

After the system starts, the VDD capacitor can be charged by the auxiliary winding. There are some operation condition changes (load changes, output voltage adjustment, burst mode), may lead the primary side DRV stop working when the output value is higher than the set value. Furthermore, the VDD voltage will be lower than V_{DDOFF} and the system will stop. To avoid this situation, a VDD holding circuitry is designed, which starts working when VDD drops below $V_{DDHOLDL}$ and stops working when VDD rises above $V_{DDHOLDH}$. The working process is shown in fig.4.

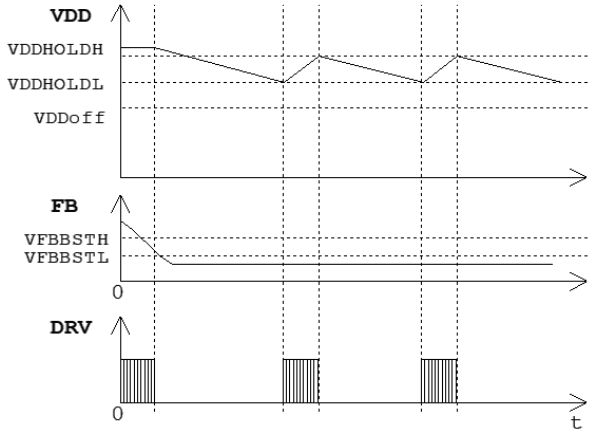


Fig. 4 VDD holding circuitry

9.4 Segment Power Supply Circuit for VDD Power Supply

In some applications with a wide output voltage range, especially for chargers that need to support PPS, the output voltage range is 3.3V ~ 21V. In order to meet the power supply of the SSR converter, additional circuits need

to be added, such as LDO or additional auxiliary windings of transformer. This increases the power consumption and cost of system. The SC3057B integrates a segment power supply circuit, which can guarantee the power supply of VDD under the low output voltage of auxiliary winding. Only a surface-mount inductor is added. The working process of the circuit is shown in fig.5.

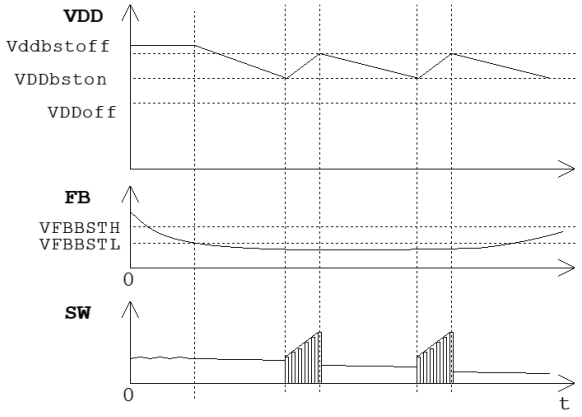


Fig. 5 The Segment Power Supply Circuit

9.5 Brown IN/OUT Detection and X-Cap Discharge

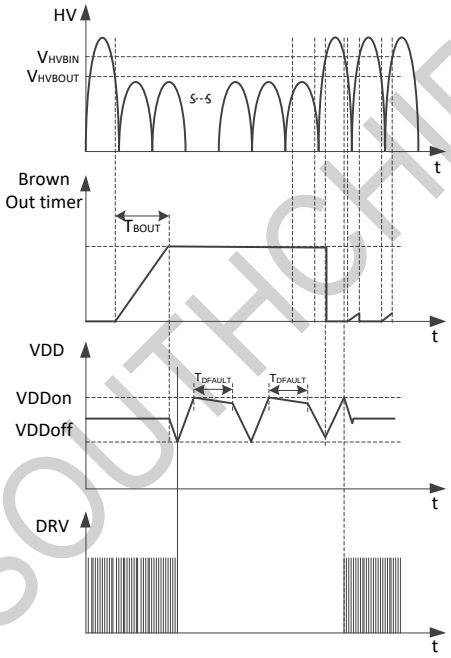


Fig. 6 Brown In/Out detection

The Brown IN/OUT function is implemented through HV pin. When HV pin voltage rises above V_{HVBIN}, the IC starts working, and it stops working when HV pin voltage decreases below V_{HVBOUT}. When HV voltage drops below V_{HVBOUT}, a brown-out timer is enabled. The converter is disabled if HV voltage doesn't exceed V_{HVBOUT} before brown-out timer expires.

SC3057B integrates X-cap discharge function. When detected the voltage on HV pin drops and no rising edge detected after T_{XDET}, it is considered that the AC power is disconnected, and then the X-cap discharge function is enabled. The HV pin generates a source current of 5mA to discharge the X-Cap until the voltage drops to a very low level.

9.6 Operation Mode

SC3057B provides an adaptive switching frequency fold-back to achieve higher efficiency in the whole loading range. It operates in DCM or QR mode under full load range. The maximum frequency is 175kHz.

At heavy load or full load, SC3057B probably operates in QR Mode with high switching frequency. When the load current decreases, it will operate in green mode (DCM) with valley switching for high efficiency. When in QR or green mode, the switching valley ranges from 1st valley to the 7th valley as load current decreases. The SC3057B won't detect the valley voltage anymore if the valley numbers are more than 7. And at no load, the IC will operate in Burst mode to reduce power consumption. In this condition, switching loss of MOSFET is the main power dissipation. The DRV will be disabled immediately if V_{FB} drops below V_{FBBSTL}. When V_{FB} rises up to V_{FBBSTH}, the DRV starts to pulse again.

9.7 GaN Device

SC3057B integrates GaN FET and its driver. The built-in line compensation resistor is help to achieve a constant power limit over different line voltage. In this way, the peripheral components can be greatly simplified, and the reliability is greatly improved.

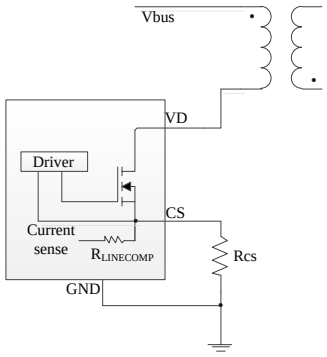


Fig. 7 current sense

9.8 Valley Switching

ZCD pin can detect the freewheel information on the secondary side. In QR mode, when the voltage of ZCD turns to a negative value, it means that after a quarter of the resonant period, the primary MOS can be turned on, and valley opening helps to improve efficiency and improve EMI performance. The best valley opening can be achieved by appropriately adjusting T_{DZCD}, T_{DPG} and T_{DDRV}, where T_{DPG} is an internal fixed delay. T_{DZCD} can be adjusted by connecting a small capacitor in parallel with $R_{ZCDDWON}$. The recommended value is 11pF.

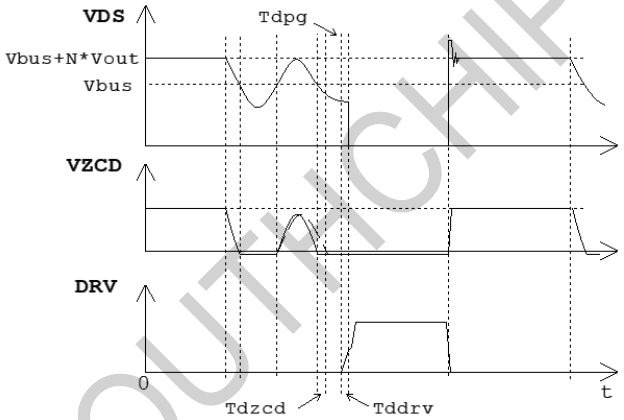


Fig. 8 Valley Switching

9.9 Auto-Recovery after Failure

SC3057B has complex protection functions, such as VDD over voltage protection, VDD under voltage lock out, two level over current protection, output over voltage protection, output short protection, over Load protection, brown IN/Out protection, line voltage over voltage protection. Unless otherwise specified, these protections are auto-recovery. After the protection is triggered, the system enters the protection mode, and the VDD power consumption is reduced. After the T_{DFAULT} delay, the VDD sink current increases until V_{DDOFF}, and VDD starts the restart process. The detailed process is as follows.

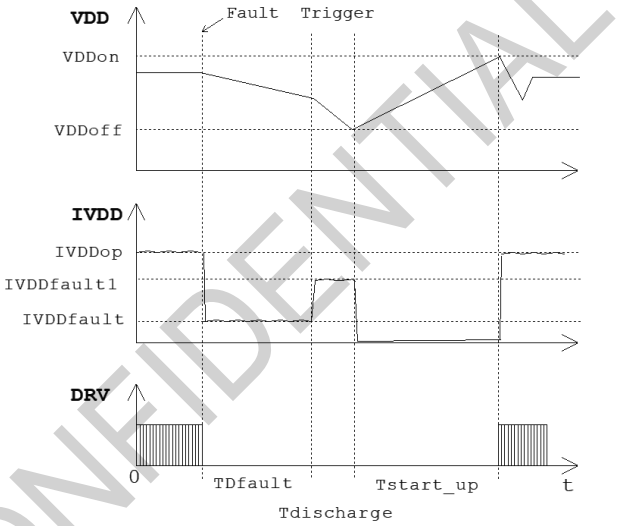


Fig. 9 Auto-Recovery Process

9.10 VDD OVP

When the VDD voltage is higher than the V_{DDOVP} and lasts for a period longer than T_{VDDOVP}, a sink current of I_{VDDOVP} is enabled and DRV will be shut down. The VDD OVP function is an auto-recovery protection.

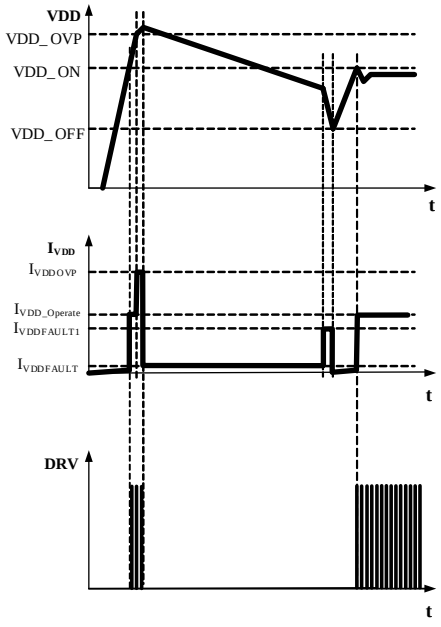


Fig. 10 VDD OVP

9.11 Over Current Protection

Two levels of overcurrent protection are integrated. One is cycle-by-cycle current limiting for overload protection. V_{CSSSCP} is the fast protection for the case of secondary rectifier shorted. The over current protection and its shielding time are shown in fig.11.

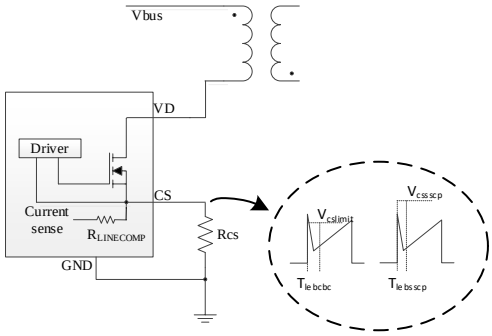


Fig. 11 LEB of OCP

9.12 Adaptive Over Load Protection

An adaptive over load protection is implemented in the SC3057B. When the voltage of VFB is higher than V_{FBOLP} and lasts for a period of time T_{FBOLP}, overload protection will be triggered. In particular, when the voltage of VFB is higher than V_{FBOLP}, and the peak voltage of ZCD pin is lower than V_{ZCDH}, the delay of T_{FBOLP} will be shortened. In the Fig.12, when V_{ZCD} is lower than V_{ZCDH}, the coefficient K is less than 1. The adaptive OLP can reduce the power loss when secondary side is shorted.

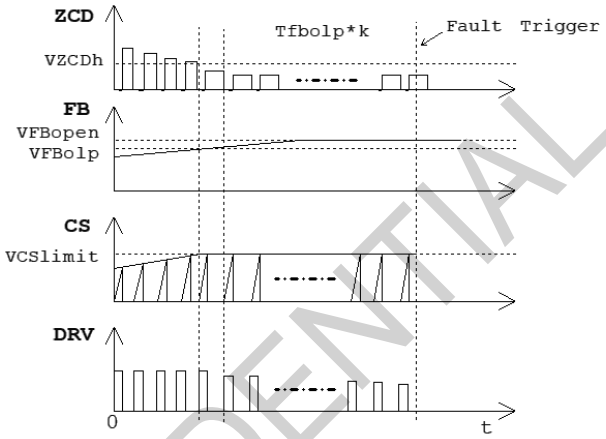


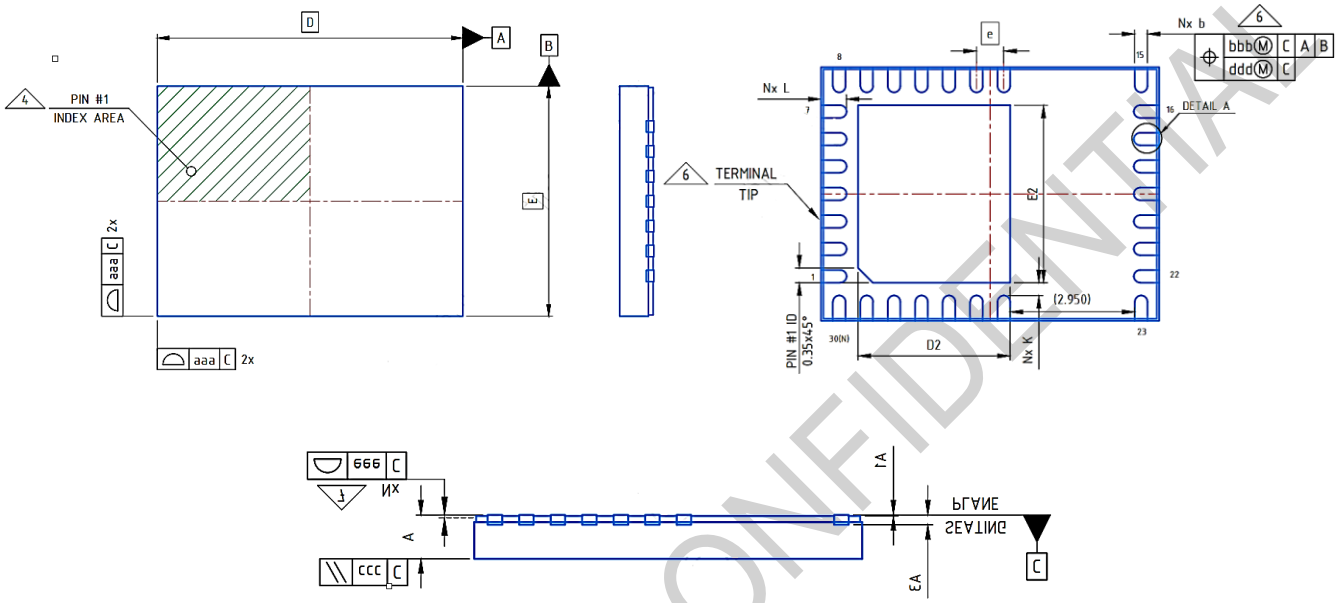
Fig. 12 Adaptive Over Load Protection

9.13 On-Chip OTP

An internal OTP circuit is embedded inside to provide the worst-case protection for SC3057B. When the chip temperature rises higher than the OTP_H, the converter will be disabled and works in the failure mode until the chip is cooled down below the hysteresis OTP_{HYS}.

MECHANICAL DATA

QFN6*8 (6.0mmx8.0mmx0.9mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.8	0.9	1.00
A1	0.00	0.02	0.05
A3		0.203	
b	0.25	0.30	0.35
D		8.00 BSC	
E		6.00 BSC	
e		0.65BSC	
D2	3.50	3.60	3.70
E2	4.10	4.20	4.30
K	0.25		
L	0.50	0.60	0.70
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
N		30	
ND		8	
NE		7	