4V~42V输入，支持100%占空比模式，3.5A同步降压变换器

4~42V Input, Support 100% Duty Cycle, 3.5A, Synchronous Buck Converter

■ FEATURES

- 3.5A converter with 90mΩ+60mΩ FET
- Input voltage range: 4V~42V
- Pulse Skipping Mode (PSM) to keep high efficiency in light load
- 115μA Quiescent Current
- Up to 2MHz Programmable Switching Frequency
- Peak current mode control
- Low Dropout Mode Operation (High duty cycle close to 100%, VOUT < 15V)
- Over-voltage , Over-current and Over-Temperature Protection
- Packages: Pb-free Packages, ESOP8, DFN3×3-10L

- 3.5A降压，内置90mΩ+60mΩ功率管
- 输入电压范围：4V~42V
- 脉冲跳跃模式使得轻载下高效率
- 115uA静态电流
- 最高2MHz可编程开关频率
- 峰值电流控制架构
- 支持低压降模式（接近100%占空比，VOUT<20V）
- 欠压保护、过流保护和过热关断保护
- 无铅封装，ESOP8，DFN3×3-10L

■ APPLICATIONS

- 12V, 24V Industry and Telecom Power System
- Automotive Systems
- Distributed Power Systems
- High Voltage Power Conversion

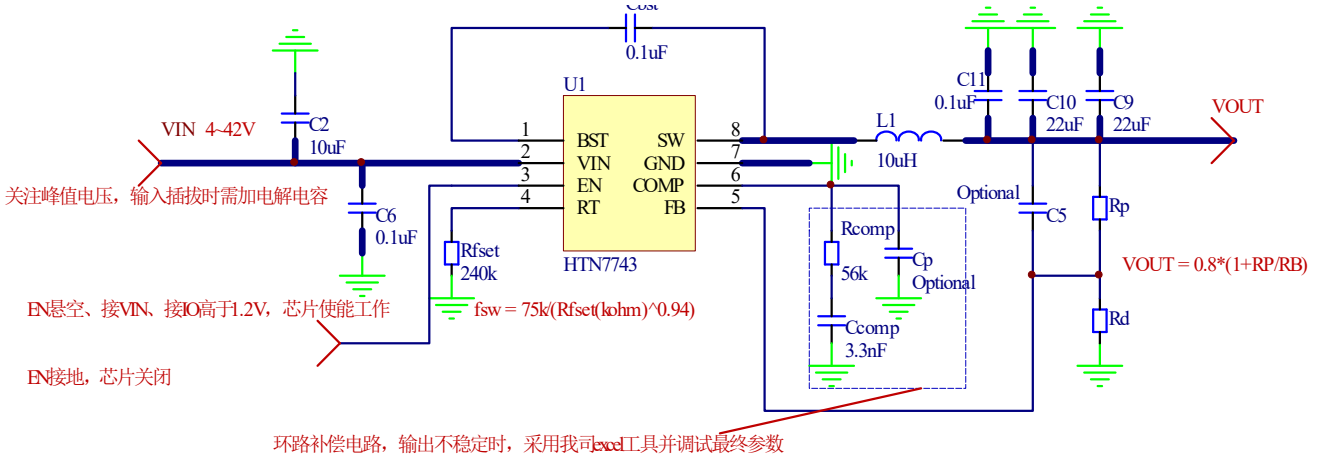
- 12V，24V工业和电信电源轨系统
- 汽车系统
- 分布式电源系统
- 高压电源转换

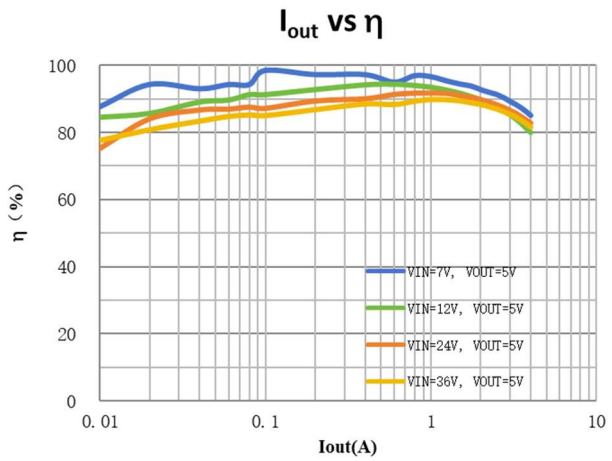
■ DESCRIPTION

The HTN7743 is 3.5A buck converters with wide input voltage, ranging from 4V to 42V, which integrates an 90mΩ high-side MOSFET and an 60mΩ low-side MOSFET. The HTN7743, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) which assists the converter on achieving high efficiency at light load. The HTN7743 features programmable switching frequency from 100kHz to 2MHz with an external resistor. The HTN7743 allows power conversion from high input voltage to low output voltage with a minimum 120ns on-time of switch MOS. The device offers fixed 2.5mS soft start to prevent inrush current during the startup. The HTN7743 features external loop compensation to provide the flexibility to optimize either loop stability or loop response. The HTN7743 provides cycle-by-cycle current limit, thermal shutdown protection, output over-voltage protection, output over load protection and input voltage under-voltage protection. The device is available in an ESOP8 package.

HTN7743是3.5A降压转换器，具有从4V到42V的宽输入电压，集成了90mΩ高侧MOSFET和60mΩ低端MOSFET。HTN7743采用峰值电流模式控制，支持跳周期调制（PSM），有助于转换器在轻负载下实现高效率。HTN7743具有100kHz至2MHz的可编程开关频率，外部电阻可调。HTN7743允许从高输入电压到低输出电压的功率转换，开关MOS的最小导通时间为120ns。该设备提供2.5mS的固定软启动，以防止启动过程中的涌入电流。HTN7743具有外部环路补偿功能，可灵活优化环路稳定性或环路响应。HTN7743提供逐周期电流限制、热关断保护、输出过压保护、输出过载保护和输入电压欠压保护。该设备采用ESOP8封装。

■ TYPICAL APPLICATION

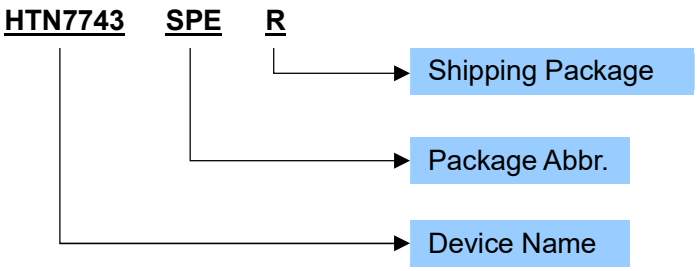




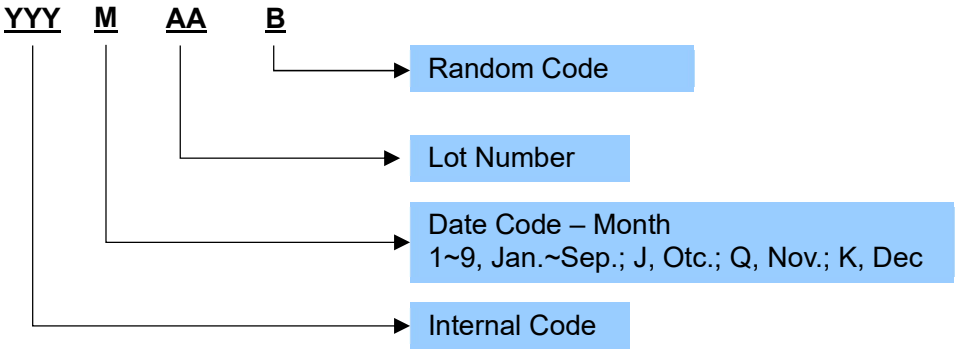
■ ORDERING INFORMATION

Part Number	Package Type	Package Abbr.	Eco Plan	MSL Level	Marking	Shipping Package / MOQ
HTN7743SPER	ESOP8	SPE	RoHS	MSL3	HTN7743 YYYMAAB[1]	Tape and Reel (R) / 2500pcs
HTN7743DNER	DFN3×3-10L	DNE	RoHS	MSL3	HTN7743 YYYMAAB	Tape and Reel (R) / TBD

Part Number

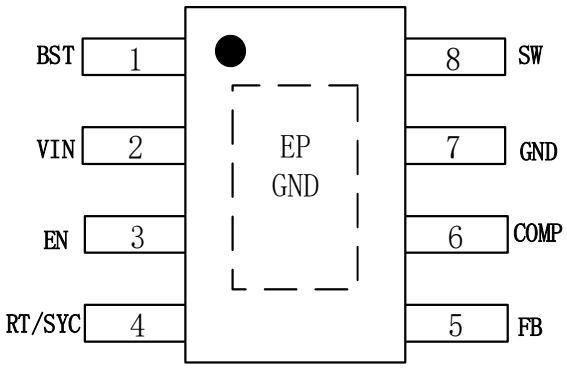


Production Tracking Code

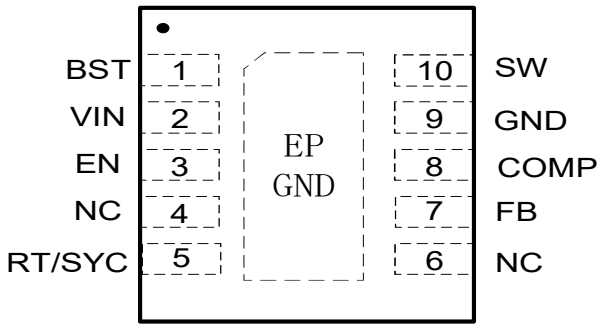


[1] YYYMAAB is production tracking code

■ TERMINAL CONFIGURATION



HTN7743SPE(ESOP8) Top View



HTN7743DNE(DFN3×3-10L) Top View

■ TERMINAL FUNCTION

Pin No.		Name	Description
ESOP	DFN		
1	1	BST	Bootstrap. Power supply for the high-side MOSFET driver. Connect a bypass capacitor between BST and SW. BST是内部高端MOSFET驱动器的正电源。在BST和SW之间连接一个旁路电容器。
2	2	VIN	Input supply. VIN supplies power to all of the internal control circuitries. A decoupling capacitor to ground must be placed close to VIN to minimize switching spikes. 输入电源。VIN为所有内部控制电路供电。接地滤波电容必须放置在VIN附近，以减少开关尖峰。
3	3	EN	Enable pin to the regulator with internal pull-up current source. Pull below 1.2V to disable the converter. Float or connect to VIN to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold. 稳压器使能引脚，带内部上拉电流源。将电压降至1.2V以下禁用转换器。悬空或连接到VIN可以启动转换器。从VIN到GND的电阻分压抽头连接EN引脚的可以调节输入电压锁定阈值。
4	5	RT/SYC	Set the internal oscillator clock frequency or synchronize to an external clock. Connect a resistor from this pin to ground to set switching frequency. An external clock can be input directly to the RT/CLK pin. The internal oscillator synchronizes to the external clock frequency with PLL. If detected clocking edges stops, the operation mode automatically returns to resistor programmed frequency. 设置内部振荡器时钟频率或与外部时钟同步。将一个电阻器从该引脚连接到地，以设置开关频率。外部时钟可以直接输入到RT/SYC引脚。内部振荡器通过PLL与外部时钟频率同步。如果检测到的时钟边沿停止，操作模式将自动返回电阻器编程频率。
5	7	FB	Feedback. Connect resistor divider to output voltage. 反馈。接分压电阻到输出电压。
6	8	COMP	Error amplifier output. Connect to frequency loop compensation network. 误差放大器输出。连接到频率环路补偿网络。
7	9	GND	Ground. GND should be placed as close to the output capacitor as possible to avoid the high-current switch paths. 地。GND应尽可能靠近输出电容，以避免高电流开关路径。
8	10	SW	Switch node,Connect SW to an external power inductor 开关端口，连接外部功率电感。
--	4, 6	NC	No internal connection, connection GND 内部无电气连接，外部可连接至地。
9	EP	GND	Heat dissipation path of die. Electrically connection to GND pin. 芯片散热路径。与GND引脚电气相连。

■ SPECIFICATIONS[1]

● Absolute Maximum Ratings [2]

PARAMETER	Symbol	MIN	TYP	MAX	UNIT
VIN supply voltage	VIN	-0.3		50	V
BST voltage	BST	-0.3		55.5	V
BST voltage (10ns transient)	BST	-0.3		57.5	V
Voltage between BST and SW	BST to SW	-0.3		6	V
FB voltage	FB	-0.3		5.5	V
EN voltage	EN	-0.3		VIN+0.3	V
SW voltage	SW	-2		50	V
SW voltage (10ns transient)	SW	-3.5		52	V
Moisture Sensitivity Level (MSL)			MSL3		
Junction Temperature	T_J	-40		150	℃
Storage Temperature	T_{STG}	-55		150	℃
ESD, Human-body model (HBM)	HBM		±2000		V
ESD, Charged-device model (CDM)	CDM		±500		V

● Recommended Operating Conditions

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
VIN supply voltage	VIN		4		42	V
BST voltage	BST		-0.1		47.5	V
Voltage between BST and SW	BST to SW		-0.1		5.5	V
FB voltage	FB		-0.1		4.5	V
EN voltage	EN		-0.1		VIN	V
SW voltage	SW		-1.8		42	V
Junction Temperature	T_J		-40		125	℃

● Electrical Characteristics

VIN = 12V, T_A = +25°C, unless otherwise noted.

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
VIN UVLO threshold	V_{UVLO}	Rising		3.9		V
		Falling		3.6		V
VIN UVLO hysteresis	V_{hys}			0.3		V
Quiescent supply current	I_Q	V_{EN} = 12V, V_{FB} = 1.0 V, no switching		115		uA
Shutdown supply current	I_{SD}	V_{EN} = 0V		0.5		μA
High-side switch on resistance	$R_{DS(ON)\_H}$	V_{BST} - V_{SW} = 5.5V		90		mΩ
Low-side switch on resistance	$R_{DS(ON)\_L}$			60		mΩ
Peak Current limit	I_{LIM_peak}			5.5		A
Valley Current limit	I_{LIM_valley}			5		A
EN threshold	V_{ENH}	No voltage hysteresis, rising and falling		1.2		V
EN source current	$I_{source1}$	Enable threshold +50 mV		-4.8		uA
	$I_{source2}$	Enable threshold -50 mV		-1.2		uA
Feedback voltage	V_{FBH}			800		mV
FB input current	I_{FB}	V_{FB} = 0.8V	-100		100	nA
Error Amplifier source/sink		V_{comp} = 1V，Vfb = 0.8±0.1V		±20		uA
Gm of Error Amplifier				188		uS
Minimum on time	t_{ON_MIN}			120		ns
Soft-start time	t_{SS}			2.5		ms

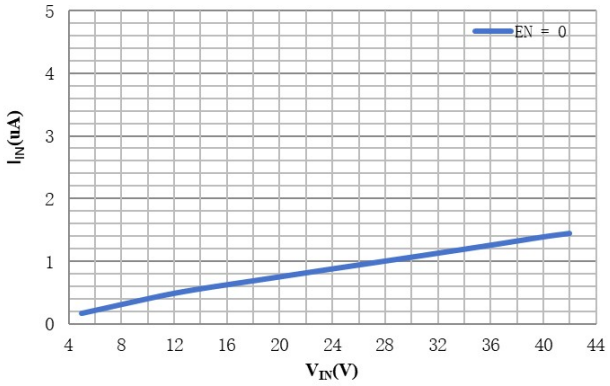
[1] Depending on parts and PCB layout, characteristics may be changed.
[2] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

Switching frequency range	f_{sw}		100		2000	kHz
		RT = 200KΩ		500		kHz
Thermal shutdown		Trigger thermal shutdown		165		℃
		Hysteresis		25		℃

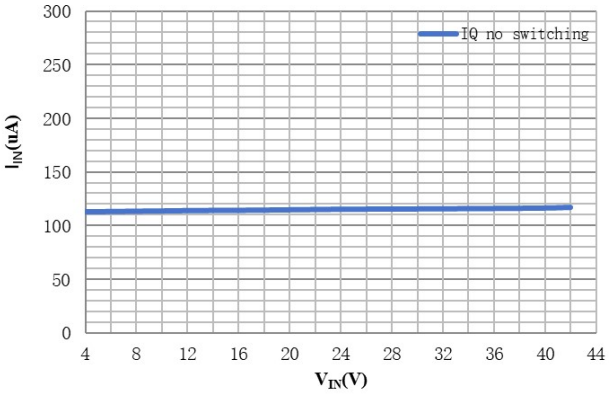
■ TYPICAL OPERATING CHARACTERISTICS

VIN = 24V, VOUT =5V, CIN = 0.1uF//10uF, COUT = 0.1uF//22uF//22uF, L = 10μH, RT = 240k, Rcomp = 56k, Ccomp = 3.3nF, TA = +25°C, unless otherwise noted.

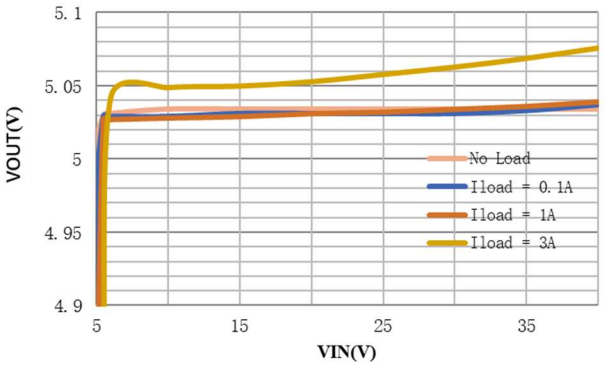
V_{IN} vs I_{IN}



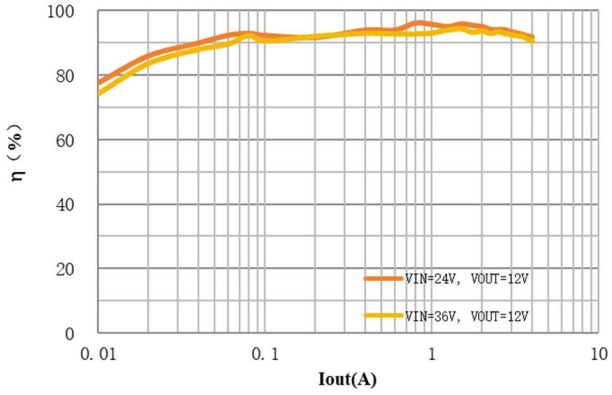
V_{IN} vs I_{IN}



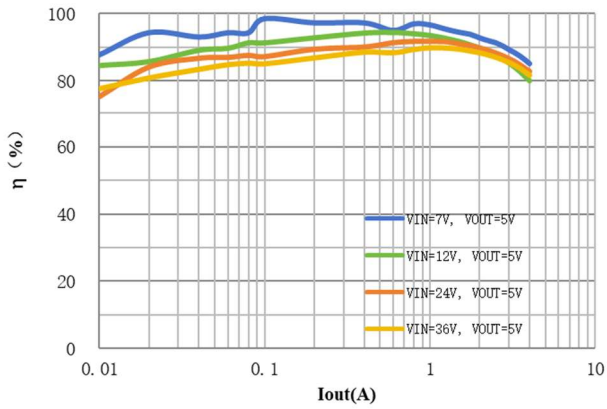
VOUT vs VIN



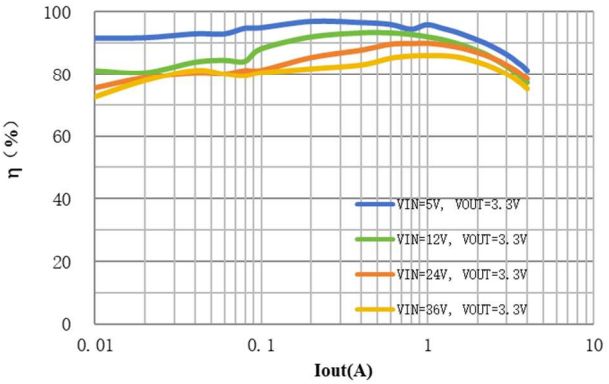
I_{out} vs η



I_{out} vs η



I_{out} vs η



■ APPLICATION INFORMATION

1 Description

The HTN7743 is 3.5A buck converters with wide input voltage, ranging from 4V to 42V, which integrates an 90mΩ high-side MOSFET and an 60mΩ low-side MOSFET. The HTN7743, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) which assists the converter on achieving high efficiency at light load. The HTN7743 features programmable switching frequency from 100kHz to 2MHz with an external resistor. The HTN7743 allows power conversion from high input voltage to low output voltage with a minimum 120ns on-time of switch MOS. The device offers typical 2.5mS soft start to prevent inrush current during the startup. The HTN7743 features external loop compensation to provide the flexibility to optimize either loop stability or loop response. The HTN7743 provides cycle-by-cycle current limit, thermal shutdown protection, output over-voltage protection, output over load protection and input voltage under-voltage protection. The device is available in an ESOP8, DFN3×3-10L package.

HTN7743 是 3.5A 降压转换器，具有从 4V 到 42V 的宽输入电压，集成了 90mΩ高侧 MOSFET 和 60mΩ低端 MOSFET。HTN7743 采用峰值电流模式控制，支持跳周期调制（PSM），有助于转换器在轻负载下实现高效率。HTN7743 具有 100kHz 至 2MHz 的可编程开关频率，外部电阻可调。HTN7743 允许从高输入电压到低输出电压的功率转换，开关 MOS 的最小导通时间为 120ns。该设备提供 2.5mS 的典型软启动，以防止启动过程中的涌入电流。HTN7743 具有外部环路补偿功能，可灵活优化环路稳定性或环路响应。HTN7743 提供逐周期电流限制、热关断保护、输出过压保护、输出过载保护和输入电压欠压保护。该设备采用 ESOP8, DFN3×3-10L 封装。

2 Enable (EN) Control

The HTN7743 is enabled when the VIN pin voltage rises above 3.8 V and the EN pin voltage exceeds the enable threshold of 1.2 V. The HTN7743 is disabled when the VIN pin voltage falls below 3.6 V or when the EN pin voltage is below 1.2 V. The EN pin has an internal pull-up current source, I1, of 1.2 µA that enables operation of the HTN7743 when the EN pin floats. If an application requires a higher under-voltage lockout (UVLO) threshold, to adjust the input voltage UVLO with two external resistors. When the EN pin voltage exceeds 1.2 V, an additional 3.6µA of hysteresis current, IHYS, is sourced out of the EN pin. When the EN pin is pulled below 1.2 V, the 3.6µA Ihys current is removed. This additional current facilitates adjustable input-voltage UVLO hysteresis.

当 VIN 引脚电压升至 3.8V 以上且 EN 引脚电压超过 1.2 V 的启用阈值时，HTN7743 启用。当 VIN 引脚的电压降至 3.6 V 以下或 EN 引脚的电压低于 1.2 V 时，HTN7743 禁用。EN 引脚有一个 1.2 µA 的内部上拉电流源 I1，当 EN 引脚浮空时，它可以使 HTN7743 工作。如果应用需要更高的欠压锁定（UVLO）阈值，则使用两个外部电阻调整输入电压 UVLO。当 EN 引脚电压超过 1.2 V 时，EN 引脚会额外提供 3.6 µA 的滞回电流 IHYS。当 EN 引脚被拉到 1.2V 以下时，3.6 µA 的电流被移除。这种额外的电流有助于调节输入电压 UVLO 滞回。

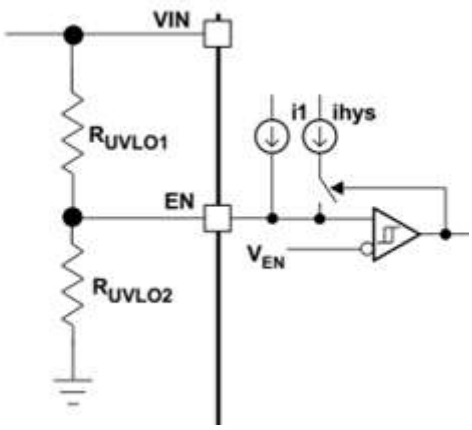


Figure 1 EN Terminal Schematic

3 Soft Start and Start Delay with Pre-biased Output Voltage

The HTN7743 employs an internal 2.5mS soft start to ramp up the FB voltage from 0V to 0.8V linearly once EN pulled high.

If the output voltage is pre-biased when EN is pulled high, the device start switching and ramping up only after internal reference voltage is larger than V_{FB}.

HTN7743 采用内部 2.5mS 软启动，一旦 EN 拉高，FB 电压就会线性上升至 0.8V。

如果 EN 被拉高时输出有预偏置电压，器件仅在内部基准电压大于 V_{FB} 后开始工作。

4 Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at an insufficient supply voltage. The UVLO rising threshold is about 3.9V, while its falling threshold is about 3.6V.

欠压锁定（UVLO）功能可避免芯片工作在电源电压不足的条件。UVLO 上升阈值约为 3.9V，下降阈值为 3.6V。

5 Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than its upper threshold, the entire chip shuts down. When the temperature is lower than its lower threshold, the chip is enabled again.

过热关断保护是为了防止芯片在极高的温度下工作。当芯片温度高于其上限阈值时，整个芯片关闭。当温度低于其下限阈值时，芯片再次启用。

6 Peak Current Mode Control

The HTN7743 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the integrated high-side MOSFET is turned off. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent subharmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control. The HTN7743 operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold (700mV typically), device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold. Then high-side power MOSFET turns on in next clock pulse. After several switching cycles, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded. This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. The controller consumption quiescent current is 115uA during skipping period with no switching to improve efficiency further.

HTN7743 采用固定频率峰值电流模式控制。内部时钟在每个周期启动内部高侧功率 MOSFET 的开启，然后电感器电流线性上升。当通过高侧 MOSFET 的电流达到由内部误差放大器的 COMP 电压设置的阈值水平时，集成的高侧 MOSFET 被关断。当负载电流增加时，相对于参考电压的反馈电压降低会提高 COMP 电压，直到平均电感器电流与增加的负载电流相匹配。该反馈回路很好地将输出电压调节到参考值。该设备还集成了一个内部斜坡补偿电路，以防止在固定频率峰值电流模式控制的占空比大于 50% 时发生次谐波振荡。HTN7743 在轻负载电流下以脉冲跳过模式（PSM）运行，以提高效率。当负载电流降低时，反馈电压的增加导致 COMP 电压降。当 COMP 降至低箝位阈值（通常为 700mV）时，设备进入 PSM。在跳跃期间，由于输出电容器放电，输出电压衰减。一旦 FB 电压降至低于参考电压，并且 COMP 电压升至低箝位阈值以上，高侧功率 MOSFET 在下一个时钟脉冲中导通。在几个开关周期后，COMP 电压下降并再次被箝位，如果输出继续轻载，则重复跳周期模式。这种控制方案通过跳过周期来减少开关功率损耗和栅极驱动充电损耗，从而有助于实现更高的效率。控制器在跳过期间消耗的静态电流为 115uA，无需切换，以进一步提高效率。

7 Bootstrap Voltage Regulator and Low Drop-out Operation

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and the external low-side diode conducts. The recommended value of the BOOT capacitor is 0.1μF. The UVLO of high-side MOSFET gate driver has rising threshold of 2.6V and hysteresis of 210mV. When the device operates with high duty cycle or extremely light load, bootstrap capacitor may be not recharged in considerable long time. The voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. When the voltage across bootstrap capacitor drops below 2.39V, BOOT UVLO occurs. The converter forces turning on an integrated low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee the converter's operation over a wide duty range. During the condition of ultra-low voltage difference from the input to the output, HTN7743 operates in Low Drop-Out LDO mode. High-side MOSFET remains turning on as long as the BOOT pin to SW pin voltage is higher than BOOT UVLO threshold 2.6V. When the voltage from BOOT to SW drops below 2.39V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Low-side MOSFET only turns on for 200ns in each refresh cycle to minimize the output voltage ripple. Low-side MOSFET may turn on for several times till the bootstrap voltage is charged to higher than 2.6V for high-side MOSFET working normally. The effective duty cycle of the converter during LDO operation can be approaching to 100%. During slowing power up and power down application, the output voltage can closely track the input voltage ramping down thanks to LDO operation mode.

BOOT 引脚和 SW 引脚之间的外部自举电容器为高侧功率 MOSFET 的浮栅驱动器供电。当高侧功率 MOSFET 关断并且外部低侧二极管导通时，自举电容器电压从集成电压调节器充电。BOOT 电容器的推荐值为 0.1μF。高侧 MOSFET 栅极驱动器的 UVLO 具有 2.6V 的上升阈值和 210mV 的滞后。当设备以高占空比或极轻负载运行时，自举电容器可能在相当长的时间内无法再充电。自举电容器上的电压不足以驱动高压侧 MOSFET 完全导通。当自举电容上的电压降至 2.39V 以下时，会发生 BOOT UVLO。转换器周期性地强制开启集成低压侧 MOSFET，以刷新自举电容器的电压，从而保证转换器在宽占空比范围内的运行。在输入到输出的超低电压差条件下，HTN7743 以低压差 LDO 模式运行。只要 BOOT 引脚到 SW 引脚的电压高于 BOOT UVLO 阈值 2.6V，高侧 MOSFET 就会保持导通。当从 BOOT 到 SW 的电压降至 2.39V 以下时，高压侧 MOSFET 关断，低压侧 MOSFET 接通，在接下来的几个开关周期内定期对自举电容器进行充电。低侧 MOSFET 在每个刷新周期中仅导通 200ns，以尽量减少输出电压纹波。低侧 MOSFET 可能会导通几次，直到自举电压充电到高于 2.6V，以便高侧 MOSFET 正常工作。LDO 操作期间转换器的有效占空比可以接近 100%。在缓慢加电和断电应用期间，由于 LDO 操作模式，输出电压可以密切跟踪输入电压的下降。

8 Over Current Limit and Hiccup Mode

The inductor current is monitored during high-side MOSFET and low-side MOSFET on. The HTN7743 implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition. When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The COMP pin voltage ramps up to high clamp voltage 1.65V typical. When COMP voltage is clamped for 256 cycles, the converter stops switching. After remaining OFF for about 12mS，the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and make COMP voltage clamped at high for 256 cycles，the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enter normal regulating

在高侧 MOSFET 和低侧 MOSFET 导通期间监测电感电流。HTN7743 通过逐周期限制高侧 MOSFET 峰值电流和低侧 MOSFET 谷值电流来实现过电流保护，以避免电感器电流在意外过载或输出硬短路情况下失控。当发生过载或硬短路时，转换器无法提供输出电流以满足负载要求。电感器电流被箝位在过电流限制下。因此，输出电压持续下降到低于调节电压，FB 电压低于内部参考电压。COMP 引脚电压上升到典型的高箝位电压 1.65V。当 COMP 电压被箝位 256 个周期时，转换器停止切换。在保持关闭状态约 12mS 后，设备从软启动阶段重新启动。如果软启动期间过载或硬短路情况仍然存在，并使 COMP 电压在 256 个周期内保持在高电平，则设备再次进入关闭模式。当过载或硬短路条件消除时，设备会自动恢复，进入正常调节操作。上述打嗝保护模式使平均短路电流减轻热问题并保护调节器。

operation. The hiccup protection mode above makes the average short circuit current to alleviate thermal issues and protect the regulator.

9 Clock Setting and Clock Synchronization

The HTN7743 oscillating frequency is set by an external resistor R_{fset}, from the RT pin to ground. The value of R_{fset} can be set according to the following equation or curve.

HTN7743 的开关频率可通过 RT 对地电阻 Rfset 调节，参考如下公式或曲线图。

$$FSW(kHz) = \frac{75000}{Rfset(kohm)^{0.94}} \quad (1)$$

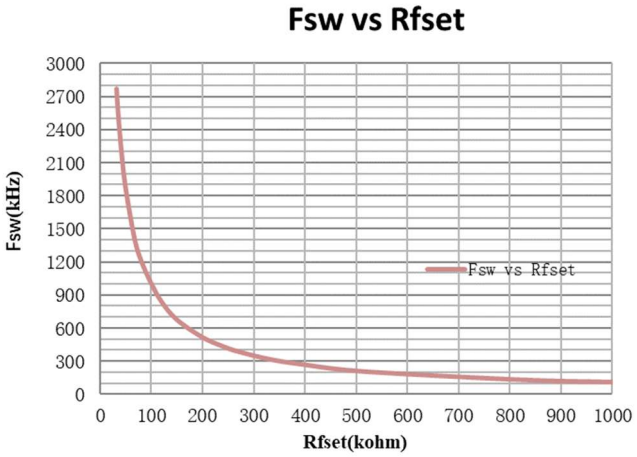


Figure 2 Fsw vs Rfset

In clock synchronization mode, the switching frequency synchronizes to an external clock applied to RT/SYC pin. The synchronization frequency range is from 100KHz to 2MHz and the rising edge of the SW synchronizes to the falling edge of the external clock at RT/SYC pin with typical 60ns time delay. A square wave clock signal to RT/SYC pin must have high level no lower than 1.7V, low level no higher than 0.5V, and pulse width larger than 80ns

在时钟同步模式下，开关频率与施加到 RT/SYC 引脚的外部时钟同步。同步频率范围为 100KHz 至 2MHz，SW 的上升沿与 RT/SYC 引脚处的外部时钟的下降沿同步，具有典型的 60ns 时延。RT/SYC 引脚的方波时钟信号必须具有不低于 1.7V 的高电平、不高于 0.5V 的低电平和大于 80ns 的脉冲宽度。

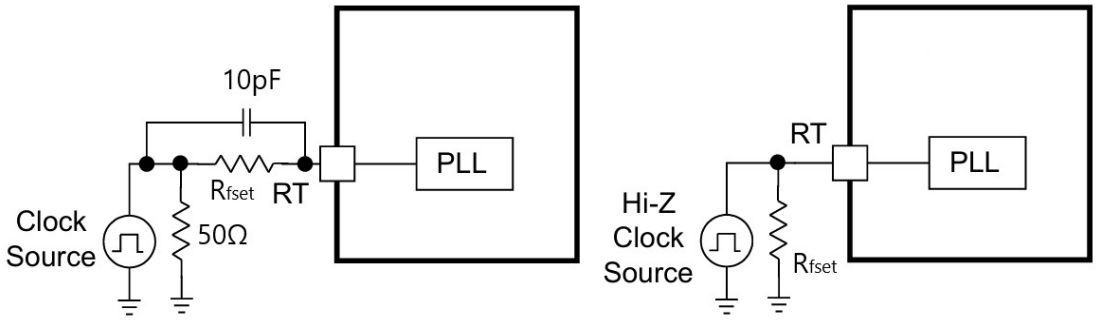


Figure 3 External Clock Synchronization Schematic

10 Setting the Output Voltage

The output voltage (V_{OUT}) is set by a resistor divider (R_P and R_B). The resistors can be determined with following Equation.

Where V_{FB} is 0.8V, typically.

输出电压（VOUT）由电阻分压器（R_P 和 R_B）设置。 电阻可以通过以下公式确定。

其中，V_{FB} =0.8V。

$$VOUT = V_{FB} \times \left(1 + \frac{R_P}{R_B}\right) \quad (2)$$

11 Overvoltage Protection

The HT7743 incorporates an output OVP circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients in designs with low output capacitance. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier increases to a maximum voltage corresponding to the peak-current-limit threshold. When the overload condition is removed, the regulator output rises, and the error amplifier output transitions to the normal operating level. In some applications, the power-supply-output voltage can increase faster than the response of the error-amplifier output resulting in an output overshoot. The OVP feature minimizes output overshoot when using a low-value output capacitor by comparing the FB pin voltage to the rising OVP threshold, which is nominally 109% of the internal voltage reference. If the FB pin voltage is greater than the rising OVP threshold, the high-side MOSFET is immediately disabled to minimize output overshoot. When the FB voltage drops below the falling OVP threshold, which is nominally 106% of the internal voltage reference, the high-side MOSFET resumes normal operation.

HT7743 集成了一个输出 OVP 电路，以在低输出电容的设计中从输出故障条件或强卸载瞬态中恢复时，最大限度地减少电压过冲。例如，当电源输出过载时，误差放大器将实际输出电压与内部参考电压进行比较。如果 FB 引脚电压在相当长的一段时间内低于内部参考电压，则误差放大器的输出增加到与峰值电流限制阈值对应的最大电压。当过载条件消除时，稳压器输出上升，误差放大器输出转换到正常工作电平。在某些应用中，电源输出电压的增加可能比误差放大器输出的响应更快，从而导致输出过冲。当使用低值输出电容器时，OVP 功能通过将 FB 引脚电压与上升的 OVP 阈值（标称为内部电压参考的 109%）进行比较，最大限度地减少了输出过冲。如果 FB 引脚电压大于上升的 OVP 阈值，则立即禁用高侧 MOSFET 以最小化输出过冲。当 FB 电压降至 OVP 阈值（标称为内部电压参考的 106%）以下时，高侧 MOSFET 恢复正常工作。

12 Selecting the Inductor, Diode and Output Capacitor

Use the inductor and output capacitor as following.

推荐电感和输出电容如下表。

OUTPUT VOLTAGE (V)	R_P (kΩ)	R_B(kΩ)	L (uH)			C_{OUT}(uF)
			MIN	TYP	MAX	
1.8	66.5	53.6	6.8	10	15	22~100
2.5	61.9	29.4	6.8	10	15	22~100
3.3	127	40.2	6.8	10	15	22~100
5	48.7	9.31	6.8	10	15	44~100
12	140	10	6.8	10	15	68~100

The inductor peak-to-peak ripple current I_{L_PP}, peak current I_{L_PK} and RMS current I_{L_RMS} are calculated as following. The inductor saturation current rating must be greater than the I_{L_PK} and the RMS or heating current rating must be greater than I_{L_RMS}.

电感峰峰值电流 I_{L_PP}、峰值电流 I_{L_PK} 和 RMS 电流 I_{L_RMS} 计算如下。电感额定饱和电流必须大于 I_{L_PK}，RMS 或热电流额定值必须大于 I_{L_RMS}。

$$I_{L_{PP}} = \frac{V_{OUT}}{V_{IN_{MAX}}} \times \frac{V_{IN_{MAX}} - V_{OUT}}{L \times f_{SW}} \quad (3)$$

$$I_{L_{PK}} = I_{OUT} + \frac{I_{L_{PP}}}{2} \quad (4)$$

$$I_{L_{RMS}} = \sqrt{{I_{OUT}}^2 + \frac{1}{12} \times {I_{L_{PP}}}^2} \quad (5)$$

The output capacitor should be used with ceramic or other low ESR capacitors. The required RMS current rating for the output capacitor is as follow.

输出电容应使用陶瓷电容或其他低 ESR 电容。输出电容要求的额定 RMS 电流如下。

$$I_{C_{RMS}} = \frac{\left(V_{IN_{MAX}} - V_{OUT}\right) \times V_{OUT}}{\sqrt{12} \times F_{SW} \times V_{IN_{MAX}} \times L} \quad (6)$$

13 Input Capacitor (C_{IN})

An input decoupling capacitor (0.1uF) and a bulk capacitor (Over 10uF) is needed. The voltage rating should be higher than the maximum input voltage.

输入端推荐一个滤波电容（0.1uF）和一个储能电容（超过 10uF）。额定电压应高于最大输入电压。

14 PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to following figure and follow the guidelines below.

(1) Place the input capacitor and output capacitor as close to the device as possible.

(2) Keep the power traces very short and fairly wide, especially for the SW node.

This can help greatly reduce voltage spikes on the SW node and lower the EMI noise level.

(3) Run the feedback trace as far from the inductor and noisy power traces (like the SW node) as possible.

有效的 PCB 布局对于稳定运行至关重要。要获得最佳结果，请参考下图并遵循以下指南。

（1）将输入电容、输出电容尽可能靠近芯片。

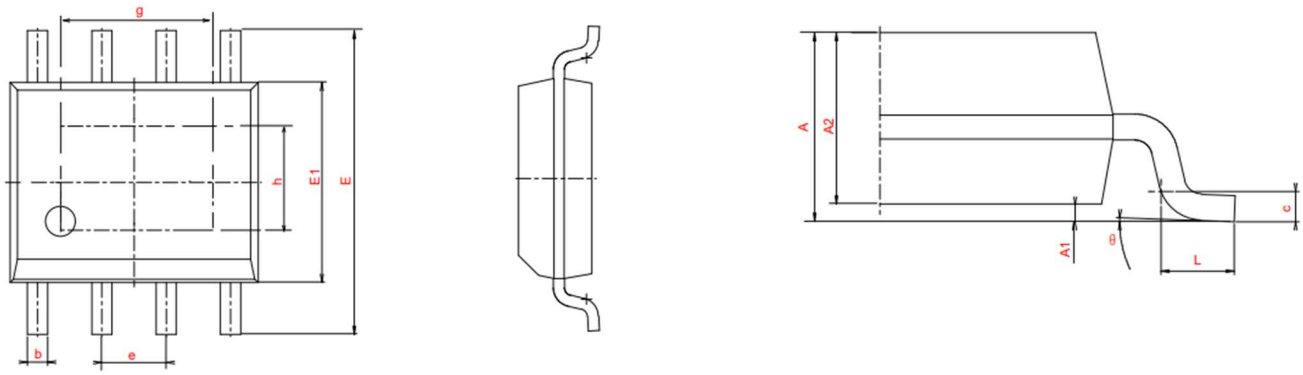
（2）保持电源轨迹非常短且相当宽，特别是对于 SW 节点。

这有助于大大降低 SW 节点上的电压尖峰，并降低 EMI 噪声水平。

（3）FB 走线尽可能远离电感和功率走线（如 SW 节点）。

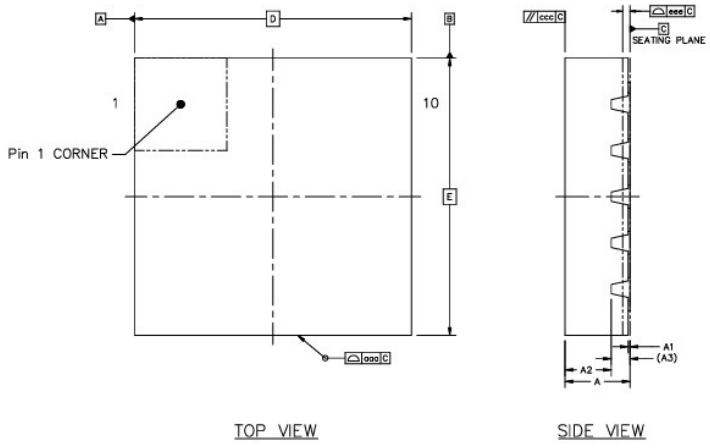
■ PACKAGE OUTLINE

ESOP8

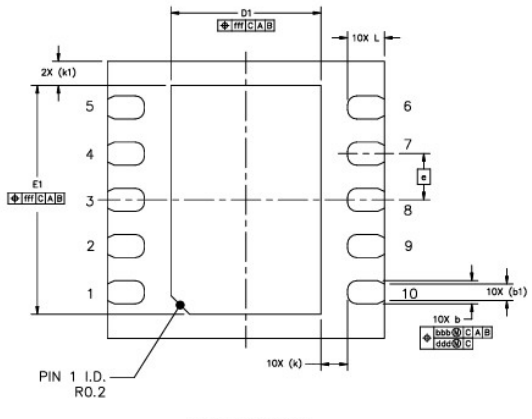


名称	尺寸	
	Min	Max
A	1.45	1.75
A1	0.05	0.15
A2	1.35	1.55
b	0.3	0.5
c	0.22	0.28
D	4.7	5.1
E	5.8	6.2
E1	3.85	4.05
L	0.4	1.27
θ	0 °	8 °
e	1.270 (BSC)	
h	2.4	
g	3.3	

DFN3×3-10L

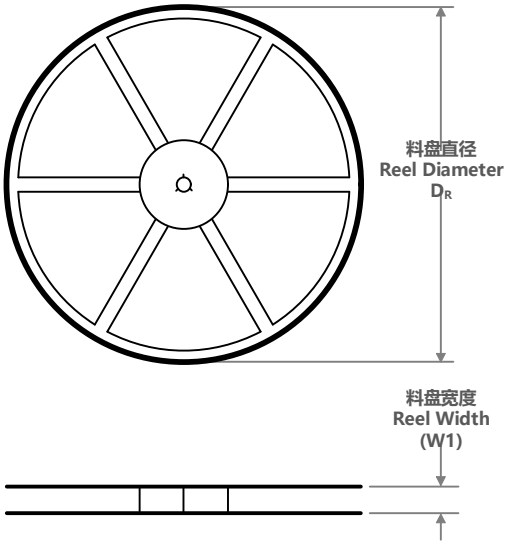


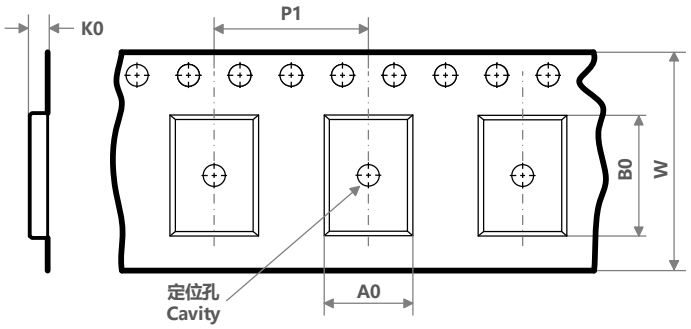
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.2	0.25	0.3
		b1	0.18 REF		
BODY SIZE	X	D	3 BSC		
	Y	E	3 BSC		
LEAD PITCH		e	0.5 BSC		
EXPOSED PAD SIZE	X	D1	1.525	1.625	1.725
	Y	E1	2.375	2.475	2.575
LEAD LENGTH		L	0.35	0.4	0.45
EP EDGE TO LEAD EDGE		k	0.2875 REF		
EP EDGE TO PACKAGE EDGE		k1	0.2625 REF		
PACKAGE EDGE TOLERANCE		aaa	0.05		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.05		
LEAD OFFSET		bbb	0.1		
		ddd	0.08		
EXPOSED PAD OFFSET		fff	0.1		



NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNR LEADS AND DIE ATTACH PAD;
3.PROHIBIT OR RESTRICT THE USE OF HAZARDOUS SUBSTANCES SPECIFIED BY He Xin;
4.FINISH: Cu/EP • Sn8~20s

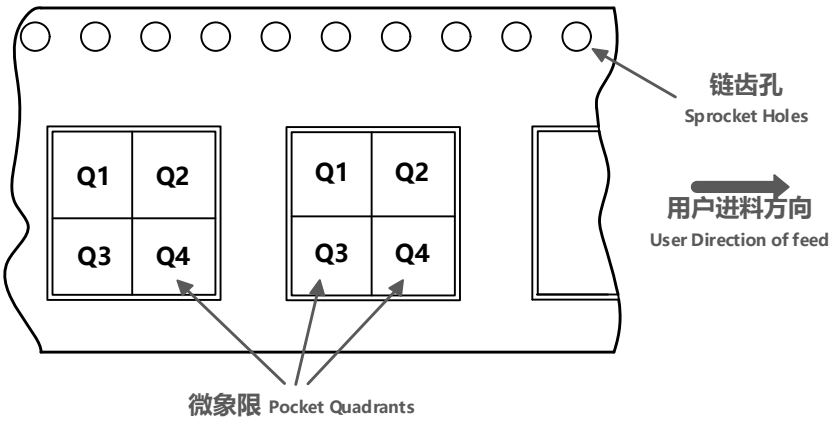
■ TAPE AND REEL INFORMATION





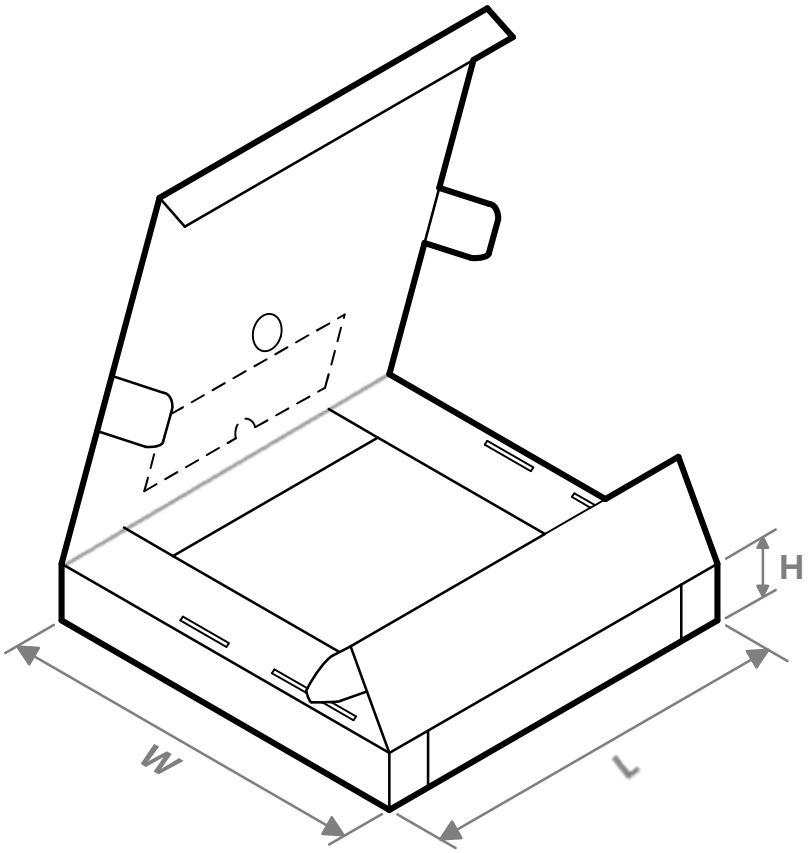
A0	Dimension designed to accommodate the component width; 料槽宽度
B0	Dimension designed to accommodate the component length; 料槽长度
K0	Dimension designed to accommodate the component thickness; 料槽厚度
W	Overall width of the carrier tape; 载带整体宽度
P1	Pitch between successive cavity centers; 相邻槽中心间距

编带 PIN1 方位象限分配
Quadrant Assignments for Pin1 Orientation in Tape



器件料号 Part No.	封装类型 Package Type	封装标识 Package Code	引脚数 Pins	SPQ	料盘直径 D_R(mm)	料盘宽度 W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 象限 Quadrant
HTN7743SPER	ESOP	SPE	8	2500	330	12	6.55	5.55	1.95	8	12	Q1
HTN7743DNER	DFN3×3	DNE	10	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

■ TAPE AND REEL BOX INFORMATION



器件料号 Part No.	封装类型 Package Type	封装标识 Package Code	引脚数 Pins	SPQ	长度 Length (mm)	宽度 Width (mm)	高度 Height (mm)
HTN7743SPER	ESOP	SPE	8	5000	360	345	65
HTN7743DNER	DFN3×3	DNE	10	TBD	TBD	TBD	TBD