1MHz, 18V, 3.0A FPWM Synchronous Step-Down Converter

Features

- Wide Input Voltage Range: 4.5V to 18V
- Output Voltage Range: 0.6V to 7V
- High Efficiency: Up to 93%(@3.3V)
- Force PWM 1MHz Operation
- Up to 3.0A Output Current
- Low $R_{DS(ON)}$ for internal switches: 80mΩ/40mΩ(top/bottom)
- Advanced COT Control to Achieve Fast Transient Responses
- Integrated internal compensation
- Stable with Low ESR Ceramic Output Capacitors
- Over Current Protection with Hiccup Mode
- Thermal Shutdown
- Inrush Current Limit and Soft Start
- Build in Input Over Voltage Protection
- Available in DFN1.6x1.6-6 Package

Description

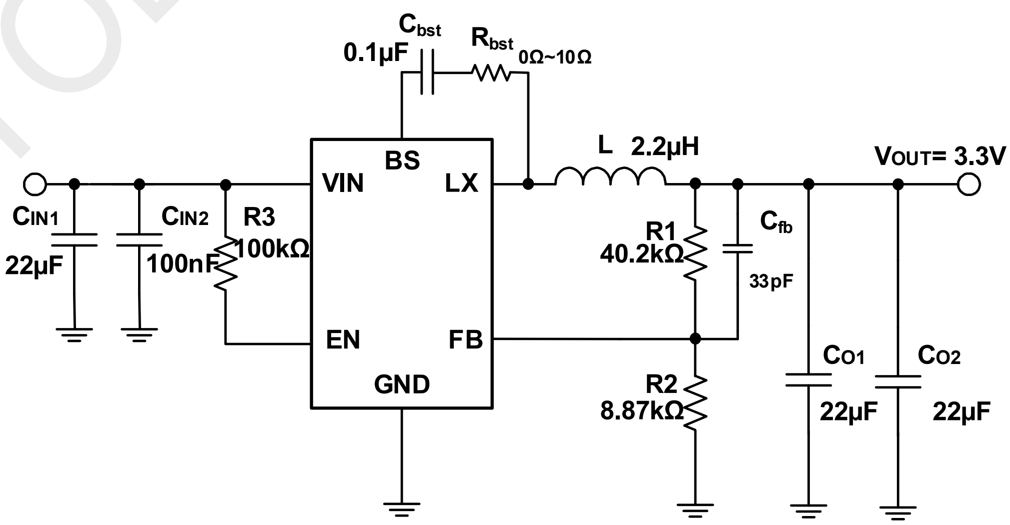
The STI3453FIN is s a high efficiency 1MHz, Advanced Constant-on-Time (COT) control mode synchronous step-down DC-DC converter capable of delivering up to 3A current with FPWM operation. STI3453FIN integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. Low output voltage ripple and small external inductor and capacitor size are achieved with 1MHz switching frequency. It adopts the COT architecture to achieve fast transient responses.

The STI3453FIN requires a minimum number of readily available standard external components and is available in a space saving 6-pin DFN1.6mm x 1.6mm ROHS compliant package.

Application

- Digital Set Top Boxes
- Flat Panel Television and Monitors
- Notebook computer
- Wireless and DSL Modems

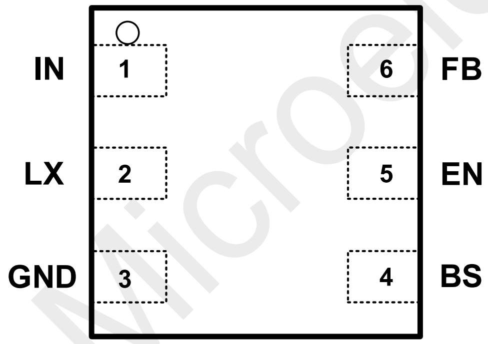
Typical Application



Absolute Maximum Ratings (Note 1)

Parameter	Min	Max	Unit
Input Supply Voltage, EN	-0.3	20	V
LX Voltages	-0.3	20	V
LX Voltages (<10ns transient)	-5	22	V
FB Voltage	-0.3	6	V
BS Voltage	-0.3	26	V
BS to LX Voltage	-0.3	6	V
Storage Temperature Range	-65	150	°C
Junction Temperature (Note 2)	160		°C
Power Dissipation	1500		mW
Lead Temperature (Soldering, 10s)	260		°C

Package / Order Information



DFN1.6x1.6-6(Top View)

Top Mark: SG3H/xxx (SG3H: Device Code, xxx: Inside Code)

Part Number	Package	Top Mark	Quantity/ Reel
STI3453FIN	SOT563	SG3H xxx	3000

STI3453FIN devices are Pb-free and RoHS compliant.

Pin Functions

Pin	Name	Function
1	VIN	Power Supply Pin
2	LX	Switching Pin
3	GND	Ground
4	BS	Bootstrap. A capacitor connected between LX and BS pins is required to form a floating supply across the high-side switch driver.
5	EN	Drive this pin to a logic-high to enable the IC. Drive to a logic-low to disable the IC and enter micro-power shutdown mode. Do not leave EN pin floating.
6	FB	Output Voltage feedback input. Connect FB to the center point of the external resistor divider.

ESD Rating

Items	Description	Value	Unit
V_{ESD_HBM}	Human Body Model for all pins	±2000	V
V_{ESD_CDM}	Charged Device Model for all pins	±1000	V

JEDEC specification JS-001

Recommended Operating Conditions

Items	Description	Min	Max	Unit
V_{IN}	Input Voltage Range	4.5	18	V
T_J	Operating Temperature Range	-40	125	°C

Thermal Resistance (Note3)

Items	Description	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	105	°C/W
θ_{JC}	Junction-to-case(top) thermal resistance	51	°C/W
ψJC	Junction-to-case(top) characterization parameter	3.2	°C/W

Electrical Characteristics

V_{IN}=12V, V_{OUT}=1.2V, T_A = 25°C, unless otherwise noted.

Parameter	Conditions	Min	Typ.	Max	Unit
Input Voltage Range		4.5		18	V
OVP Threshold		18.5	19	19.5	V
UVLO Rising Threshold		3.8	4.1	4.4	V
UVLO Hysteresis			0.4		V
Quiescent Current	V_{EN}=2.0V, I_{OUT}=0A, V_{FB}=V_{REF} x 105%		300		μA
Shutdown Current	V_{IN}=12V, EN=0V		5	10	μA
Regulated Feedback Voltage	T_A=25°C, V_{IN}=12V	0.591	0.600	0.609	V
High-Side Switch On-Resistance			80		mΩ
Low-Side Switch On-Resistance			40		mΩ
High-Side Switch Leakage Current	V_{EN}=0V, V_{LX}=0V	1		10	μA
Switch Valley Current Limit	Minimum Duty Cycle	3.6	4.2	4.8	A
High-side Switch Peak Current Limit			4.8		A
Low-side Switch Negative Current Limit			-3		A
On Time	V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=1A	85	100	115	ns
Oscillation Frequency		900	1000	1100	kHz
Switching Frequency in Maximum Duty Cycle	V_{IN}=12V, V_{FB}=0.5V		130		kHz
Maximum Duty Cycle	V_{IN}=12V, V_{FB}=0.5V	95	97.5		%
Minimum On-Time			60		ns
Minimum Off-Time			160		ns
Output UV Falling Threshold	Reference to V_{FB}		54%		V_{FB}
Soft Start Time	V_{OUT} 10% to 90%	0.5	0.8	1.1	ms
Hiccup on Time (Note 4)			3		ms
Hiccup Time Before Restart			43		ms
EN Rising Threshold		0.98	1.1	1.22	V
EN Falling Threshold		0.92	0.99	1.06	V
EN Hysteresis			110		mV
Thermal Shutdown Threshold (Note 4)			165		°C
Thermal Shutdown Hysteresis (Note 4)			30		°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + P_D \times \theta_{JA}$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D(MAX)} = (T_{J(MAX)}-T_A)/\theta_{JA}$.

Note 3: Measured on JESD51-7, 4-layer PCB.

Note 4: Guaranteed by design.

Block Diagram

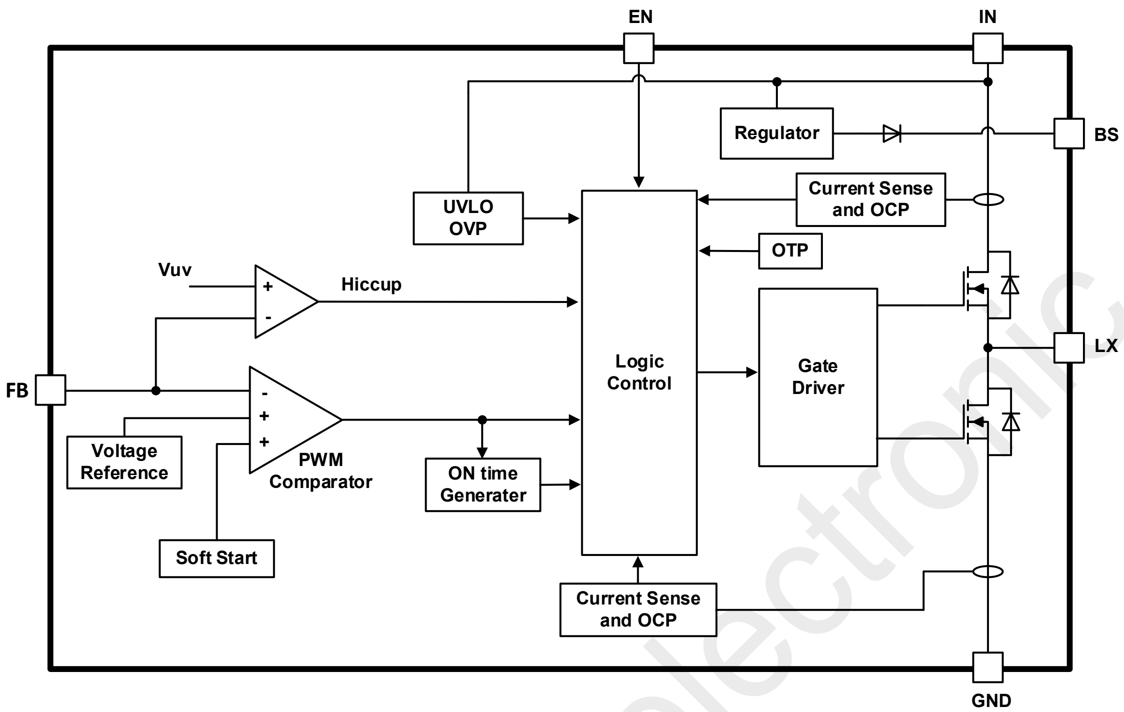


Figure 1. STI3453FIN Block Diagram

Operation Description

Overview

The STI3453FIN is an advanced constant on-time (COT) step down DC/DC converter with force PWM Operation mode that provides excellent transient response with no extra external compensation components. This device contains low resistance, high voltage high side and low side power MOSFETs, and operates at 1MHz operating frequency to ensure a compact, high efficiency design with excellent AC and DC performance.

Maximum Duty Cycle

STI3453FIN is based on COT control mode and it has minimum off time. The maximum duty cycle is limited by minimum off time and maximum on time. STI3453FIN has a mechanism to decrease the switching frequency by increasing on-time, when the input voltage of STI3453FIN is close to output voltage and minimum off time is reached, the high side switch on time extends, and the frequency drops. With this function, the STI3453FIN is able to 97.5% maximum duty cycle and 130kHz switching frequency typically.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 0.6V(0%-100%). When it is lower than the internal FB reference (V_{REF}), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than V_{REF}, V_{REF} regains control. The SS time is internally fixed to 1.0ms typically (V_{OUT} 10% to 90% is internally fixed to 0.8ms typically).

Over-Current-Protection and Short Circuits Protection

The STI3453FIN has cycle-by-cycle current limit on both high-side MOSFET and low-side MOSFET. During every switching cycle and high side MOSFET is turned on, when the peak current of high-side MOSFET is larger than high-side MOSFET peak current limit the high-side MOSFET is turned off and low-side MOSFET is turned on immediately. When the low-side MOSFET valley current value is larger than the valley current limit during low side MOSFET on state, the device enters into valley over current protection mode and low side MOSFET keeps on state until inductor current drops down to the value equal or lower than the valley current limit, and then on time pulse could be generated and high side MOSFET could turn on again.

If the output is short to GND and the output voltage drop until feedback voltage V_{FB} is below the output under-voltage V_{UV} threshold which is typically 54% of V_{REF}, STI3453FIN enters into hiccup mode to periodically disable and restart switching operation. The hiccup mode helps to reduce power dissipation and thermal rise during output short condition. The period of STI3453FIN hiccup mode is typically 45ms.

Negative Current Limit

Low-side MOSFEET Negative Current Limit (NCL) is realized by monitoring the current following from LX to GND when Low-side MOSFET (LSFET) is turned on. When the current reaches negative current limit, the LSFET is turned off to limit the negative current.

STI3453FIN work in FPWM mode. In order to prevent the Negative Current Limit is triggered on light load operation the inductor valley current should be designed to higher than I_{LIM_NEG}, when the output of STI3453FIN have energy flowing backward from output side and drive feedback voltage start rise, its inductor current will increase negatively. STI3453FIN first releases the output backward energy to the input under internal control loop adjustment, and slows down the output voltage rise range. In this process, the inductor current continues to increases negatively. After triggering the NCL, STI3453FIN will turn off LSFET, and the HSFET is also controlled by internal control loop circuits. If the FB voltage is higher than the internal reference voltage, the HSFET is turned off by internal control loop circuits. The continuous output energy flowing backward will sustain feedback voltage higher than reference voltage, leading to the internal control loop of STI3453FIN keeps HSFET and LSFET closing, once output voltage drops down to target voltage, the STI3453FIN will return to normal switching operation immediately.

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts switching operation. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The floating driver is not subject to this shutdown command.

Thermal Shutdown

The STI3453FIN implements a thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature rises to 165°C (typical), the device shuts down immediately. The STI3453FIN releases thermal shutdown when the junction temperature of the device is reduced to 135°C typically.

Application Information

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). Choose R1 to be around 40.2kΩ for optimal transient response. R2 is then given by:

Table 1: Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{FB} (pF)	L (μH)
5	40.2	5.49	33	2.2
3.3	40.2	8.87	33	2.2
2.5	40.2	12.7	33	2.2
1.8	40.2	20	33	1.5
1.5	40.2	26.7	33	1.5
1.2	40.2	40.2	33	1.0
1	40.2	60.4	33	1.0
0.8	20.5	60.4	33	1.0

$$R_2 = \frac{R_1}{V_{out}/V_{FB} - 1}$$

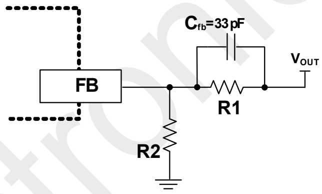


Figure 2. Feedback Network

A C_{fb} capacitor paralleling with high side divider resistor R1 can be used to improve load transient performance. It adds a zero in the frequency 1/2π·R1·Cfb to increase bandwidth of the system. 33pF C_{fb} is sufficient in most application and increasing C_{fb} capacitance can reduce output ripple value in fast transient load current condition.

Selecting the Inductor

A DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. Inductance value is related to inductor ripple current value, input voltage, output voltage setting and switching frequency. The inductor value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current. STI3453FIN is force PWM operation mode. In dull load condition, the average inductor current is zero and valley inductor current is $-\Delta I_L/2$. the minus current valley is limited to around -3A, so the inductor ripple current ΔI_L should be smaller than 6A, and the minimum inductance value is limited. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Selecting the Output Capacitor

The output capacitors (Co1 and Co2) are required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times \left[R_{ESR} + \frac{1}{8 \times f_S \times C_2}\right]$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^{\,2} \times L \times C_2} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The STI3453FIN can be optimized for a wide range of capacitance and ESR values.

PCB Layout Guide

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines and take Figure 3 for reference.

1) Keep the path of switching current short and minimize the loop area formed by Input capacitor, IN pin and GND.

2) Bypass ceramic capacitors are suggested to be put close to the IN Pin.

3) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the chip as possible.

4) VOUT, LX away from sensitive analog areas such as FB.

5) Connect IN, LX, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

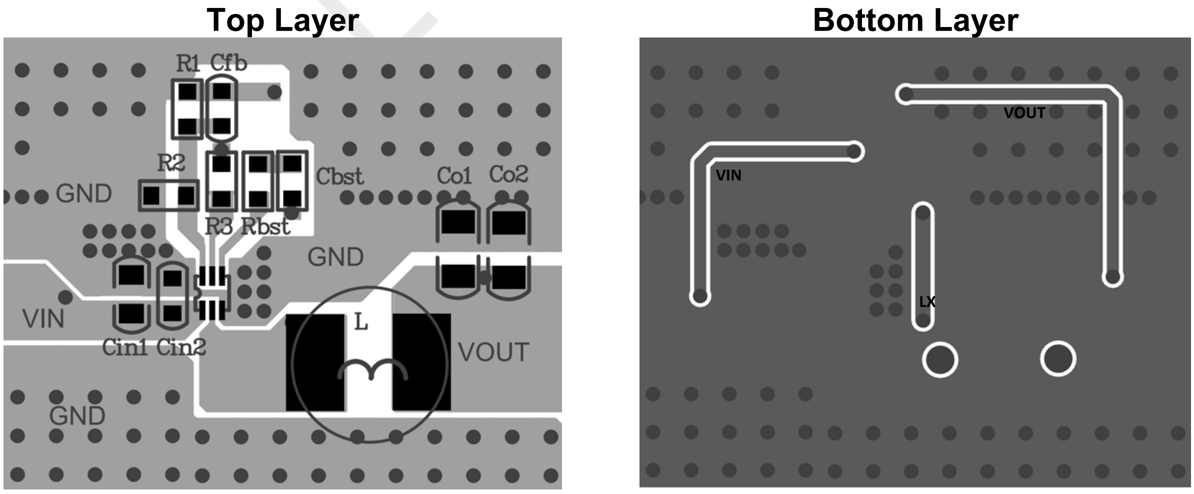


Figure 3. Sample of PCB Layout

Typical Application Circuits

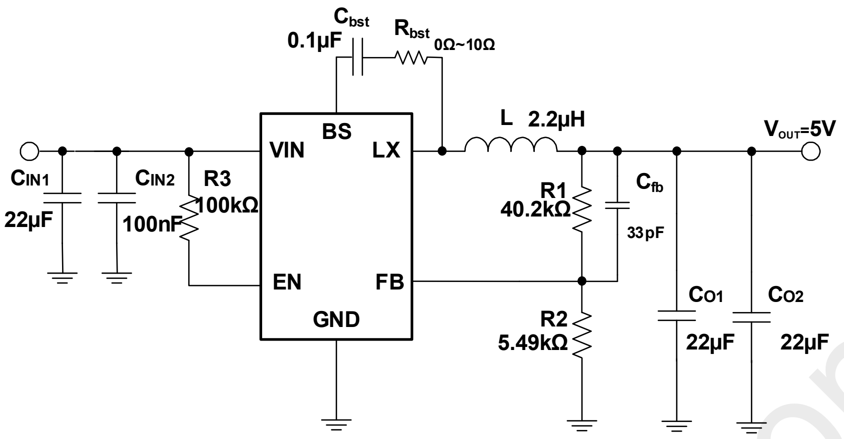


Figure 4. 12V$_{IN}$, 5V Output

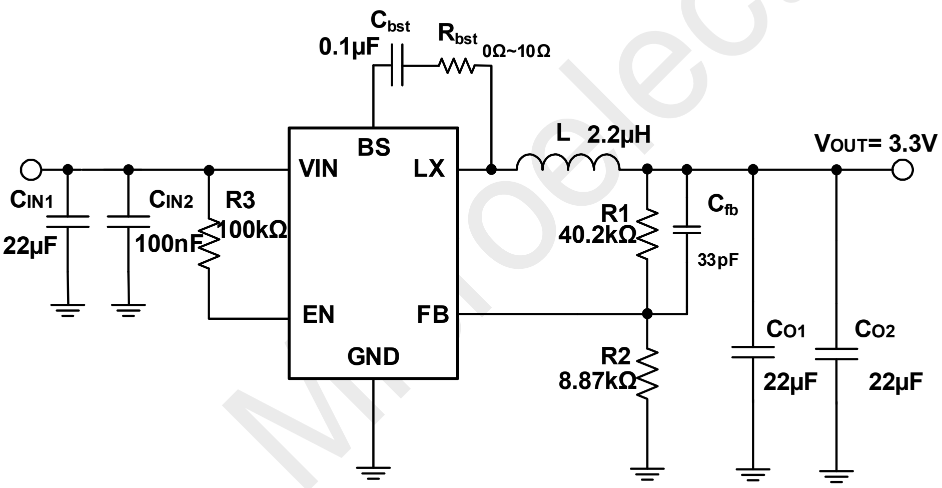


Figure 5. 12V$_{IN}$, 3.3V Output

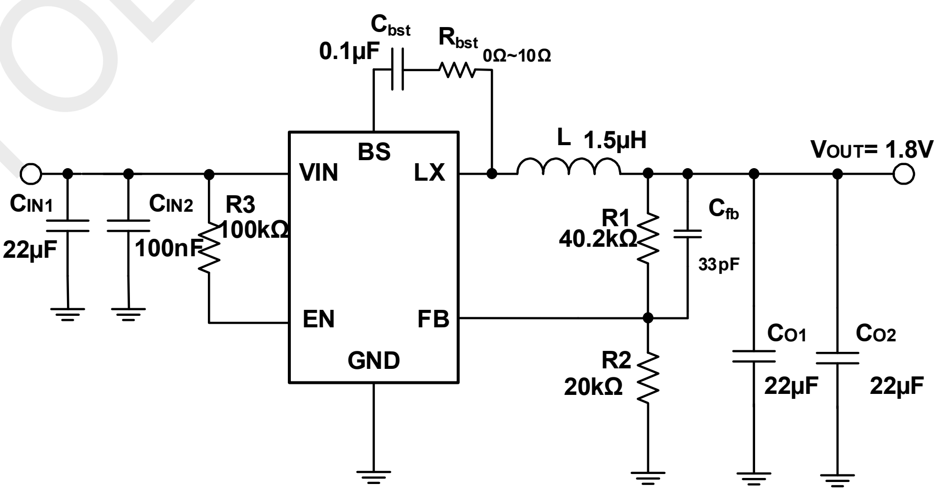


Figure 6. 12V$_{IN}$, 1.8V Output

Typical Application Circuits(continued)

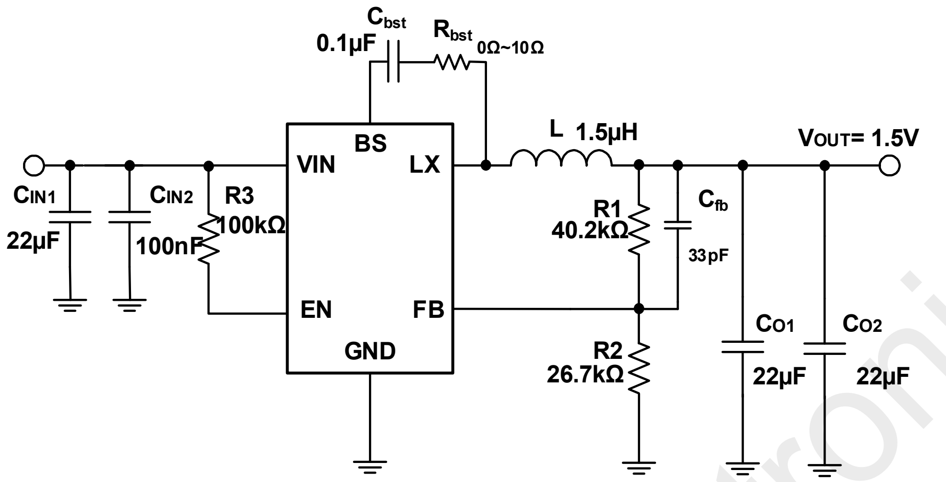


Figure 7. 12V$_{IN}$, 1.5V Output

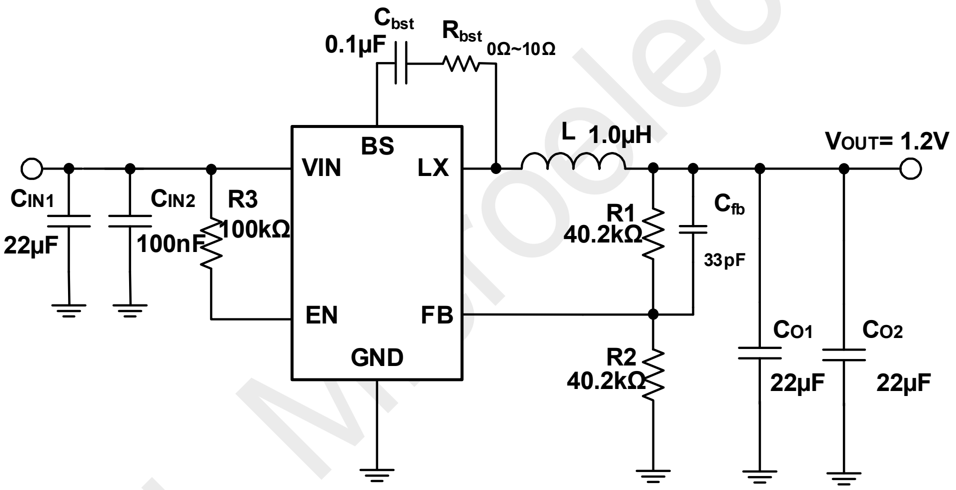


Figure 8. 12V$_{IN}$, 1.2V Output

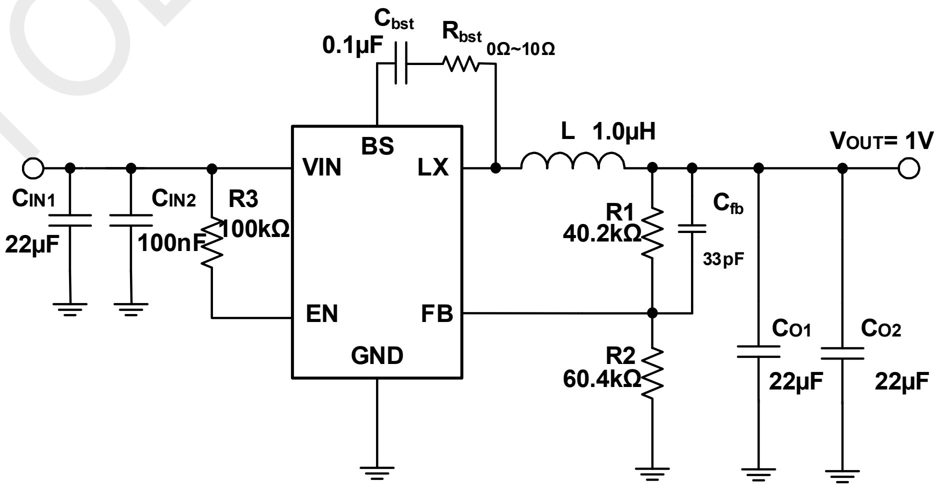
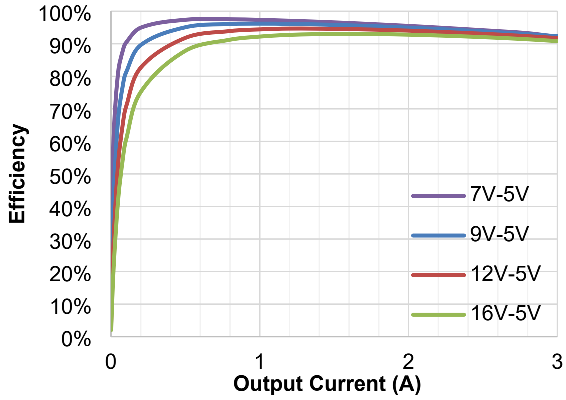


Figure 9. 12V$_{IN}$, 1V Output

Typical Performance Characteristics

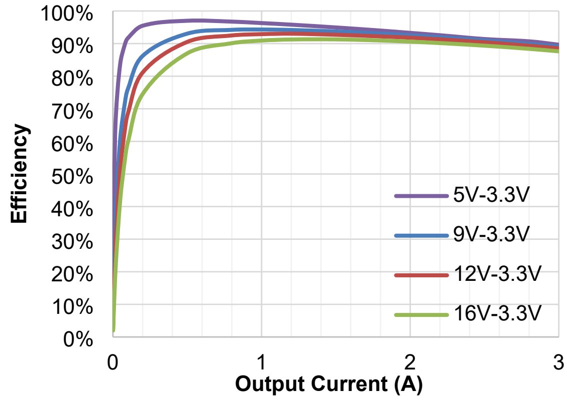
Efficiency at V_{OUT} = 5V

V_{OUT} =5V, L=2.2μH, DCR=20mΩ



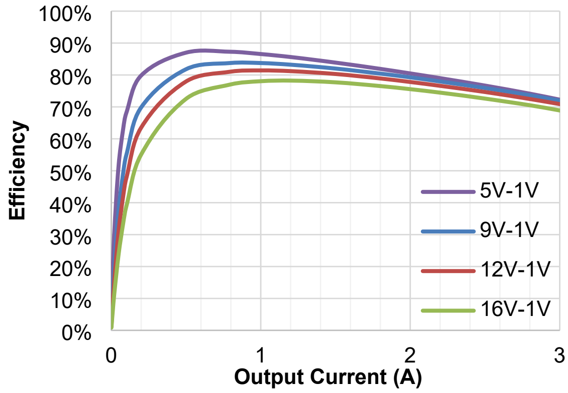
Efficiency at V_{OUT} = 3.3V

V_{OUT} =3.3V, L=2.2μH, DCR=20mΩ



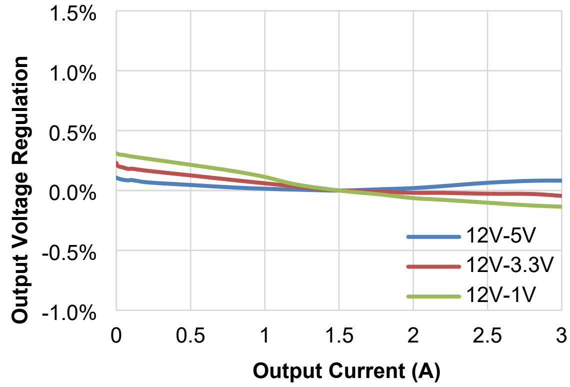
Efficiency at V_{OUT} = 1V

V_{OUT}=1V, L=1.0μH, DCR=20mΩ



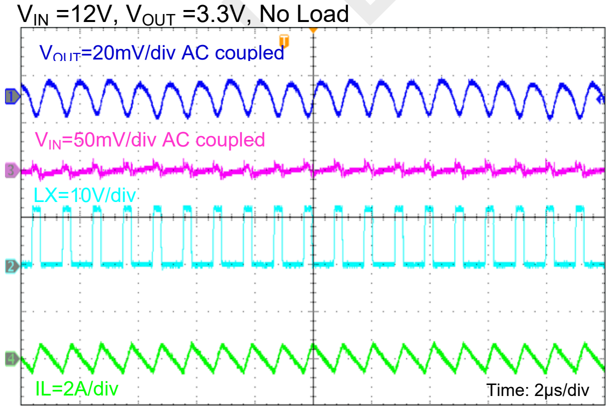
Load Regulation at V_{IN} = 12V

V_{IN}=12V, T_A=25°C



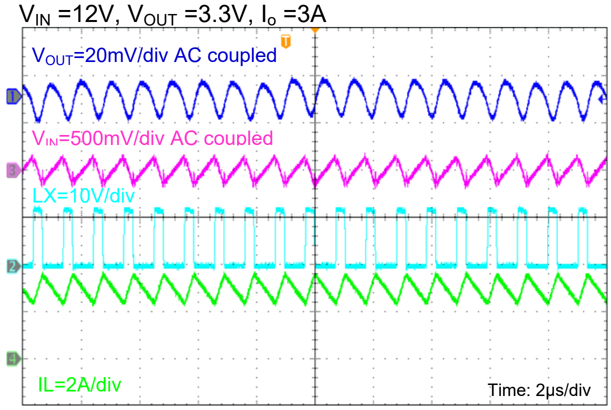
Steady State

V_{IN} =12V, V_{OUT} =3.3V, No Load



Steady State

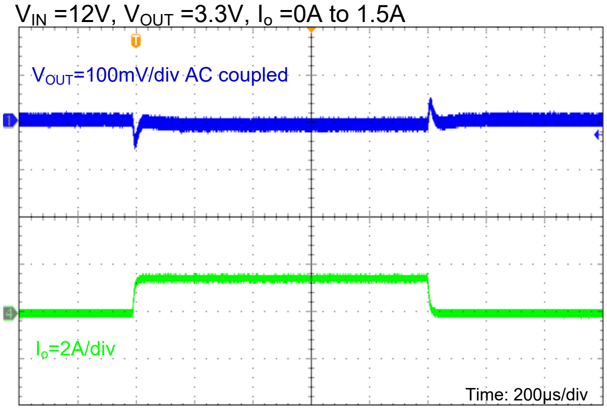
V_{IN} =12V, V_{OUT} =3.3V, I_o =3A



Typical Performance Characteristics (continued)

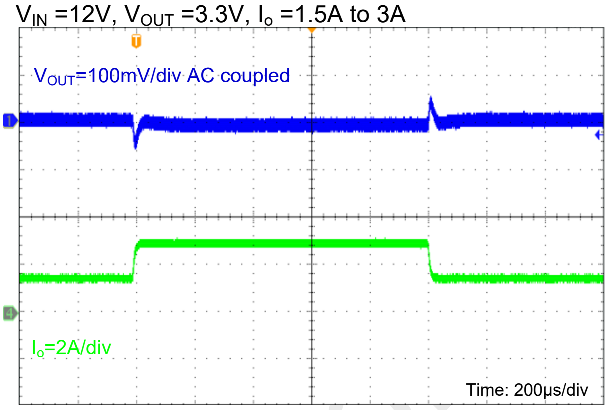
Load Transient

V_{IN} =12V, V_{OUT} =3.3V, I_o =0A to 1.5A



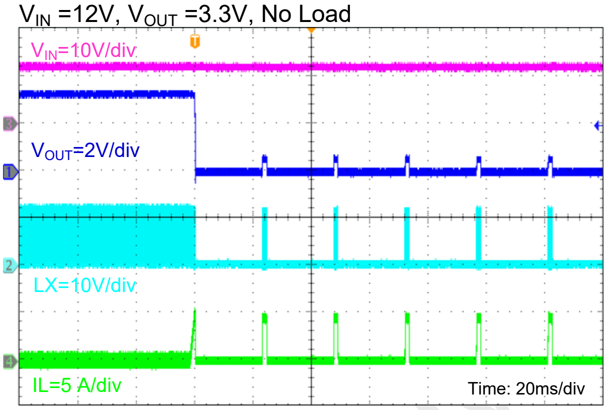
Load Transient

V_{IN} =12V, V_{OUT} =3.3V, I_o =1.5A to 3A



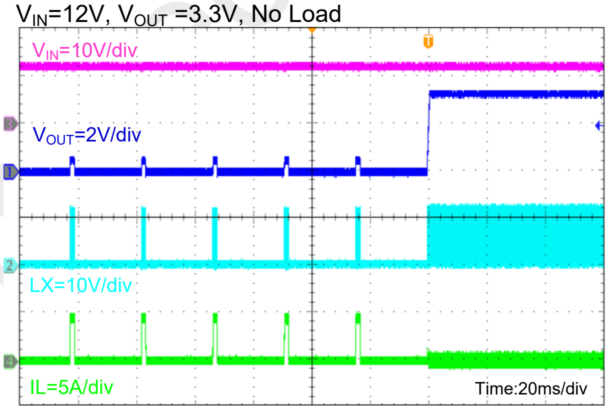
Output Short Entry

V_{IN} =12V, V_{OUT} =3.3V, No Load



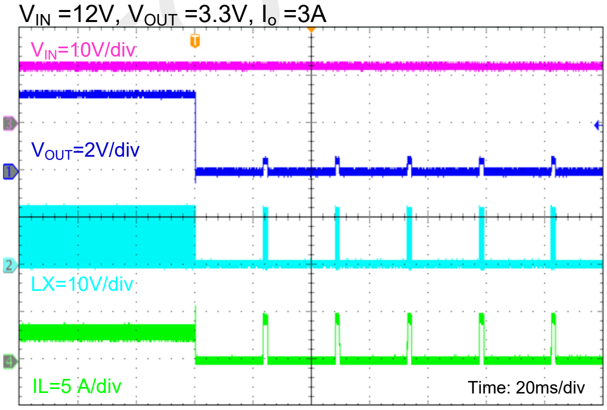
Output Short Recovery

V_{IN}=12V, V_{OUT} =3.3V, No Load



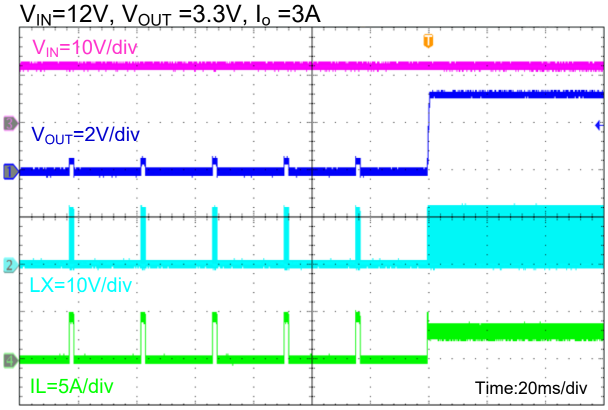
Output Short Entry

V_{IN} =12V, V_{OUT} =3.3V, I_o =3A



Output Short Recovery

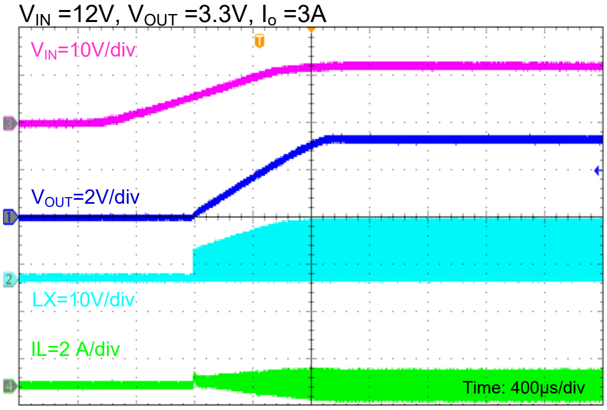
V_{IN}=12V, V_{OUT} =3.3V, I_o =3A



Typical Performance Characteristics (continued)

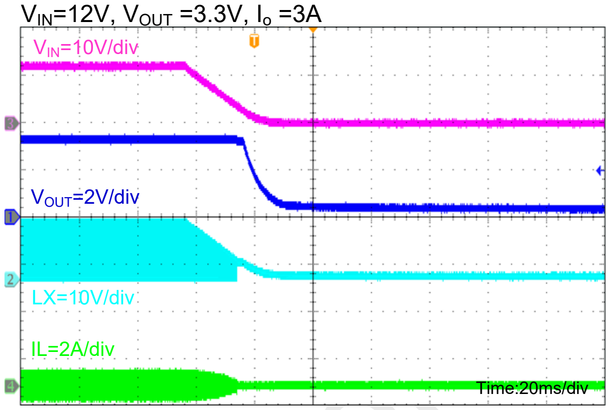
Input Power On

V_{IN} =12V, V_{OUT} =3.3V, I_o =3A



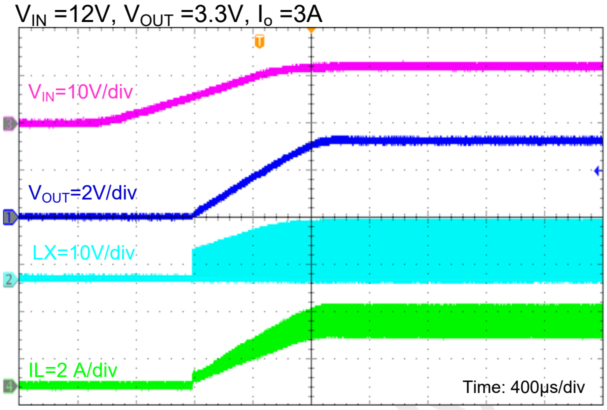
Input Power Down

V_{IN}=12V, V_{OUT} =3.3V, I_o =3A



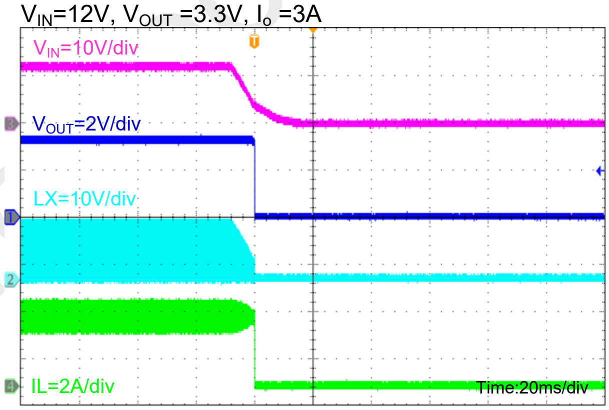
Input Power On

V_{IN} =12V, V_{OUT} =3.3V, I_o =3A



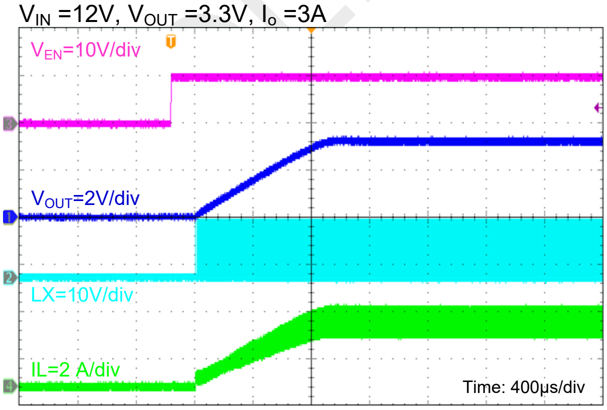
Input Power Down

V_{IN}=12V, V_{OUT} =3.3V, I_o =3A



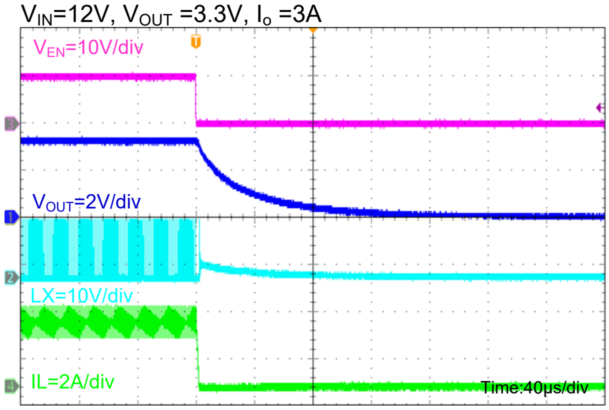
EN Enable Power On

V_{IN} =12V, V_{OUT} =3.3V, I_o =3A



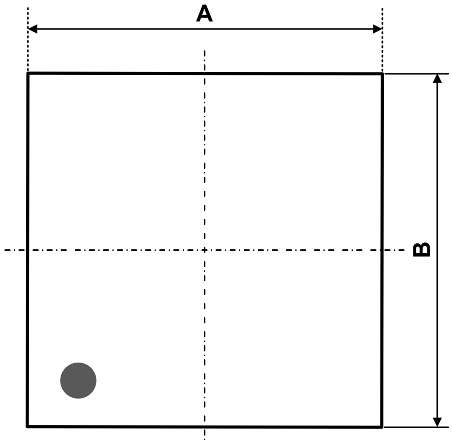
EN Disable Power down

V_{IN}=12V, V_{OUT} =3.3V, I_o =3A

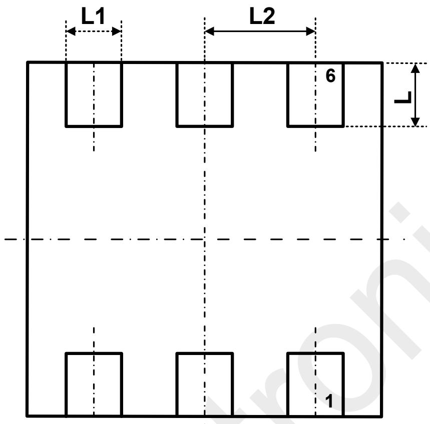


Package Information

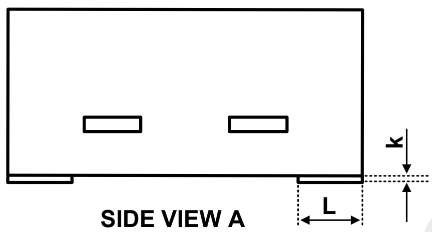
DFN1.6x1.6



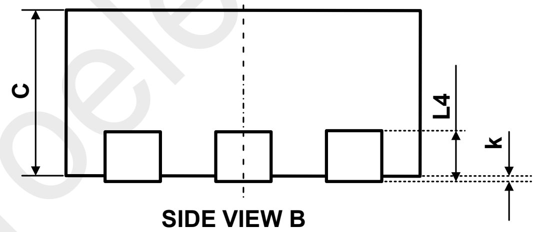
TOP VIEW



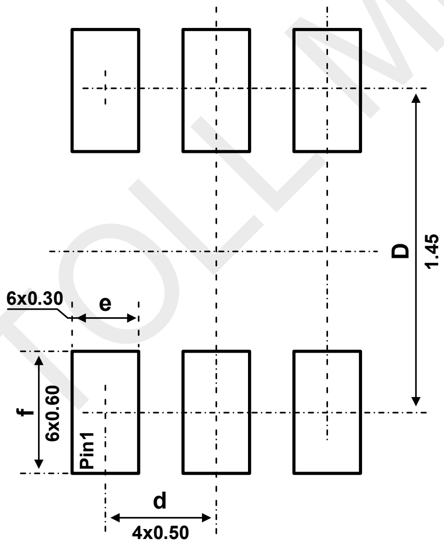
BOTTOM VIEW



SIDE VIEW A



SIDE VIEW B



RECOMMENDED PAD LAYOUT

Unit: mm

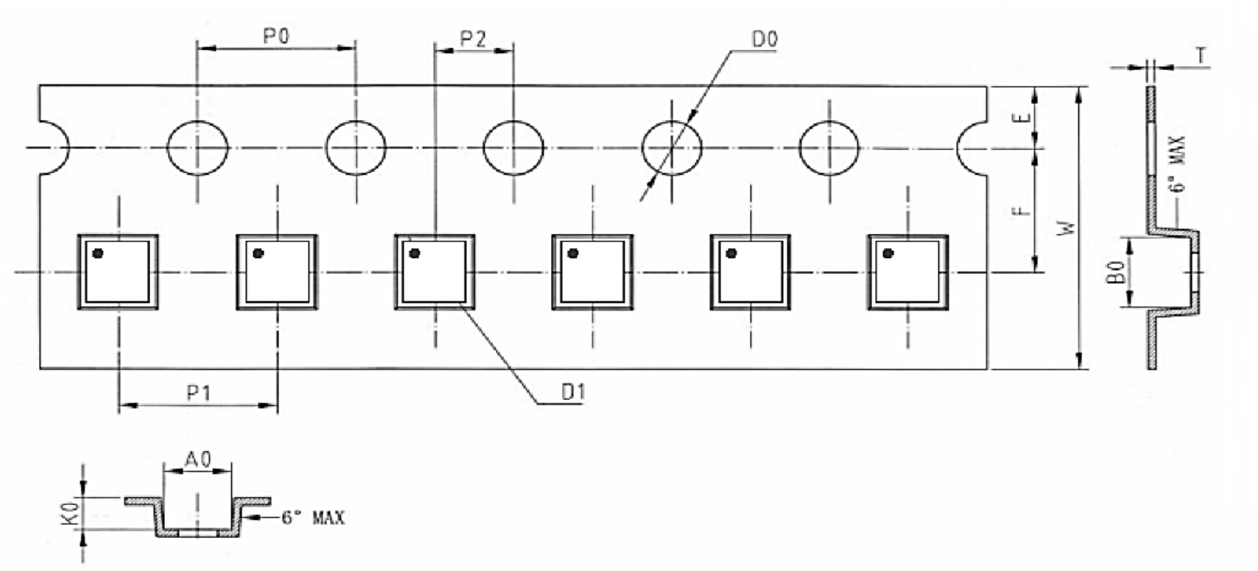
Symbol	Min.	Typ.	Max.
A	1.50	1.60	1.65
B	1.50	1.60	1.65
C	0.70	0.75	0.80
L	0.230	0.275	0.330
L1	0.20	0.25	0.30
L2	-	0.50	-
L4	-	0.203	-
k	0.00	0.02	0.05
D	-	1.45	-
d	-	0.50	-
e	-	0.30	-
f	-	0.60	-

Note:

1) All dimensions are in millimeters.
2) Package length does not include mold flash, protrusion or gate burr.
3) Package width does not include inter lead flash or protrusion.

Package Information

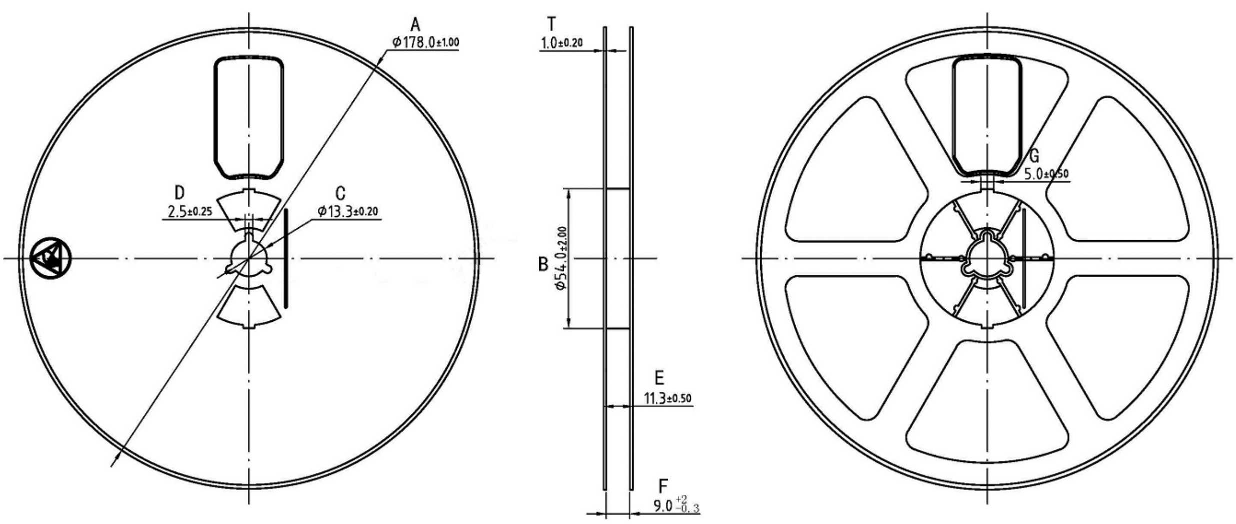
Tape Dimensions: DFN1.6x1.6



Unit: mm

Symbol	A0	B0	K0	P0	P1	P2
Spec	1.76±0.05	1.78±0.05	1.00±0.05	4.00±0.10	4.00±0.10	2.00±0.05
Symbol	T	E	F	D0	D1	W
Spec	0.20±0.02	1.75±0.05	3.5±0.05	1.55±0.05	1.10±0.10	8.00±0.10

Reel Dimensions: DFN1.6x1.6



Note:

1) All Dimensions are in Millimeter
2) Quantity of Units per Reel is 3000
3) MSL level is level 3.

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