



## PRODUCT DATA SHEET



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**Datasheet**



**Resources**

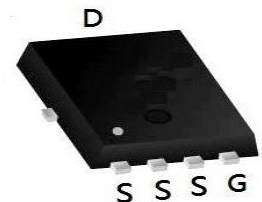


**Samples**

Please note: Please check the JINGAO Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at [www.jg-semi.cn](http://www.jg-semi.cn). Please email any questions regarding the system integration to [JINGAO\\_questions@jgsemi.com](mailto:JINGAO_questions@jgsemi.com).

## Product Summary

BVDSS	RDSON	ID
40V	1.1mΩ	225A



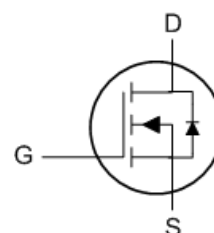
PDFN5060-8L

## Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$

## Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications



## ■ Absolute Maximum Ratings ( $T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	40	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current (Silicon limited)		$I_D$	225	A
Drain Current <sup>A</sup>	$T_c=25^{\circ}\text{C}$	$I_D$	130	A
	$T_c=100^{\circ}\text{C}$		82	
Pulsed Drain Current <sup>B</sup>		$I_{DM}$	390	A
Avalanche energy <sup>C</sup>		$E_{AS}$	450	mJ
Total Power Dissipation <sup>D</sup>		$P_D$	114	W
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	1.1	$^{\circ}\text{C}/\text{W}$
Thermal Resistance Junction-to-Ambient <sup>E</sup>		$R_{\theta JA}$	20	
Junction and Storage Temperature Range		$T_J, T_{STG}$	$-55 \sim +150$	$^{\circ}\text{C}$

**■ Electrical Characteristics** ( $T_J=25^{\circ}\text{C}$  unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	40	48		V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=40V, V_{GS}=0V$			1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}= \pm 20V, V_{DS}=0V$			$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.8	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$		1.1	1.4	m $\Omega$
		$V_{GS}=4.5V, I_D=20A$		1.7	2.3	
Gate Resistance	$R_g$	$V_{GS}=0V, V_{DS}$ Open, $f=1MHz$		2.7		$\Omega$
Maximum Body-Diode Continuous Current	$I_S$				100	A
Dynamic Parameters						
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V, f=300KHZ$		8300		pF
Output Capacitance	$C_{oss}$			1510		
Reverse Transfer Capacitance	$C_{rss}$			130		
Switching Parameters						
Total Gate Charge	$Q_g$	$V_{GS}=10V, V_{DS}=32V, I_D=20A$		127		nC
Gate-Source Charge	$Q_{gs}$			35		
Gate-Drain Charge	$Q_{gd}$			26		
Reverse Recovery Chrage	$Q_{rr}$	$I_F=25A, di/dt=100A/us$		163		ns
Reverse Recovery Time	$t_{rr}$			100		
Turn-on Delay Time	$t_{d(on)}$	$V_{GS}=10V, V_{DD}=20V, I_D=25A$ $R_{GEN}=2\Omega$		22.5		
Turn-on Rise Time	$t_r$			6.7		
Turn-off Delay Time	$t_{d(off)}$			80.3		
Turn-off fall Time	$t_f$			26.9		

## ■ Typical Performance Characteristics

Figure.1 Typical Output Characteristics

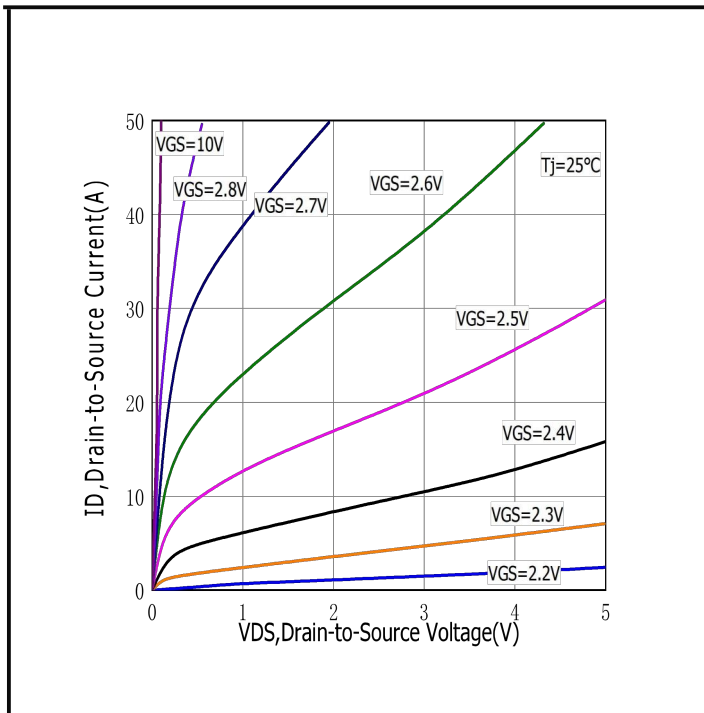


Figure.2 Typical Gate Charge vs Gate to Source Voltage

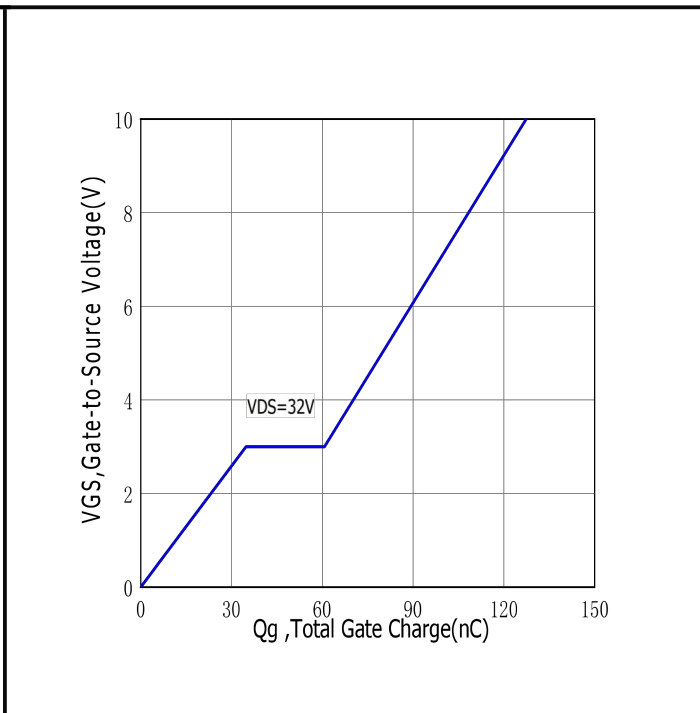


Figure.3 Typical Body Diode Transfer Characteristics

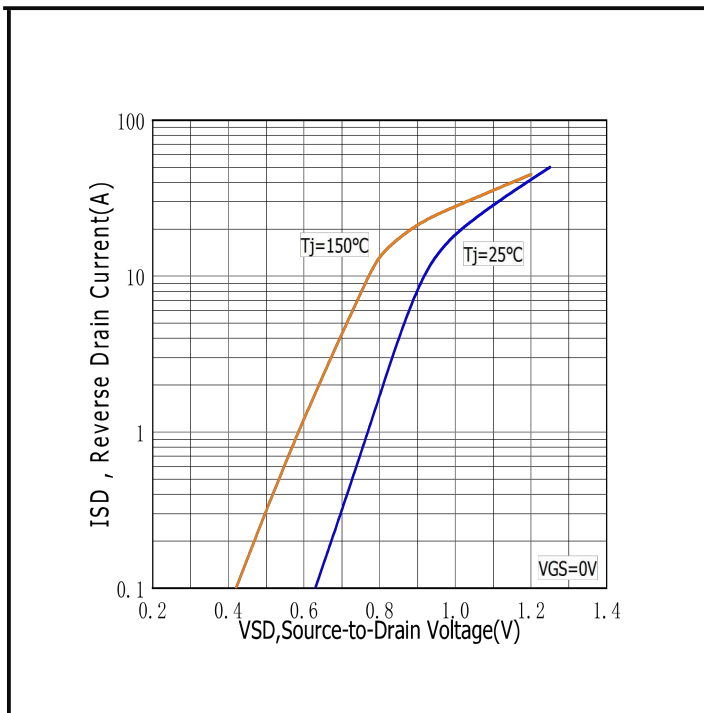


Figure.4 Typical Capacitance vs Drain to Source Voltage

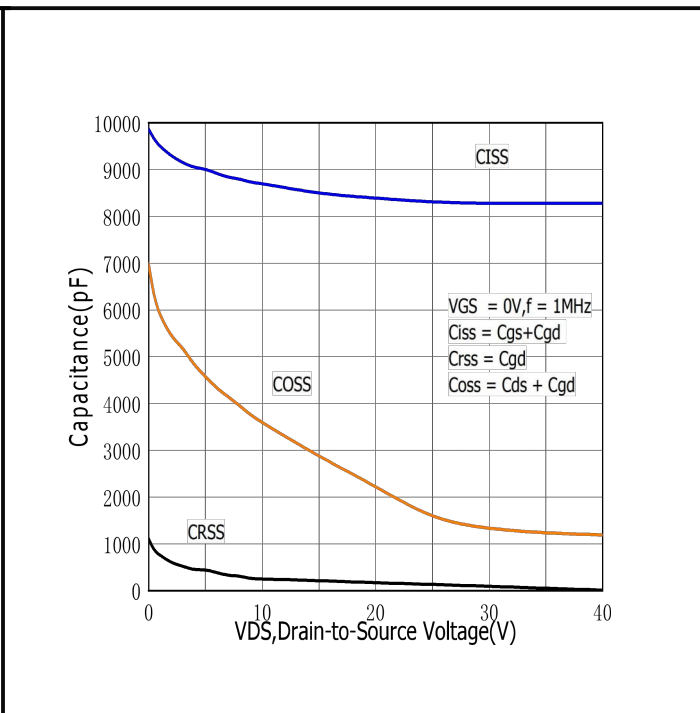


Figure.5 Typical Breakdown Voltage vs Junction Temperature

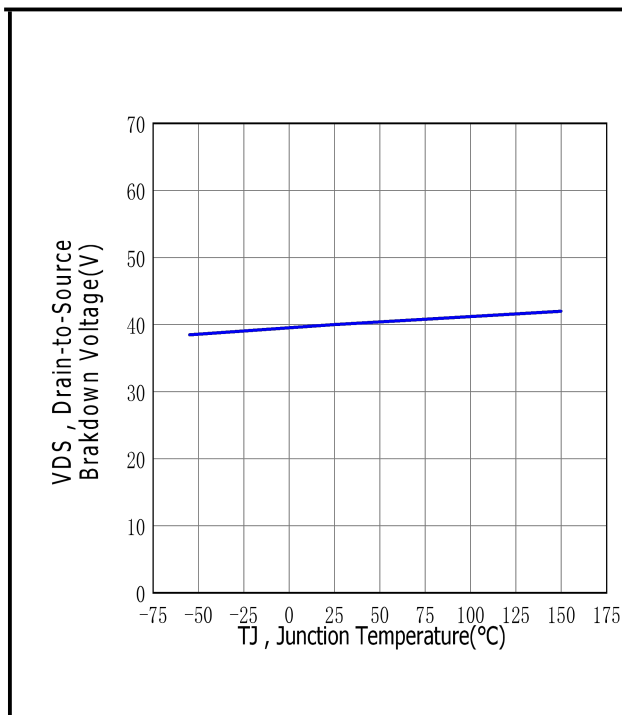


Figure.6 Typical Drain to Source on Resistance vs Junction Temperature

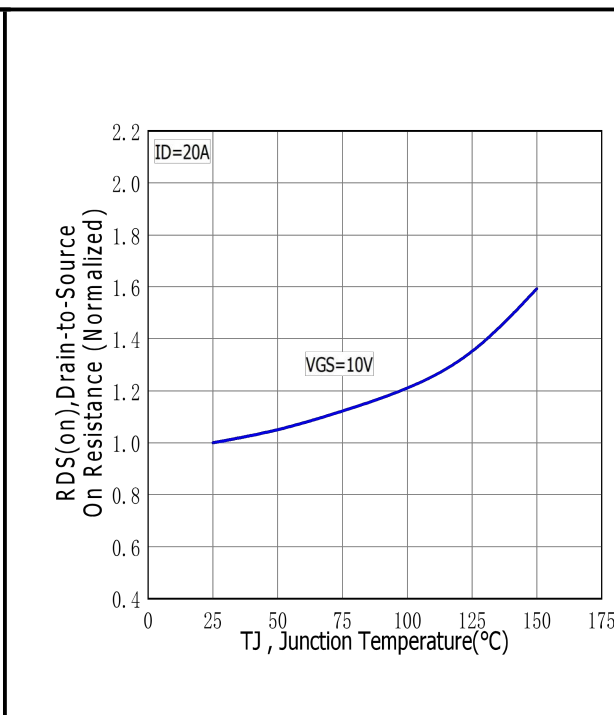


Figure.7 Maximum Forward Bias Safe Operating Area

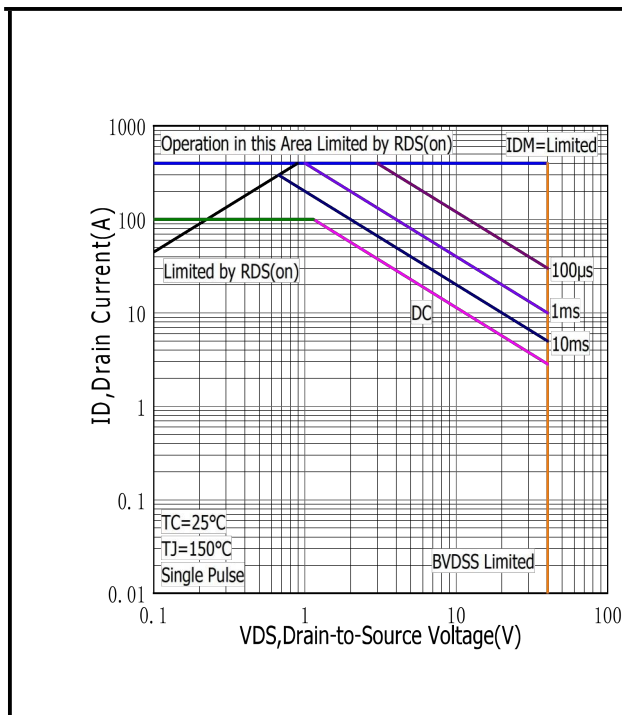
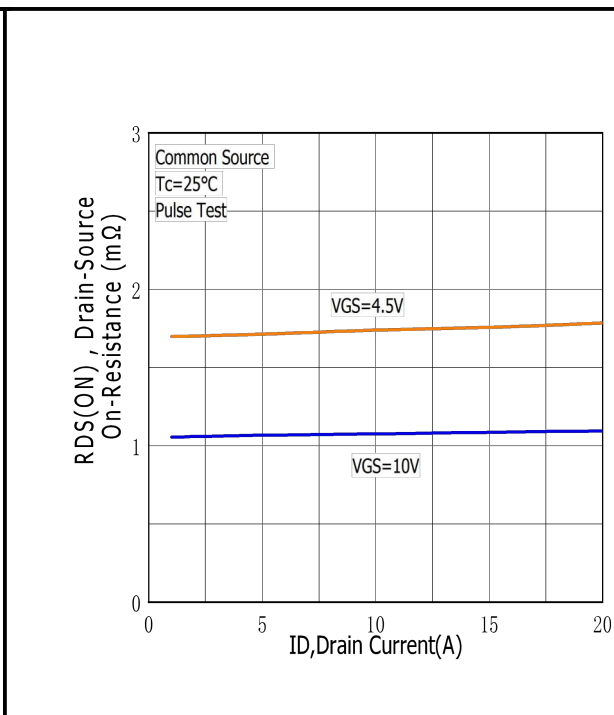


Figure.8 Typical Drain to Source ON Resistance vs Drain Current



## ■ Typical Performance Characteristics

Figure.9 Maximum EAS vs Channel Temperature

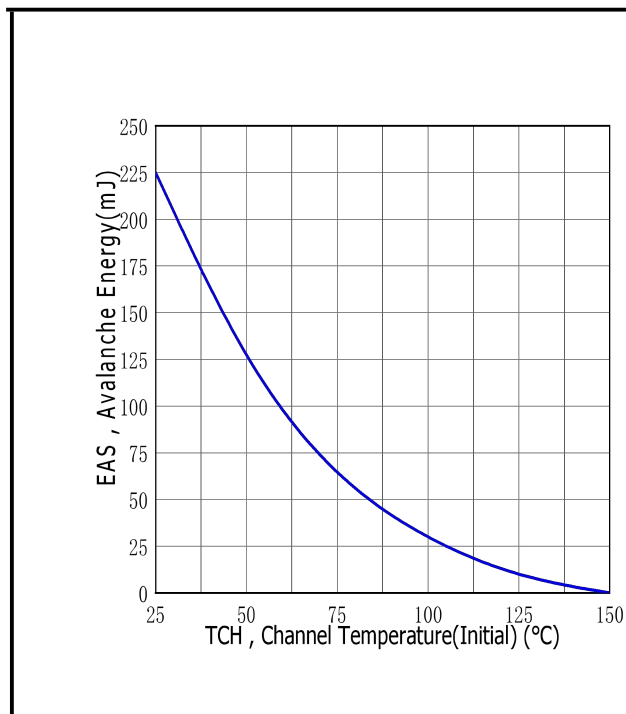


Figure.10 Typical Threshold Voltage vs Case Temperature

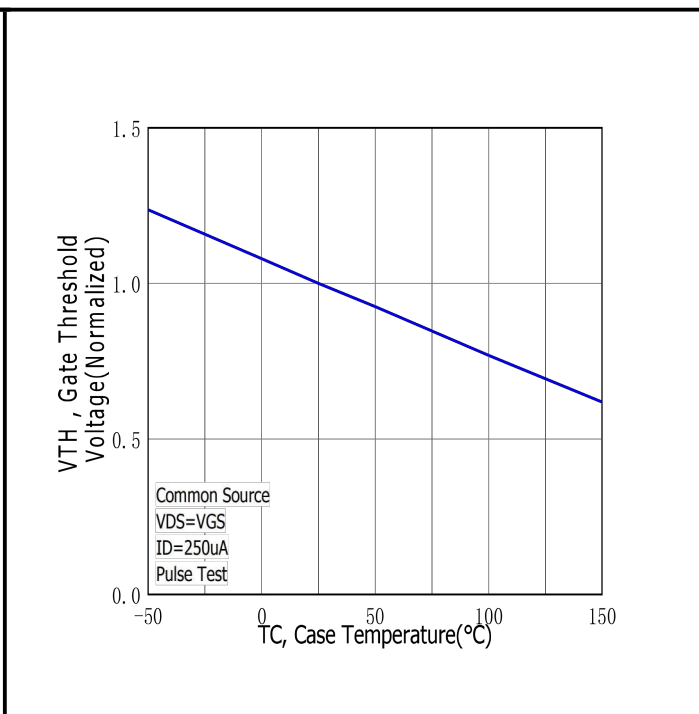


Figure.11 Typical Transfer Characteristics

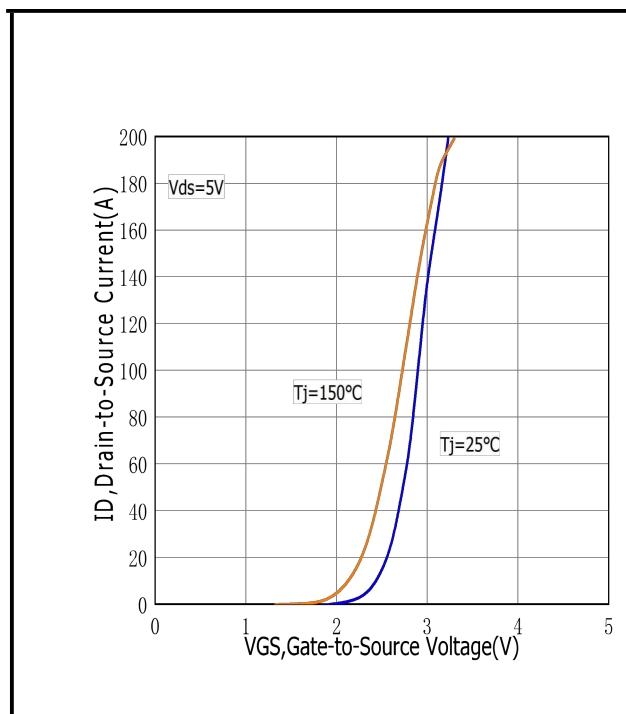


Figure.12 Maximum Power Dissipation vs Case Temperature

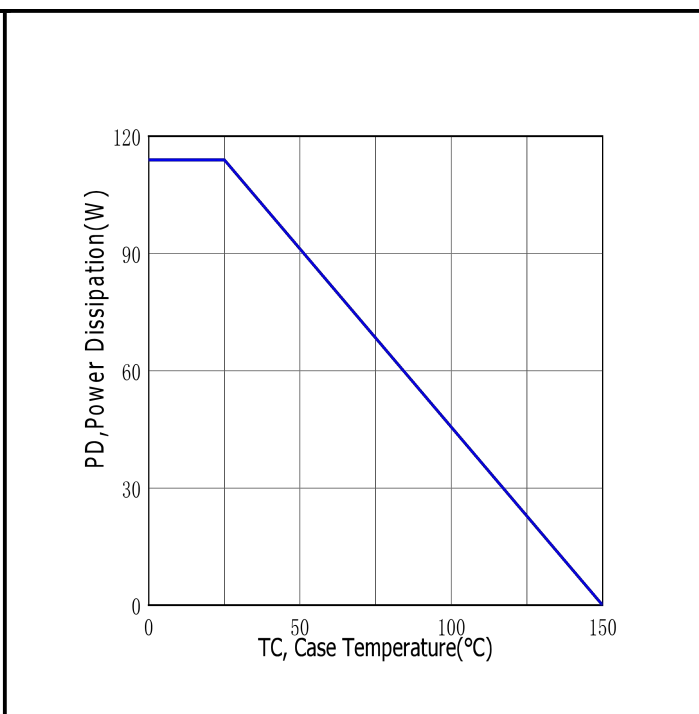
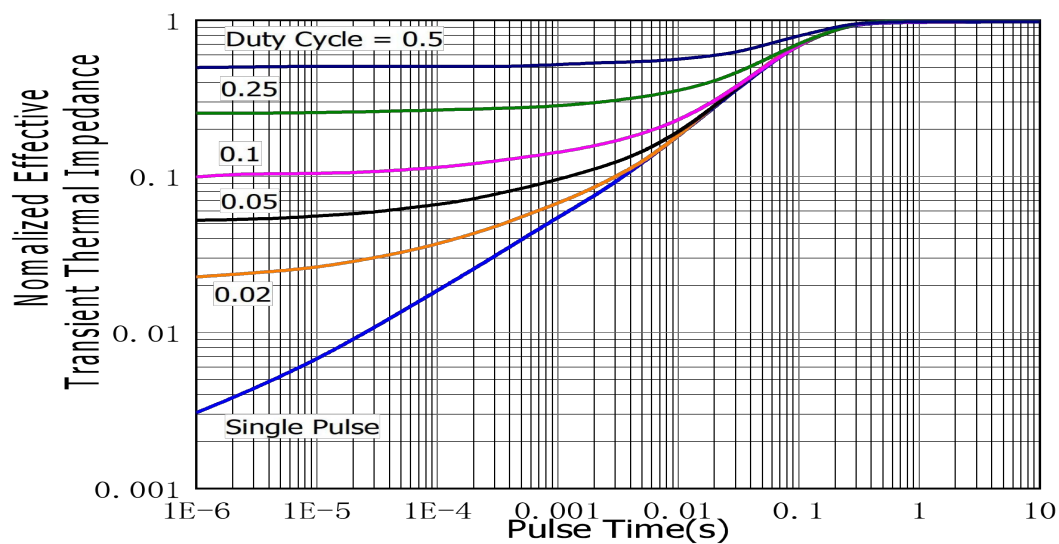


Figure.13 Maximum Effective Thermal Impedance , Junction to Case



## ■ Test circuits and waveforms

Figure A: Gate Charge Test Circuit & Waveforms

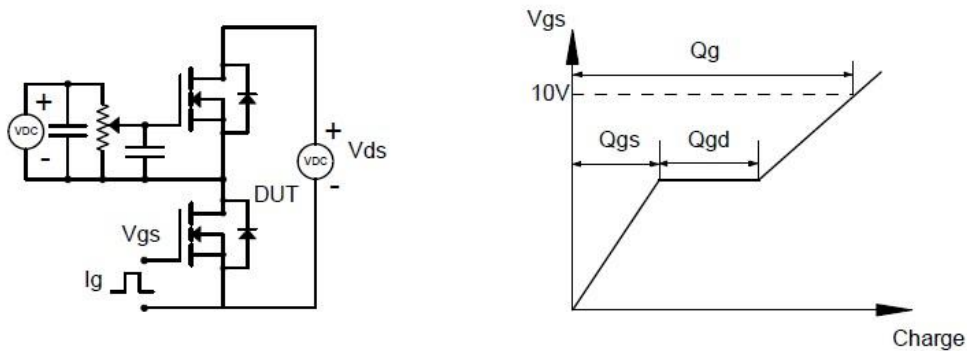


Figure B: Resistive Switching Test Circuit & Waveforms

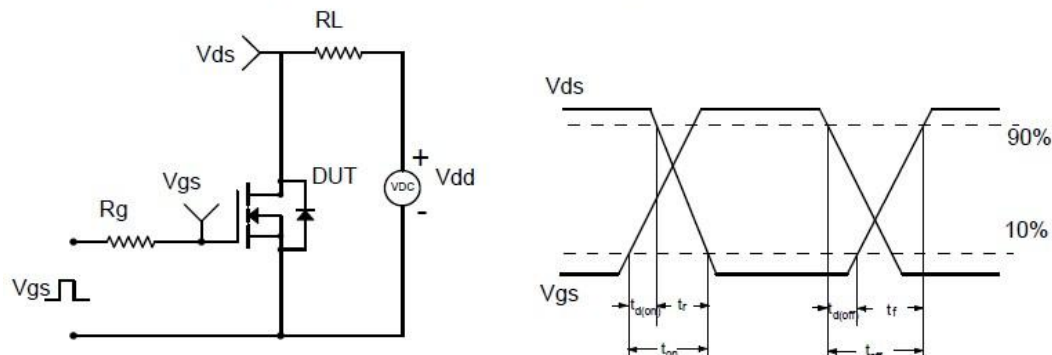


Figure C: Unclamped Inductive Switching (UIS) Test

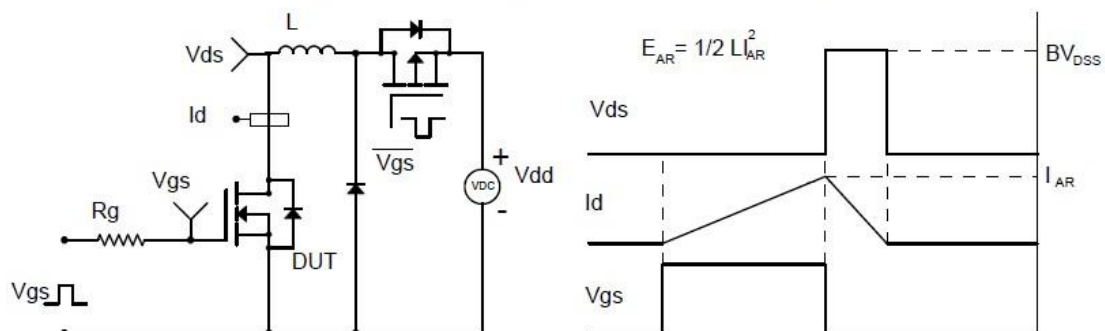
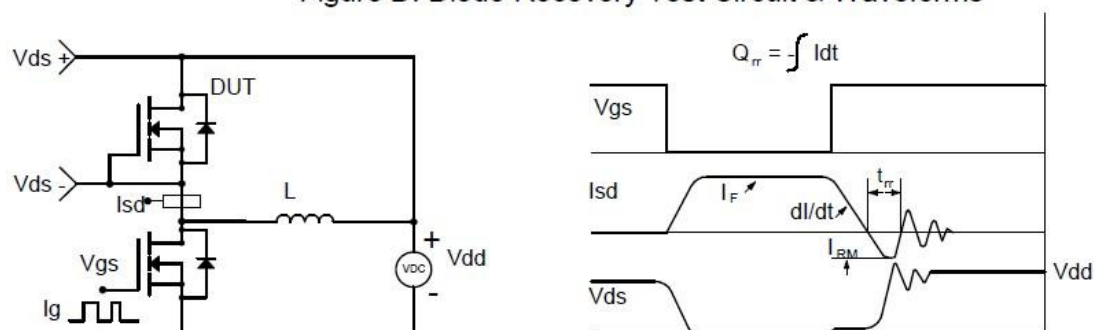
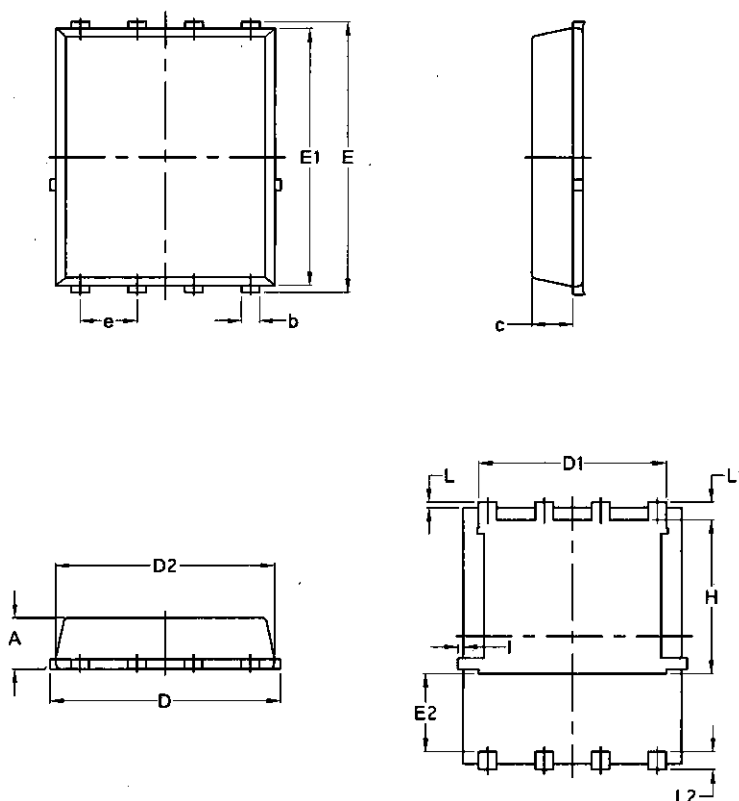


Figure D: Diode Recovery Test Circuit & Waveforms





## Package Mechanical Data-PDFN5060-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

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