Data Sheet V1.0

CLM9680BCPZ
14-Bit Dual Analog-to-Digital Converter

Description

The CLM9680BCPZ is a dual, 14-bit, 1.25 GSPS/1 GSPS/820 MSPS/ 500 MSPS Chiplon-to-digital converter (ADC). The device has an on-chip buffer and sample-and-hold circuit designed for low power, small size, and ease of use. This device is designed for sampling wide band width Chiplon signals of up to 2 GHz. The CLM9680BCPZ is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

The Chiplon input and clock signals are differential inputs. Each ADC data output is internally connected to two digital down- converters (DDCs). Each DDC consists of up to five cascaded signal processing stages: a 12-bit frequency translator (NCO), and four half-band decimation filters. The DDCs are bypassed by default.

In addition to the DDC blocks, the CLM9680BCPZ has several functions that simplify the automatic gain control (AGC) function in the communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

Users can configure the Subclass 1 JESD204B-based high speed serialized output in a variety of one-, two-, or four-lane configurations, depending on the DDC configuration and the acceptable lane rate of the receiving logic device. Multiple device synchronization is supported through the SYSREF± and SYNCINB± input pins.

The CLM9680BCPZ has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 1.8 V to 3.3 V capable, 3-wire SPI.

The CLM9680BCPZ is available in a Pb-free, 64-lead LFCSP and is specified over the −40°C to +85°C industrial temperature range. This product is protected by a U.S. patent.

Features

- JESD204B (Subclass 1) coded serial digital outputs
- 1.65 W total power per channel at 1 GSPS (default settings) SFDR at 1 GSPS = 85 dBFS at 340 MHz, 80 dBFS at 1 GHz SNR at 1 GSPS = 65.3 dBFS at 340 MHz (AIN = −1.0 dBFS),
- 60.5 dBFS at 1 GHz (AIN = −1.0 dBFS) ENOB = 10.8 bits at 10 MHz
- DNL = ±0.5 LSB
- INL = ±2.5 LSB
- Noise density = −154 dBFS/Hz at 1 GSPS 1.25 V, 2.5 V, and 3.3 V dc supply operation No missing codes
- Internal ADC voltage reference
- Flexible input range: 1.46 V p-p to 1.94 V p-p
- CLM9680BCPZ-1250: 1.58 V p-p nominal
- CLM9680BCPZ-1000 and CLM9680BCPZ-820: 1.70 V p-p nominal CLM9680BCPZ-500: 1.46 V p-p to 2.06 V p-p (2.06 V p-p nominal)
- Programmable termination impedance
- 400 Ω, 200 Ω, 100 Ω, and 50 Ω differential
- 2 GHz usable Chiplon input full power bandwidth

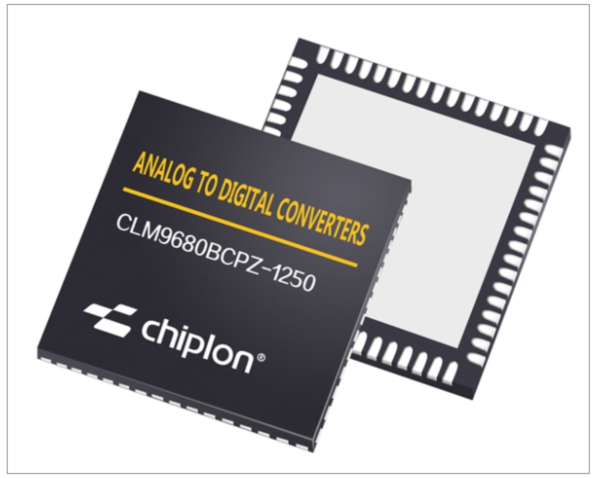
CAUTION! It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

- 95 dB channel isolation/crosstalk
- Amplitude detect bits for efficient AGC implementation 2 integrated wideband digital processors per channel
- 12-bit NCO, up to 4 half-band filters Differential clock input
- Integer clock divide by 1, 2, 4, or 8 Flexible JESD204B lane configurations Small signal dither

Applications

- Communications
- Diversity multiband, multimode digital receivers
- 3G/4G, TD-SCDMA, W-CDMA, GSM, LTE General-purpose software radios Ultrawideband satellite receivers Instrumentation
- Radars
- Signals intelligence (SIGINT)
- DOCSIS 3.0 CMTS upstream receive paths HFC digital reverse path receivers

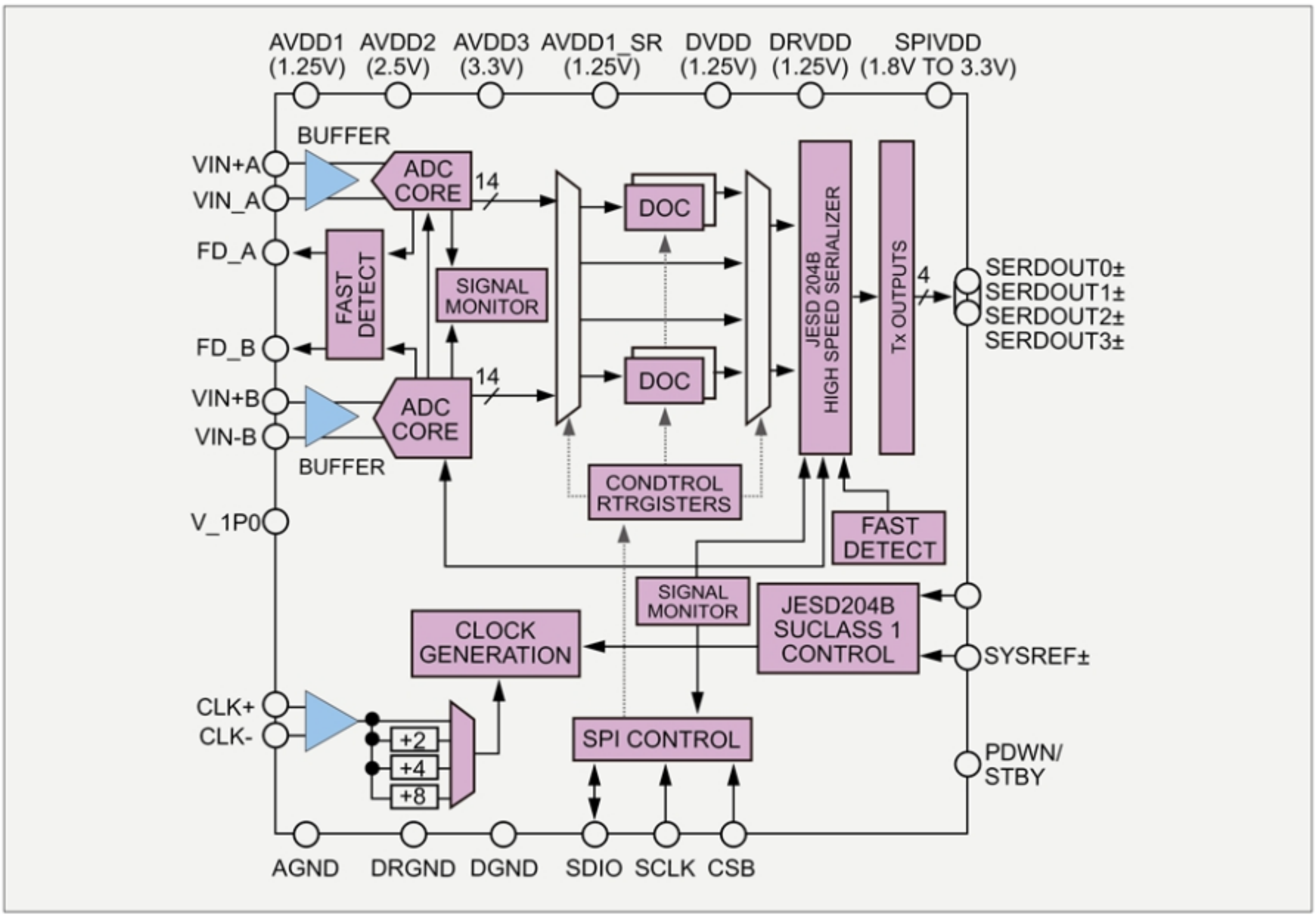
Prodect appearance



Ordering information

Part number	Description	Supplier Device Package	Package	Temperature Range	Packaging Quantity
CLM9680BCPZ-500	14-Bit Dual Analog-to-Digital Converter	LFCSP-64	Tray	–40°C to +85°C	750PCS
CLM9680BCPZ-820	14-Bit Dual Analog-to-Digital Converter	LFCSP-64	Tray	–40°C to +85°C	750PCS
CLM9680BCPZ-1000	14-Bit Dual Analog-to-Digital Converter	LFCSP-64	Tray	–40°C to +85°C	750PCS
CLM9680BCPZ-1250	14-Bit Dual Analog-to-Digital Converter	LFCSP-64	Tray	–40°C to +85°C	750PCS

Functional Block



CLM9680BCPZ

Abbreviation Listing

ADR	Address 地址
AL	Application Layer 应用层
BD	Bidirectional 双向
BGA	Ball Grid Array 球阵列封装
BHE	Bus High Enable 总线高电平使能
CMD	Command 命令
CS	Chip Select 片选
DC	Distributed Clock 集成分布时钟
DL	Data Link Layer 数据链接层
EMC	Electromagnetic Compatibility 电磁兼容性
EMI	Electromagnetic Interference 电磁干扰
EOF	End of Frame 帧结尾
EEPROM	Electrically Erasable Programmable read only memory 带电可擦可编程只读存储器
FMMU	Fieldbus Memory Management Unit 现场总线内存管理单元
GPI	General Purpose Input 通用数字量输入引脚
GPO	General Purpose Output 通用数字量输出引脚
I	Input 输入
I/O	Input or Output 输入或者输出
I2C	Inter-Intergrated Circuit 集成电路总线
IRQ	Interrupt Request 中断请求
LDO	Low Drop-Out regulator 低压差线性稳压器
LVDS	Low Voltage Differential Signaling 低压差分信号
LI-	LVDS RX- 低压差分信号负接收端
LI+	LVDS RX+ 低压差分信号正接收端
LO-	LVDS TX- 低压差分信号负发射端
LO+	LVDS TX+ 低压差分信号正发射端
LED	Light Emitting Diode 发光二极管
MAC	Media Access Controller 介质访问控制
MDIO	Management Data Input / Output 管理数据输入/输出
MI	(PHY) Management Interface 以太网物理层接口器件管理接口

MII	Media Independent Interface 介质无关接口
MISO	Master In – Slave Out 主站输入-从站输出
MOSI	Master Out – Slave In 主站输出-从站输入
n.a.	not available 未使用
n.c.	not connected 未连接
O	Output 输出
PD	Pull-down 下拉
PDI	Process Data Interface 过程数据接口
	Physical Device Interface 物理设备接口
PLL	Phase Locked Loop 锁相回路
PU	Pull-up 上拉
PHY	Physical 以太网物理层器件
QFN	Quad Flat package No leads 方形扁平无引脚封装
RD	Read 读
SII	Slave Information Interface 从站信息接口
SM	SyncManager 同步管理器
SOF	Start of Frame 帧起始
SPI	Serial Peripheral Interface 串行外设接口
TA	Transfer Acknowledge 传输应答
TFBGA	Thin-profile Fine-pitch BGA 薄型球栅阵列封装
TS	Transfer Start 传输周期启动
UI	Unused Input (PDI: PD, 其它: GND)未使用的输入引脚
WD	Watchdog 看门狗
WPD	Weak Pull-down 弱下拉，只够配置信号
WPU	Weak Pull-up 弱上拉，只够配置信号
WR	Write 写

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate for each speed grade, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Temp	CLM9680BCPZ-500	CLM9680BCPZ-820	CLM9680BCPZ-1000	CLM9680BCPZ-1250	Unit
RESOLUTION	Full	14	14	14	14	Bits
ACCURACY						
No Missing Codes	Full	Guaranteed	Guaranteed	Guaranteed	Guaranteed	
Offset Error	Full	−0.3 0 +0.3	−0.3 0 +0.3	−0.31 0 +0.31	−0.31 0 +0.31	%FSR
Offset Matching	Full	0 0.3	0 0.23	0 0.23	0 0.3	%FSR
Gain Error	Full	−6 0 +6	−6 0 +6	−6 0 +6	−6 0 +6	%FSR
Gain Matching	Full	1 5.1	1 5.5	1 4.5	1 4.5	%FSR
Differential Nonlinearity (DNL)	Full	−0.6 ±0.5 +0.7	−0.7 ±0.5 +0.8	−0.7 ±0.5 +0.8	−0.8 ±0.5 +0.8	LSB
Integral Nonlinearity (INL)	Full	−4.5 ±2.5 +5.0	−3.3 ±2.5 +4.3	−5.7 ±2.5 +6.9	−6 ±3 +6	LSB
TEMPERATURE DRIFT						
Offset Error	Full	−3	−10	−12	−15	ppm/°C
Gain Error	Full	±25	±54	±13.8	92	ppm/°C
INTERNAL VOLTAGE REFERENCE						
Voltage	Full	1.0	1.0	1.0	1.0	V
INPUT-REFERRED NOISE						
V_{REF} = 1.0 V	25°C	2.06	2.46	2.63	3.45	LSB rms
Chiplon INPUTS						
Differential Input Voltage Range (Programmable)	Full	1.46 2.06 2.06	1.46 1.70 1.94	1.46 1.70 1.94	1.46 1.58 1.94	V p-p
Common-Mode Voltage (V_{CM})	25°C	2.05	2.05	2.05	2.05	V
Differential Input Capacitance[1]	25°C	1.5	1.5	1.5	1.5	pF
Chiplon Input Full Power Bandwidth	25°C	2	2	2	2	GHz
POWER SUPPLY						
AVDD1	Full	1.22 1.25 1.28	1.22 1.25 1.28	1.22 1.25 1.28	1.22 1.25 1.28	VVV
AVDD2	Full	2.44 2.50 2.56	2.44 2.50 2.56	2.44 2.50 2.56	2.44 2.50 2.56	VVV
AVDD3	Full	3.2 3.3 3.4	3.2 3.3 3.4	3.2 3.3 3.4	3.2 3.3 3.4	V
AVDD1_SR	Full	1.22 1.25 1.28	1.22 1.25 1.28	1.22 1.25 1.28	1.22 1.25 1.28	mA
DVDD	Full	1.22 1.25 1.28	1.22 1.25 1.28	1.22 1.25 1.28	1.22 1.25 1.28	mA
DRVDD	Full	1.22 1.25 1.28	1.22 1.25 1.28	1.22 1.25 1.28	1.22 1.25 1.28	mA
SPIVDD	Full	1.7 1.8 3.4	1.7 1.8 3.4	1.7 1.8 3.4	1.7 1.8 3.4	mA
I_{AVDD1}	Full	435 467	605 660	685 720	785 880	mA
I_{AVDD2}	Full	395 463	490 545	595 680	675 780	mA
I_{AVDD3}	Full	87 101	125 140	125 142	125 142	mA
I_{AVDD1_SR}	Full	15 22	15 18	16 18	17 20	mA
I_{DVDD2}	Full	145 152	205 246	208 269	250 325	
I_{DRVDD1}	Full	190 237	200 240	200 225	220 300	
I_{DRVDD} (L = 2 Mode)	25°C	140	N/A[3]	N/A[3]	N/A[3]	
I_{SPIVDD}	Full	5 6	5 6	5 6	5 6	

Parameter	Temp	CLM9680BCPZ-			CLM9680BCPZ-			CLM9680BCPZ-10			CLM9680BCPZ-12			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER CONSUMPTION														
Total Power Dissipation (Inc	Full		2.2			2.9			3.3			3.7		W
Total Power Dissipation (L = 2 Mode) Power-Dowr	25°C		2.1			N/A[3]			N/A[3]			N/A[3]		W
	Full		700			820			835			1030		mW

[1] All lanes running. Power dissipation on DRVDD changes with lane rate and number of lanes used.
[2] Default mode. No DDCs used. L = 4, M = 2, F = 1.
[3] N/A means not applicable. At the maximum sample rate, it is not applicable to use L = 2 mode on the JESD204B output interface because this exceeds the maximum lane rate of 12.5 Gbps. L = 2 mode is supported when the equation ((M × N′ × (10/8) × f_{OUT})/L) results in a line rate that is ≤12.5 Gbps. f_{OUT} is the output sample rate and is denoted by f_S/DCM, where DCM is the decimation ratio.
[4] Can be controlled by the SPI.

AC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate for each speed grade, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter[1]	Temp	CLM9680BCPZ-500	CLM9680BCPZ-820	CLM9680BCPZ-1000	CLM9680BCPZ-1250	Unit
Chiplon INPUT FULL SCALE	Full	2.06	1.7	1.7	1.58	V p-p
NOISE DENSITY[2]	Full	−153	−153	−154	−151.5	dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)[3]						
f_{IN} = 10 MHz	25°C	69.2	67.2	67.2	63.6	dBFS
f_{IN} = 170 MHz	Full	67.8 69.0	65.6 67.0	65.1 66.6	61.5 63.2	dBFS
f_{IN} = 340 MHz	25°C	68.6	66.5	65.3	62.8	dBFS
f_{IN} = 450 MHz	25°C	68.0	65.1	64.0	62.2	dBFS
f_{IN} = 765 MHz	25°C	64.4	64.0	62.6	61.1	dBFS
f_{IN} = 985 MHz	25°C	63.8	63.4	61.5	59.2	dBFS
f_{IN} = 1950 MHz	25°C	60.5	59.7	57.0	55.5	dBFS
SNR AND DISTORTION RATIO (SINAD)[3]						
f_{IN} = 10 MHz	25°C	69.0	67.1	67.1	63.5	dBFS
f_{IN} = 170 MHz	Full	67.6 68.8	65.2 66.8	65.0 66.4	61.4 62.8	dBFS
f_{IN} = 340 MHz	25°C	68.4	66.3	65.2	62.6	dBFS
f_{IN} = 450 MHz	25°C	67.9	64.7	63.8	61.8	dBFS
f_{IN} = 765 MHz	25°C	64.2	63.5	62.5	60.8	dBFS
f_{IN} = 985 MHz	25°C	63.6	62.7	61.4	58.2	dBFS
f_{IN} = 1950 MHz	25°C	60.3	58.7	56.4	51.5	dBFS
EFFECTIVE NUMBER OF BITS (ENOB)						
f_{IN} = 10 MHz	25°C	11.2	10.9	10.8	10.3	Bits
f_{IN} = 170 MHz	Full	10.9 11.1	10.5 10.8	10.5 10.7	9.9 10.1	Bits
f_{IN} = 340 MHz	25°C	11.1	10.7	10.5	10.1	Bits
f_{IN} = 450 MHz	25°C	11.0	10.5	10.3	10.0	Bits
f_{IN} = 765 MHz	25°C	10.4	10.3	10.1	9.8	Bits
f_{IN} = 985 MHz	25°C	10.3	10.1	9.9	9.4	Bits
f_{IN} = 1950 MHz	25°C	9.7	9.5	9.1	8.3	Bits

Parameter[1]	Temp	CLM9680BCPZ-500	CLM9680BCPZ-820	CLM9680BCPZ-1000	CLM9680BCPZ-1250	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)[3]						
f_{IN} = 10 MHz	25°C	83	91	88	84	dBFS
f_{IN} = 170 MHz	Full	80 88	75 83	75 85	74 77	dBFS
f_{IN} = 340 MHz	25°C	83	81	85	78	dBFS
f_{IN} = 450 MHz	25°C	81	78	82	76	dBFS
f_{IN} = 765 MHz	25°C	80	78	82	77	dBFS
f_{IN} = 985 MHz	25°C	75	74	80	71	dBFS
f_{IN} = 1950 MHz	25°C	70	70	69	61	dBFS
WORST HARMONIC, SECOND OR THIRD[3]						
f_{IN} = 10 MHz	25°C	−83	−91	−88	−84	dBFS
f_{IN} = 170 MHz	Full	−88	−83	−85	−77	dBFS
f_{IN} = 340 MHz	25°C	−80	−75	−75	−74	dBFS
f_{IN} = 450 MHz	25°C	−83	−81	−85	−78	dBFS
f_{IN} = 765 MHz	25°C	−81	−78	−82	−76	dBFS
f_{IN} = 985 MHz	25°C	−80	−78	−82	−77	dBFS
f_{IN} = 1950 MHz	25°C	−75	−74	−80	−71	dBFS
		−70	−70	−69	−61	
WORST OTHER, EXCLUDING SECOND OR THIRD HARMONIC[3]						
f_{IN} = 10 MHz	25°C	−95	−97	−95	−87	dBFS
f_{IN} = 170 MHz	Full	−95	−93	−94	−79	dBFS
f_{IN} = 340 MHz	25°C	−82	−80	−81	−74	dBFS
f_{IN} = 450 MHz	25°C	−93	−91	−88	−81	dBFS
f_{IN} = 765 MHz	25°C	−93	−90	−86	−79	dBFS
f_{IN} = 985 MHz	25°C	−88	−83	−83	−79	dBFS
f_{IN} = 1950 MHz	25°C	−89	−84	−82	−77	dBFS
		−84	−74	−79	−69	
TWO-TONE INTERMODULATION DISTORTION (IMD), A_{IN1} AND A_{IN2} = −7 dBFS						
f_{IN1} = 185 MHz, f_{IN2} = 188 MHz	25°C	−88	−90	−87	−82	dBFS
f_{IN1} = 338 MHz, f_{IN2} = 341 MHz	25°C	−88	−87	−88	−78[4]	dBFS
CROSSTALK[5]	25°C	95	95	95	95	dB
FULL POWER BANDWIDTH[6]	25°C	2	2	2	2	GHz

DIGITAL SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate for each speed grade, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−) Logic Compliance Differential I Input Common-Mode Voltage Input Resistance (Differentia	Full Full Full Full	 600	LVDS/LVPECL 1200 0.85 35	 1800 2.5	mV p-p V kΩ pF
SYSREF INPUTS (SYSREF+, SYSREF−) Logic Compliance Differential Input Voltage Input Common-Mode Voltage Input Resistance (Differentia	Full Full Full Full	 400 0.6	LVDS/LVPECL 1200 0.85 35	 1800 2.0 2.5	mV p-p V kΩ pF
LOGIC INPUTS (SDI, SCLK, CSB, PDWN/STBY) Logic Compliance Logic 1 Voltage Logic 0 Voltage Input Re	Full Full Full Full	 0.8 × SPIVDD 0	CMOS 30	 0.5	V V kΩ
LOGIC OUTPUT (SDIO) Logic Compliance Logic 1 Voltage (I_{OH} = 800 µA) Logic 0 Voltage (I_{OL} = 50 µA)	Full Full Full	 0.8 × SPIVDD 0	CMOS	 0.5	V V
SYNCIN INPUT (SYNCINB+/SYNCINB−) Logic Compliance Differential Input Voltage Input Common-Mode Voltage Input Resistance (Differentia	Full Full Full Full	 400 0.6	LVDS/LVPECL/CMOS 1200 0.85 35	 1800 2.0 2.5	mV p-p V kΩ pF
LOGIC OUTPUTS (FD_A, FD_B) Logic Compliance Logic 1 Voltage Logic 0 Voltage Input Re	Full Full Full Full	 0.8 × SPIVDD 0	CMOS 30	 0.5	V V kΩ
DIGITAL OUTPUTS (SERDOUTx±, x = 0 TO 3) Logic Compliance Differential Output Voltage Output Common-Mode Voltage (V_{CM}) AC-Coupled Short-Circuit Current (I_{DSHORT}) Differential Return Loss (RL_{DIFF}	Full Full 25°C 25°C 25°C	 360 0 −100 8 6 80	CML 100	 770 1.8 +100 120	mV p-p V mA dB dB

[1] Differential and common-mode return loss are measured from 100 MHz to 0.75 × baud rate.

SWITCHING SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate for each speed grade, A_{IN} = −1.0 dBFS, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 4.

		CLM9680BCPZ-			CLM9680BCPZ-8			CLM9680BCPZ-			CLM9680BCPZ-1			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK														
Clock Rate (at CLK+/CLK− Pins) Maxim	Full	0.3		4	0.3		4	0.3		4	0.3		4	GHz
	Full Full	500 300 1000 1000			820 300 609.7 609.7			1000 300 500 500			1250 300 400 400			MSPS M ps
OUTPUT PARAMETERS Unit I														
80% into 100 Ω Load)	Full	80	200		80	121.95		80	100		80	80		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)	25°C 25	24	32		24	32		24	32		24	32		ps ps m
PLL Lock Time	25°C	24	32		24	32		24	32		24	32		Gbps
Data Rate per Channel (NRZ)[4]			2			2			2			2		
		3.125	5	12.5	3.125	8.2	12.5	3.125	10	12.5	3.1215	12.5	12.5	
LATENCY[5]														
Pipeline Latency Fast Dete	Full		55			55			55			55		Clock cy
Standby														
Power-Down	Full			28			28			28			28	ms
	25°C		1			1			1			1		ms
APERTURE														
Aperture Delay (t_A)	Full		530			530			530			530		ps
Aperture Uncertainty (Jitter, t_J)	Full		55			55			55			55		fs rms
Out-of-Range Recovery Time	Full		1			1			1			1		Clock cycles

1 The maximum sample rate is the clock rate after the divider.
2 The minimum sample rate operates at 300 MSPS with L = 2 or L = 1.
3 Baud rate = 1/UI. A subset of this range can be supported.
4 Default L = 4. This number can be changed based on the sample rate and decimation ratio.
5 No DDCs used. L = 4, M = 2, F = 1.
6 Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLK+ to SYSREF+ TIMING REQUIREMENTS t_{SU}	See Figure 3				
t_{H_SR}	Device clock to SYSREF+ setup time		117		ps
	Device clock to SYSREF+ hold time		−96		ps
SPI TIMING REQUIREMENTS t_{DS}	See Figure 4				
t_{DH} t_{CLK} t_S	Setup time between the data and the rising edge of SCLK Hold ti	2			ns ns ns
t_H t_{HIGH} t_{LOW} t_{ACCESS}	Setup time between CSB and SCLK	2 40 2			
	Hold time between CSB and SCLK	2 10 10			ns
t_{DIS_SDIO}	Minimum period that SCLK must be in a logic high state Minimur		6	10	
	Time required for the SDIO pin to switch from an output to an inp				
		10			

Timing Diagrams

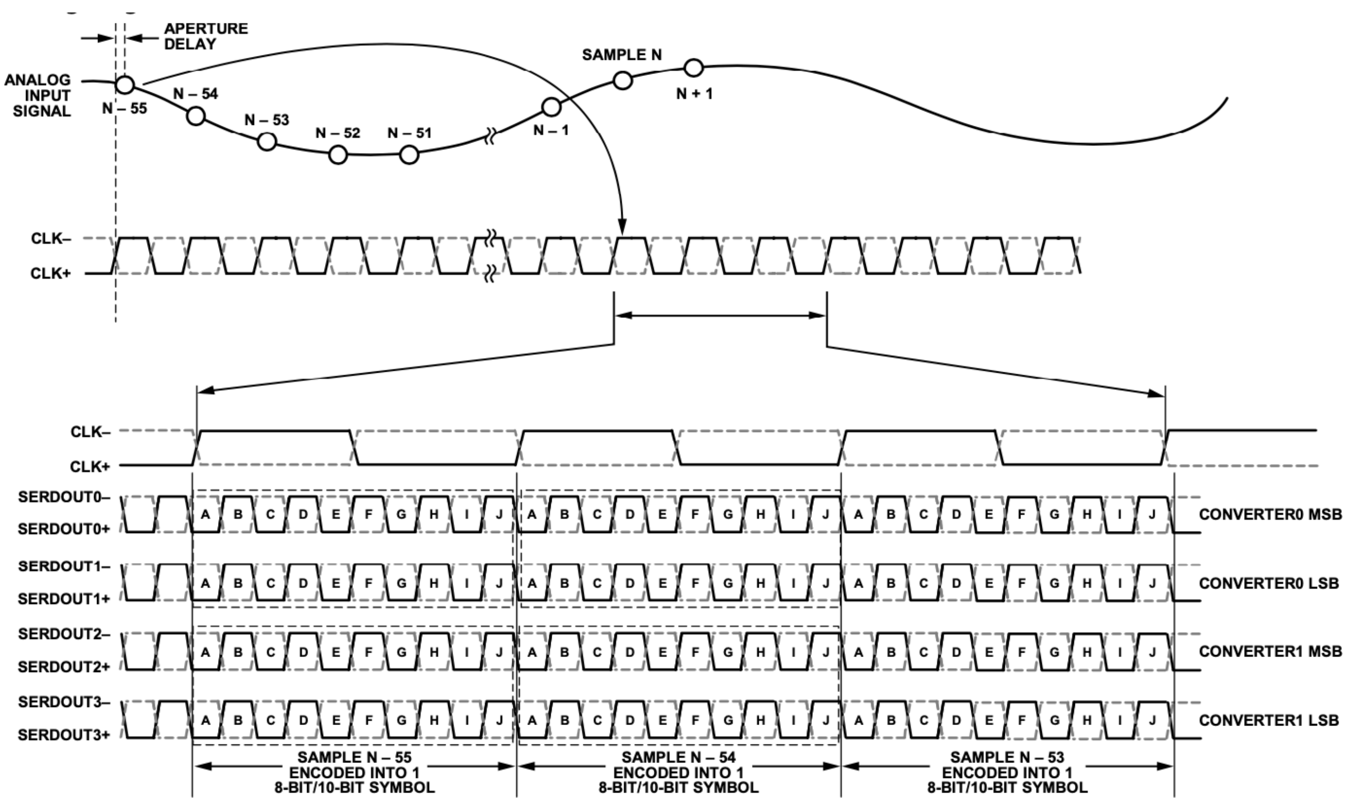


Figure 2. Data Output Timing (Full Bandwidth Mode; L = 4; M = 2; F = 1)

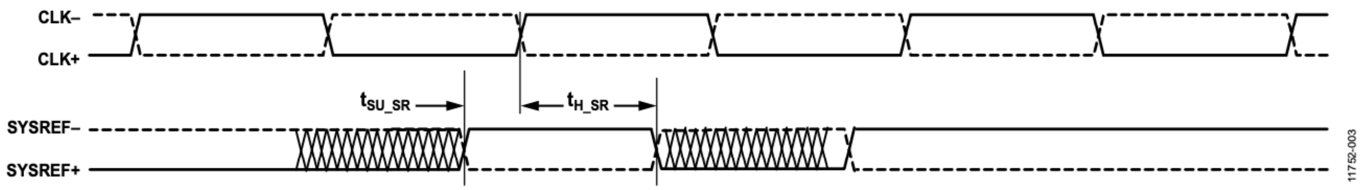


Figure 3. SYSREF± Setup and Hold Timing

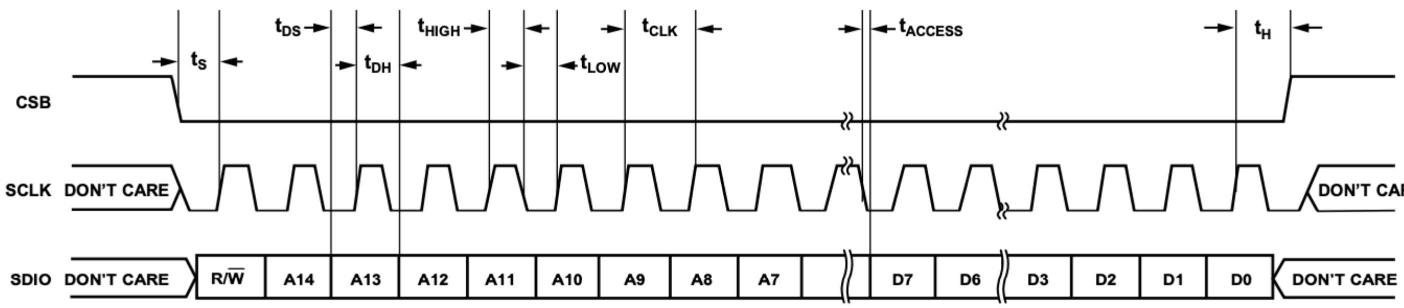


Figure 4. Serial Port Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.32 V
AVDD1_SR to	1.32 V
AGND AVDD2 to	2.75 V
AGND AVDD3 to	3.63 V
AGND DVDD to	1.32 V
DGND DRVDD to	1.32 V
DRGND SPIVDD	3.63 V
to AGND AGND to	−0.3 V to +0.3 V
DRGND VIN±x to	3.2 V
AGND	−0.3 V to SPIVDD + 0.3
SCLK, SDIO, CSB to	V −0.3 V to SPIVDD +
AGND PDWN/STBY to	0.3 V −40°C to +85°C
AGND	−40°C to +125°C
Operating Temperature Range	−65°C to +150°C

Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Typical θ_{JA}, θ_{JB}, and θ_{JC} are specified vs. the number of printed circuit board (PCB) layers in different airflow velocities (in m/sec). Airflow increases heat dissipation effectively reducing θ_{JA} and θ_{JB}. In addition, metal in direct contact with the package leads and exposed pad from metal traces, through holes, ground, and power planes, reduces θ_{JA}. Thermal performance for actual applications requires careful inspection of the conditions in an application. The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 6.

Table 7. Thermal Resistance Values

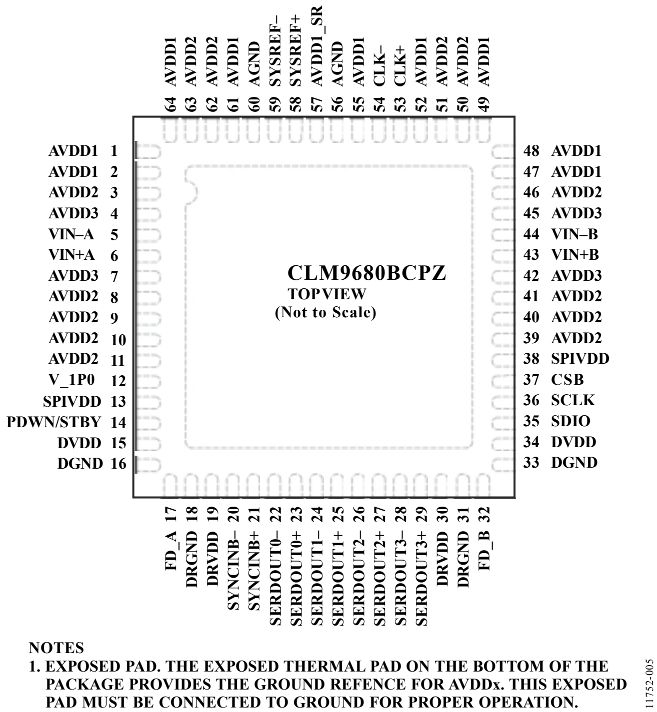
PCB Type	Airflow Velocity (m/sec)	θ_{JA}	Ψ_{JB}	θ_{JC_TOP}	θ_{JC_BOT}	Unit
JEDEC 2s2p Board	0.0	17.8[1,2]	6.3[1,3]	4.7[1,4]	1.2[1,4]	°C/W
	1.0	15.6[1,2]	5.9[1,3]	N/A[5]		°C/W
	2.5	15.0[1,2]	5.7[1,3]	N/A[5]		°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2s2p test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per JEDEC JESD51-8 (still air).
[4] Per MIL-STD 883, Method 1012.1.
[5] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE GROUND REFENCE FOR AVDDx. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

Figure 5. Pin Configuration (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
Power Supplies			
0	EPAD	Ground	Exposed Pad. The exposed thermal pad on the bottom of the package provides the ground reference for AVDDx. This exposed pad must be connected to ground for proper operation.
1, 2, 47, 48, 49, 52, 55, 61, 64	AVDD1	Supply	Chiplon Power Supply (1.25 V Nominal).
3, 8, 9, 10, 11, 39, 40, 41, 46, 50, 51, 62, 63	AVDD2	Supply	Chiplon Power Supply (2.5 V Nominal).
4, 7, 42, 45	AVDD3	Supply	Chiplon Power Supply (3.3 V Nominal).
13, 38	SPIVDD	Supply	Digital Power Supply for SPI (1.8 V to 3.3 V).
15, 34	DVDD	Supply	Digital Power Supply (1.25 V Nominal).
16, 33	DGND	Ground	Ground Reference for DVDD.
18, 31	DRGND	Ground	Ground Reference for DRVDD.
19, 30	DRVDD	Supply	Digital Driver Power Supply (1.25 V Nominal).
56, 60	AGND[1]	Ground	Ground Reference for SYSREF±.
57	AVDD1_SR[1]	Supply	Chiplon Power Supply for SYSREF± (1.25 V Nominal).
Chiplon			
5, 6	VIN−A, VIN+A	Input	ADC A Chiplon Input Complement/True.
12	V_1P0	Input/DNC	1.0 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or an input. Do not connect this pin if using the internal reference. Requires a 1.0 V reference voltage input if using an external voltage reference source.
44, 43	VIN−B, VIN+B	Input	ADC B Chiplon Input Complement/True.
53, 54	CLK+, CLK−	Input	Clock Input True/Complement.

Pin No.	Mnemonic	Type	Description
CMOS Outputs			
17, 32	FD_A, FD_B	Output	Fast Detect Outputs for Channel A and Channel B.
Digital Inputs			
20, 21	SYNCINB−, SYNCINB+	Input	Active Low JESD204B LVDS Sync Input True/Complement.
58, 59	SYSREF+, SYSREF−	Input	Active High JESD204B LVDS System Reference Input True/ Complement.
Data Outputs			
22, 23	SERDOUT0−, SERDOUT0+	Output	Lane 0 Output Data Complement/True.
24, 25	SERDOUT1−, SERDOUT1+	Output	Lane 1 Output Data Complement/True.
26, 27	SERDOUT2−, SERDOUT2+	Output	Lane 2 Output Data Complement/True.
28, 29	SERDOUT3−, SERDOUT3+	Output	Lane 3 Output Data Complement/True.
Device Under Test (DUT) Controls			
14	PDWN/STBY	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby. Requires an external 10 kΩ pull-down resistor.
35	SDIO	Input/Output	SPI Serial Data Input/Output.
36	SCLK	Input	SPI Serial Clock.
37	CSB	Input	SPI Chip Select (Active Low).

1 To ensure proper ADC operation, connect AVDD1_SR and AGND separately from the AVDD1 and EPAD connection. For more information, see the Applications Information section.

TYPICAL PERFORMANCE CHARACTERISTICS

CLM9680BCPZ-1250

AVDD1 = 1.25 V, AVDD1_SR = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, 1.58 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, default SPI settings, clock divider = 2, T_A = 25°C, 128k FFT sample, unless otherwise noted. See Table 10 for recommended settings.

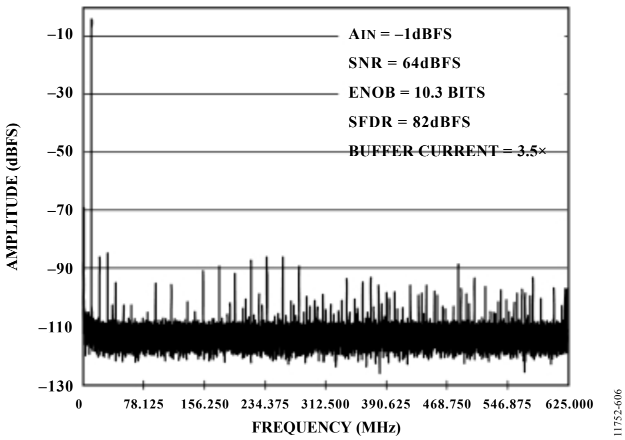


Figure 6. Single-Tone FFT with f_{IN} = 10.3 MHz

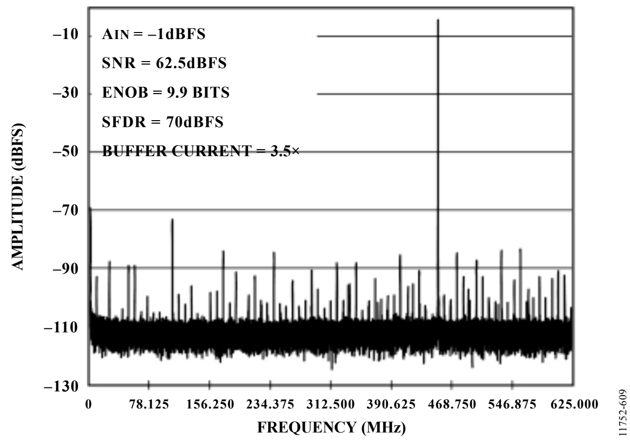


Figure 9. Single-Tone FFT with f_{IN} = 450.3 MHz

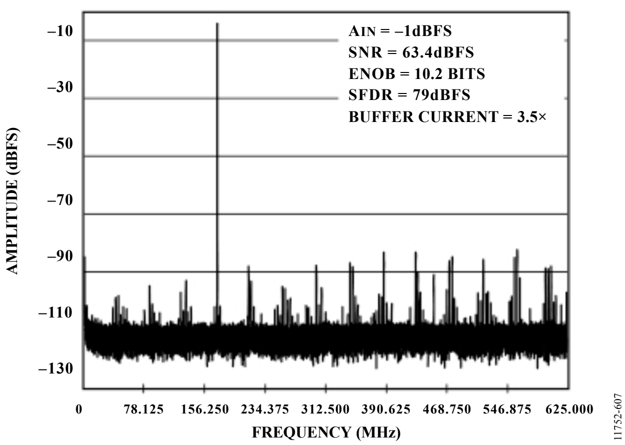


Figure 7. Single-Tone FFT with f_{IN} = 170.3 MHz

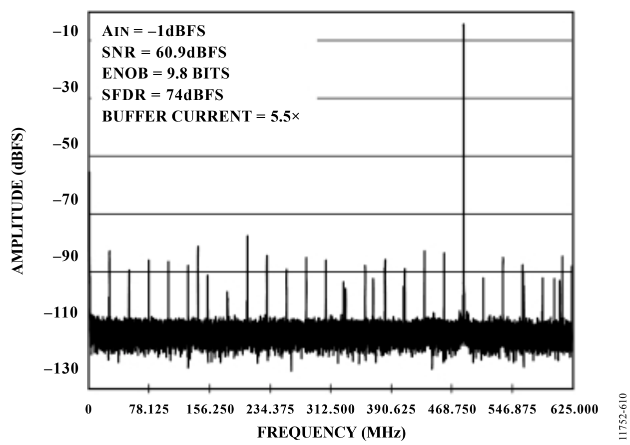


Figure 10. Single-Tone FFT with f_{IN} = 765.3 MHz

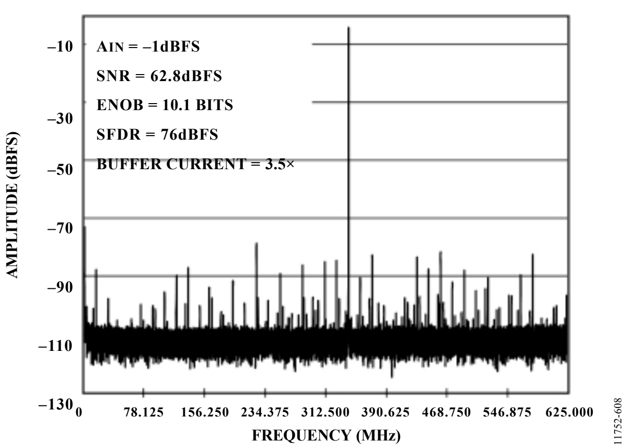


Figure 8. Single-Tone FFT with f_{IN} = 340.3 MHz

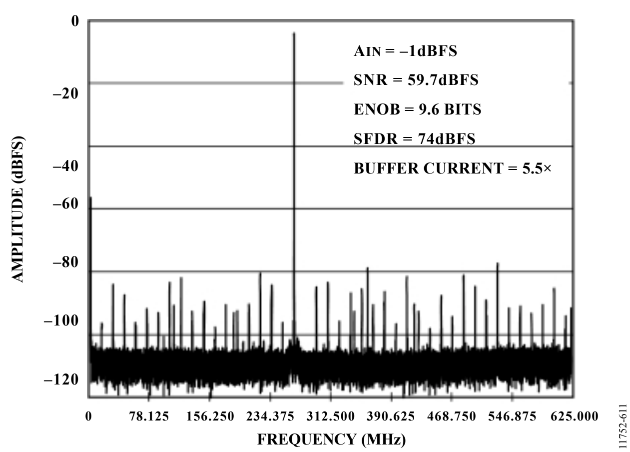


Figure 11. Single-Tone FFT with f_{IN} = 985.3 MHz

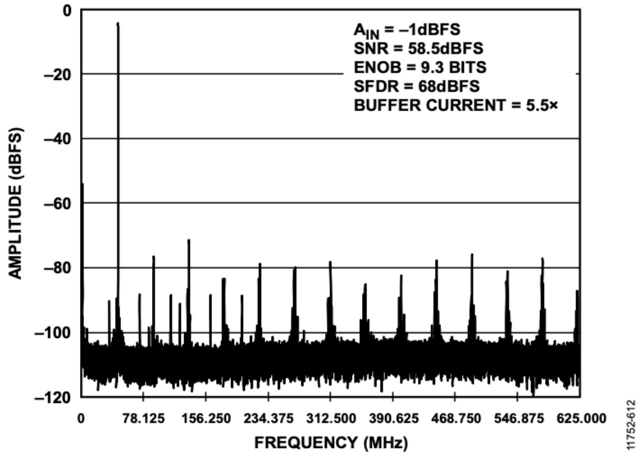


Figure 12. Single-Tone FFT with f_{IN} = 1205.3 MHz

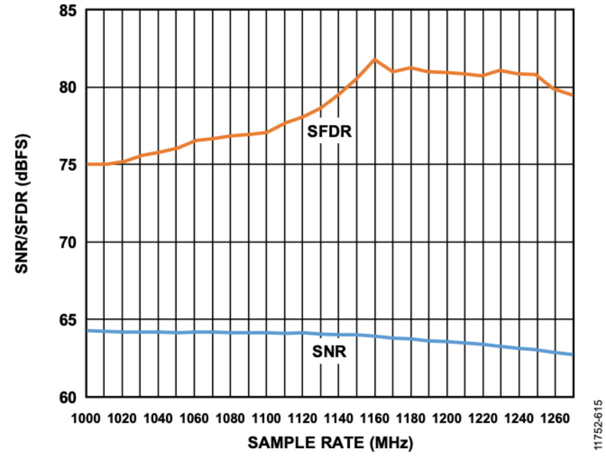


Figure 15. SNR/SFDR vs. f_S, f_{IN} = 170.3 MHz; Buffer Control 1 (0x018) = 3.5×

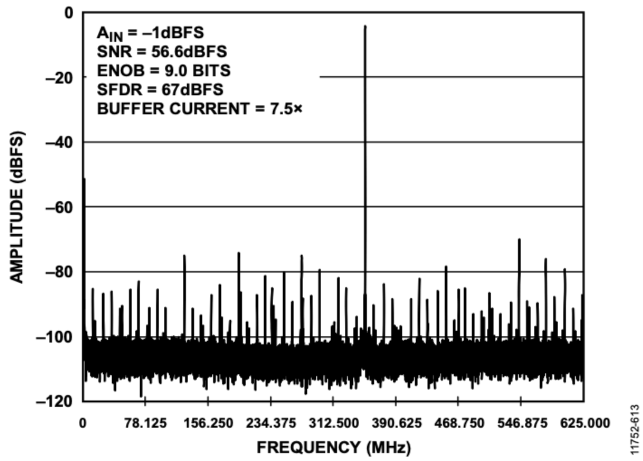


Figure 13. Single-Tone FFT with f_{IN} = 1602.3 MHz

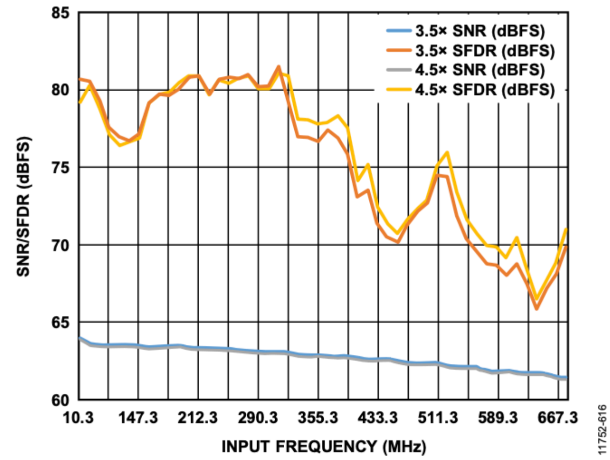


Figure 16. SNR/SFDR vs. f_{IN}; f_{IN} < 700 MHz; Buffer Control 1 (0x018) = 3.5× and 4.5×

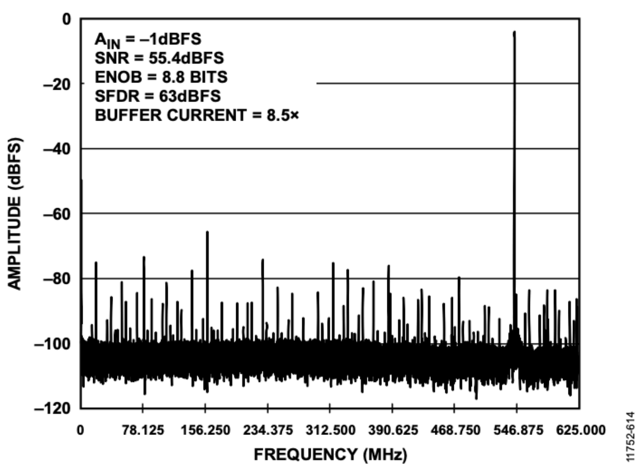


Figure 14. Single-Tone FFT with f_{IN} = 1954.3 MHz

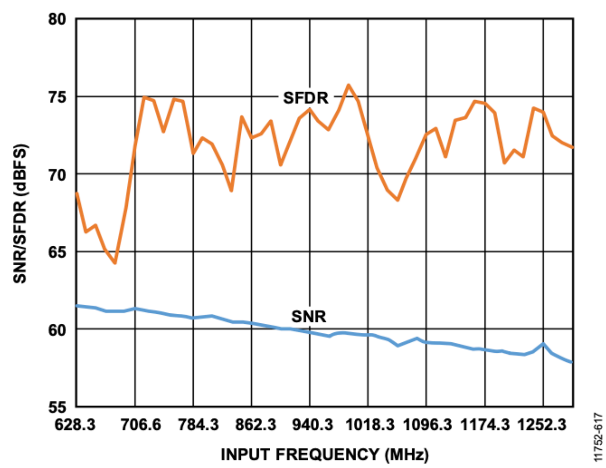


Figure 17. SNR/SFDR vs. f_{IN}; 650 MHz < f_{IN} < 1.3 GHz; Buffer Control 1 (0x018) = 6.5×

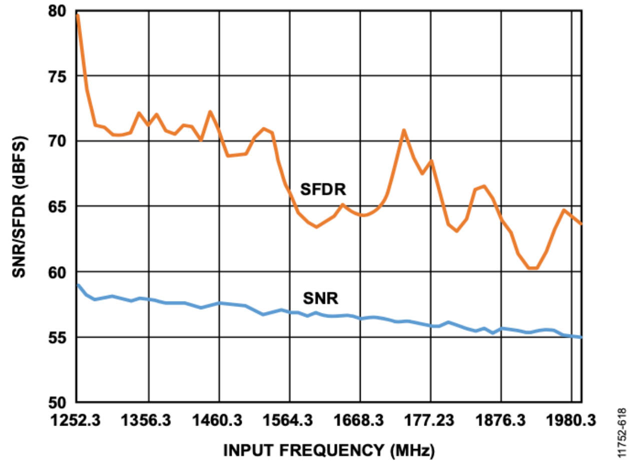


Figure 18. SNR/SFDR vs. f_{IN}; 1.3 GHz < f_{IN} < 2GHz; Buffer Control 1 (0x018) = 8.5×

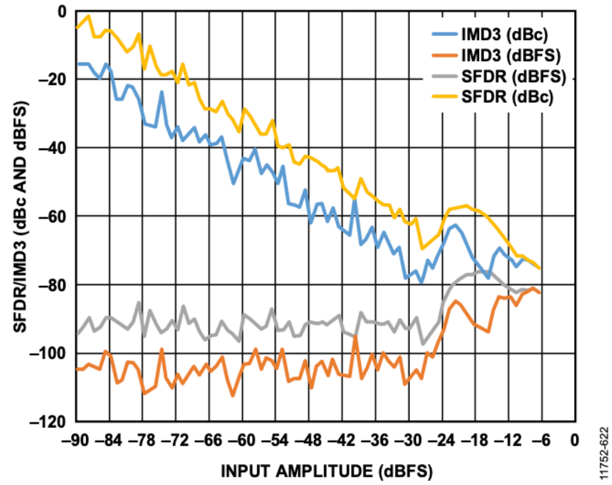


Figure 21. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

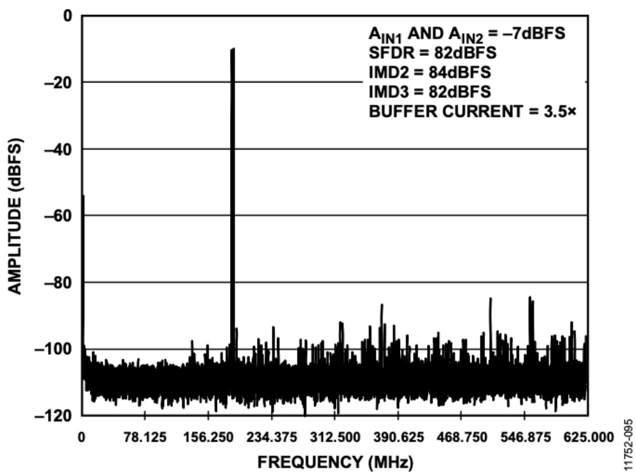


Figure 19. Two-Tone FFT; f_{IN1} = 184 MHz, f_{IN2} = 187 MHz

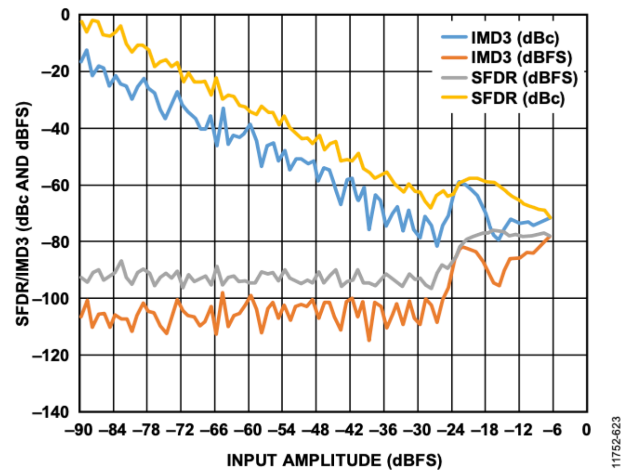


Figure 22. Two-Tone IMD3/SFDR vs. Input Amplitude (A_{IN}) with f_{IN1} = 449 MHz and f_{IN2} = 452 MHz

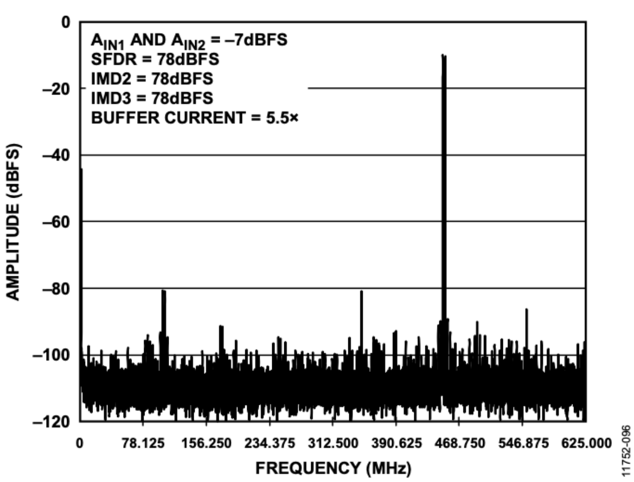


Figure 20. Two-Tone FFT; f_{IN1} = 449 MHz, f_{IN2} = 452 MHz

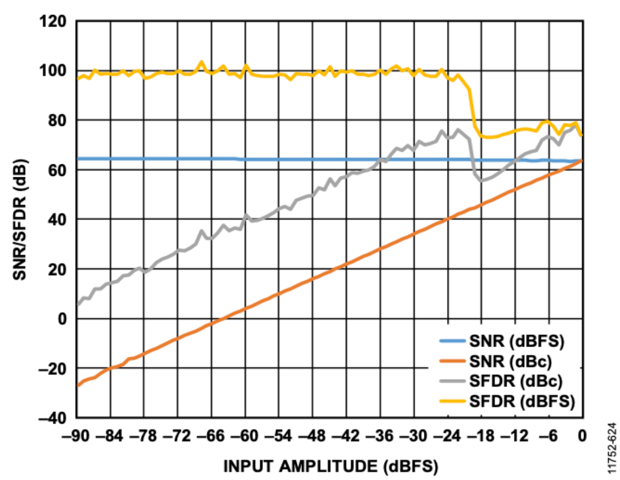


Figure 23. SNR/SFDR vs. Chiplon Input Level, f_{IN} = 170.3 MHz

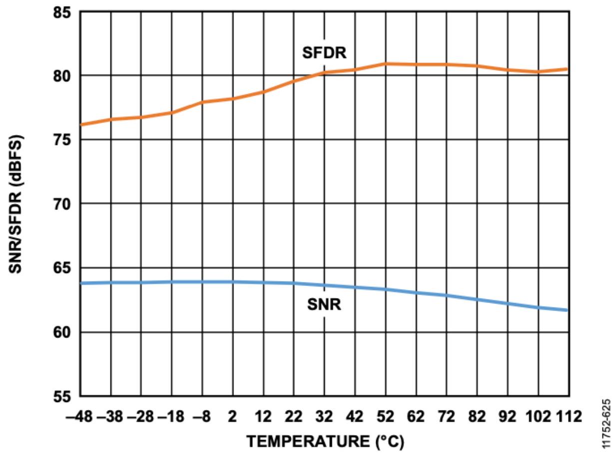


Figure 24. SNR/SFDR vs. Temperature, f_{IN} = 170.3 MHz

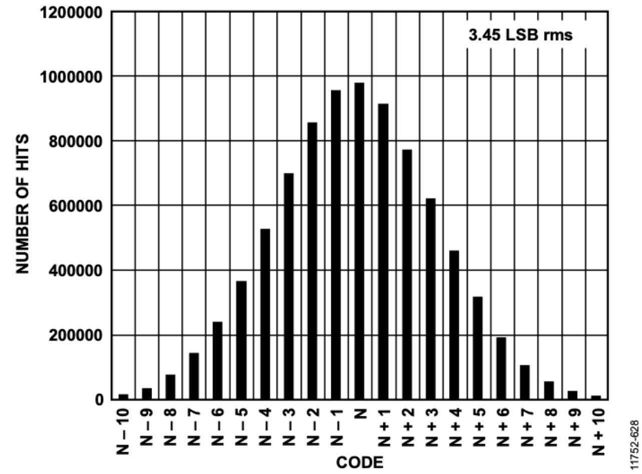


Figure 27. Input-Referred Noise Histogram

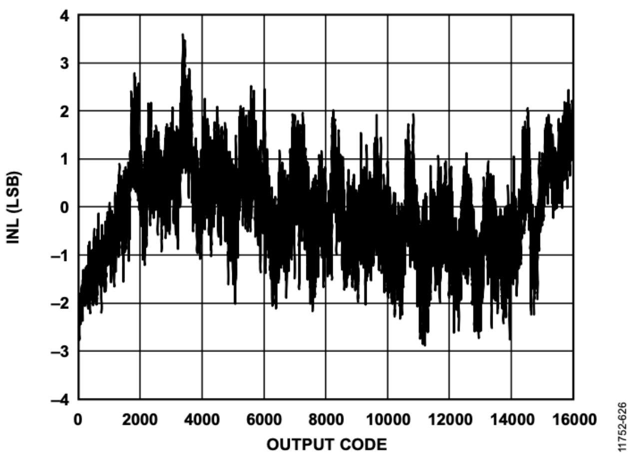


Figure 25. INL, f_{IN} = 10.3 MHz

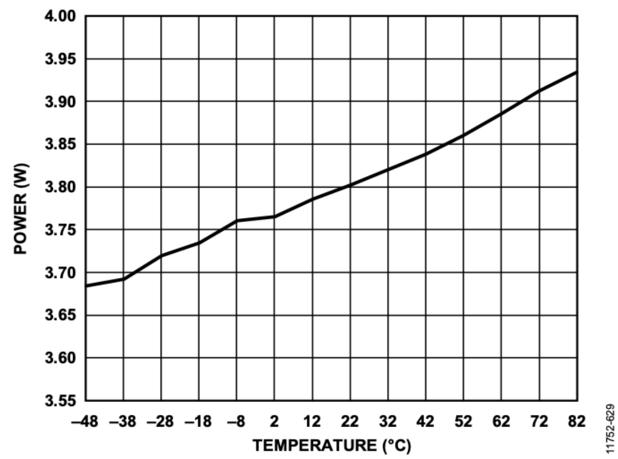


Figure 28. Power Dissipation vs. Temperature

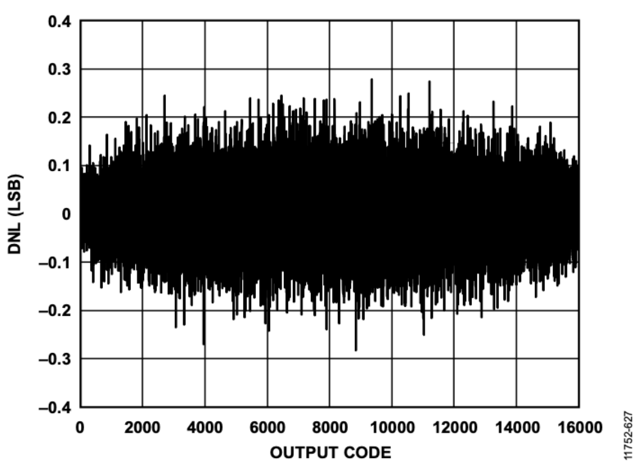


Figure 26. DNL, f_{IN} = 15 MHz

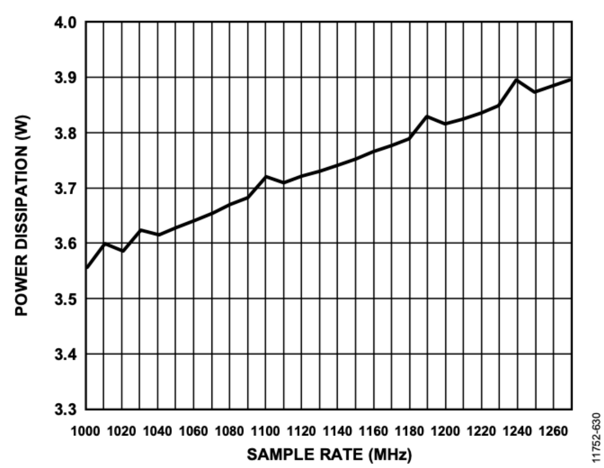


Figure 29. Power Dissipation vs. f_S

CLM9680BCPZ-1000

AVDD1 = 1.25 V, AVDD1_SR = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, 1.7 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, default SPI settings, clock divider = 2, T_A = 25°C, 128k FFT sample, unless otherwise noted. See Table 10 for recommended settings.

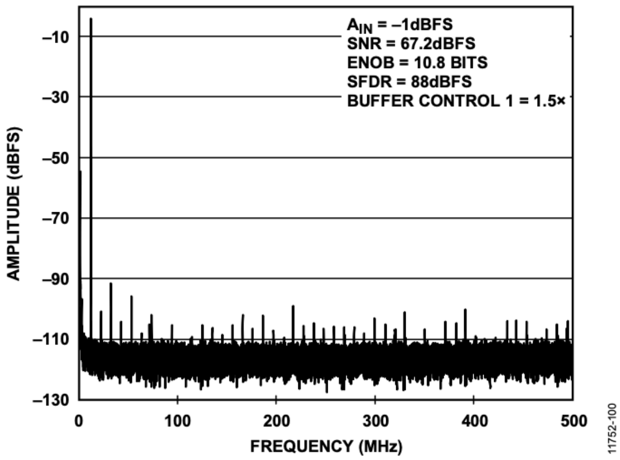


Figure 30. Single-Tone FFT with f_{IN} = 10.3 MHz

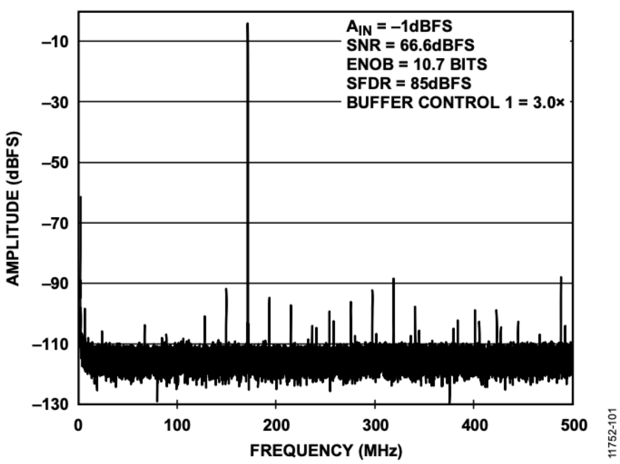


Figure 31. Single-Tone FFT with f_{IN} = 170.3 MHz

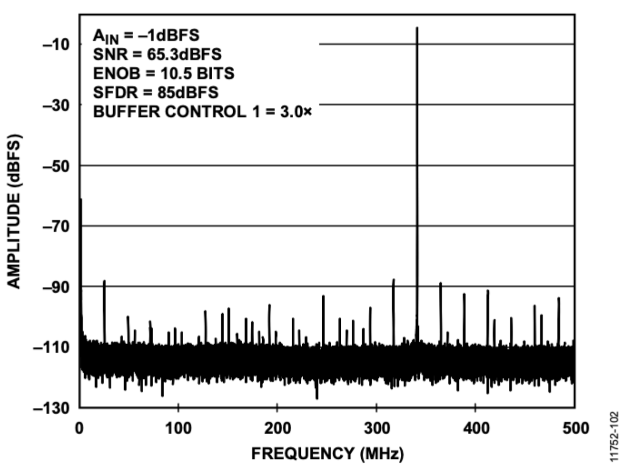


Figure 32. Single-Tone FFT with f_{IN} = 340.3 MHz

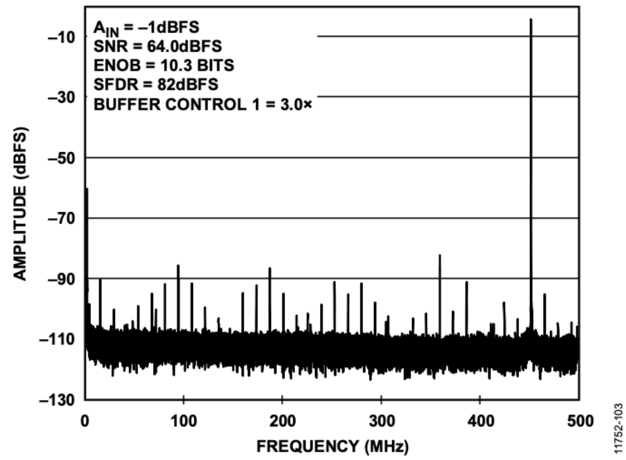


Figure 33. Single-Tone FFT with f_{IN} = 450.3 MHz

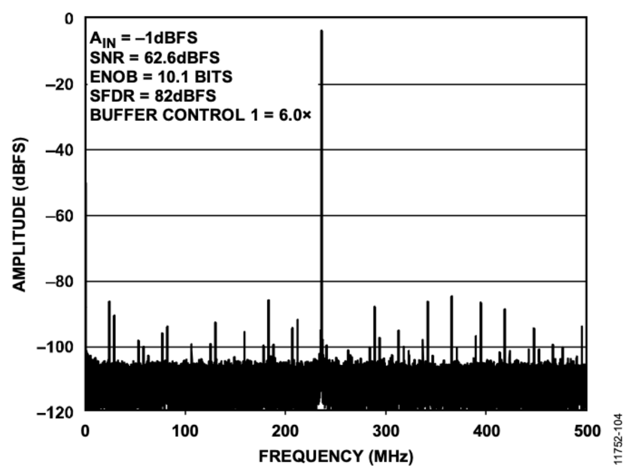


Figure 34. Single-Tone FFT with f_{IN} = 765.3 MHz

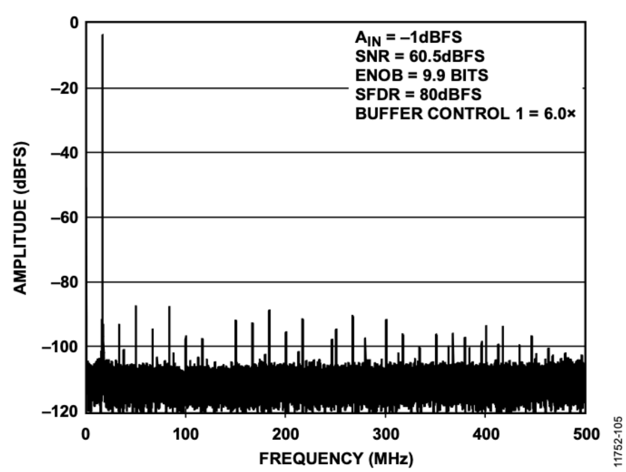


Figure 35. Single-Tone FFT with f_{IN} = 985.3 MHz

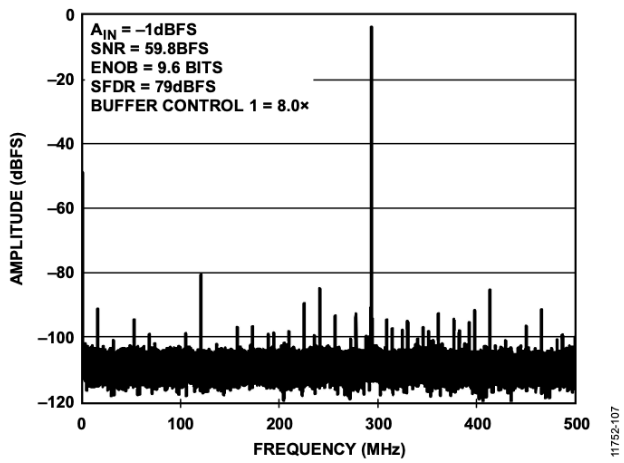


Figure 36. Single-Tone FFT with f_{IN} = 1293.3 MHz

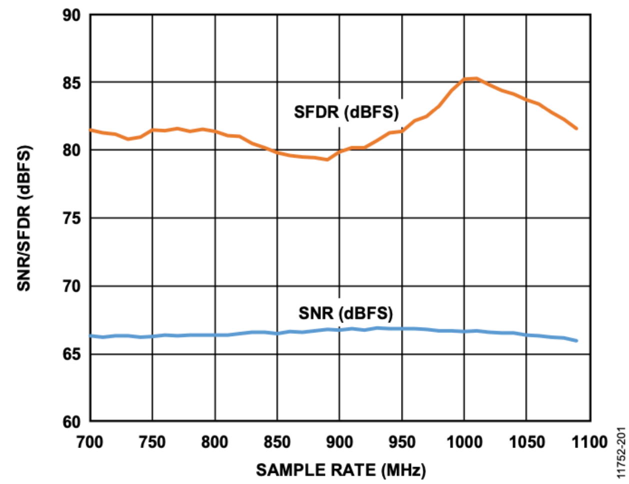


Figure 39. SNR/SFDR vs. f_S, f_{IN} = 170.3 MHz; Buffer Control 1 (0x018) = 3.0×

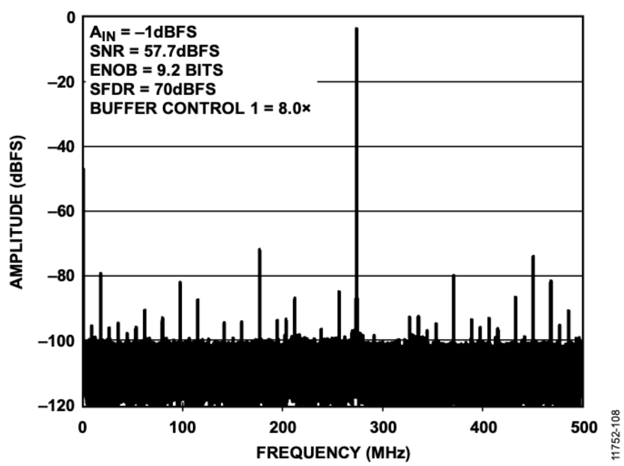


Figure 37. Single-Tone FFT with f_{IN} = 1725.3 MHz

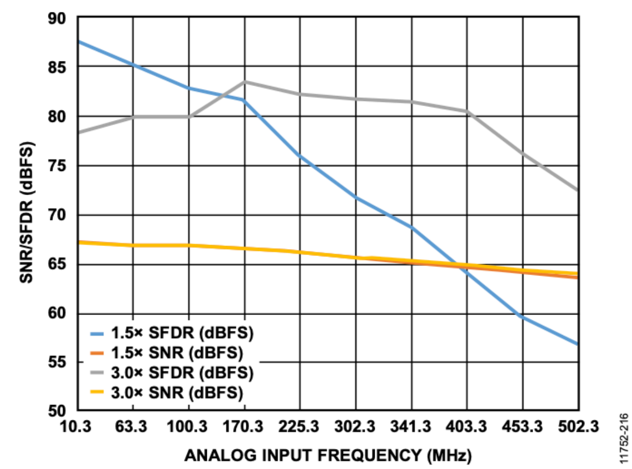


Figure 40. SNR/SFDR vs. f_{IN}; f_{IN} < 500 MHz; Buffer Control 1 (0x018) = 1.5× and 3.0×

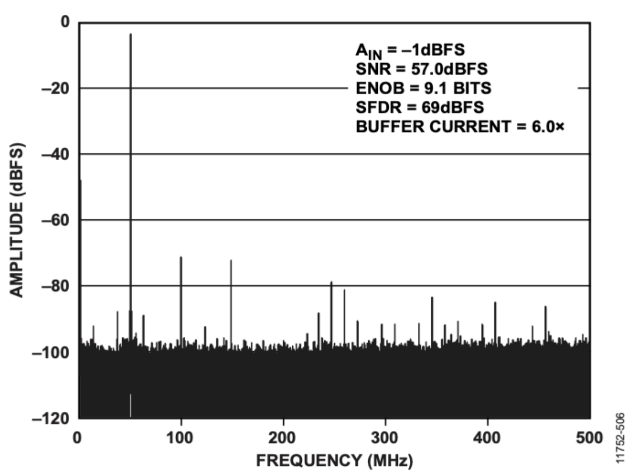


Figure 38. Single-Tone FFT with f_{IN} = 1950.3 MHz

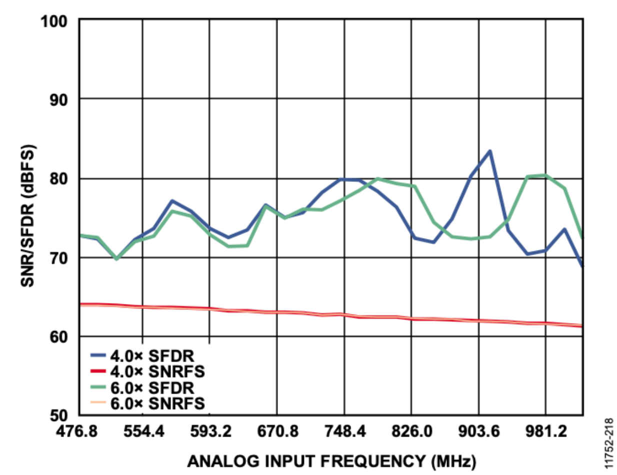


Figure 41. SNR/SFDR vs. f_{IN}; 500 MHz < f_{IN} < 1 GHz; Buffer Control 1 (0x018) = 4.0× and 6.0×

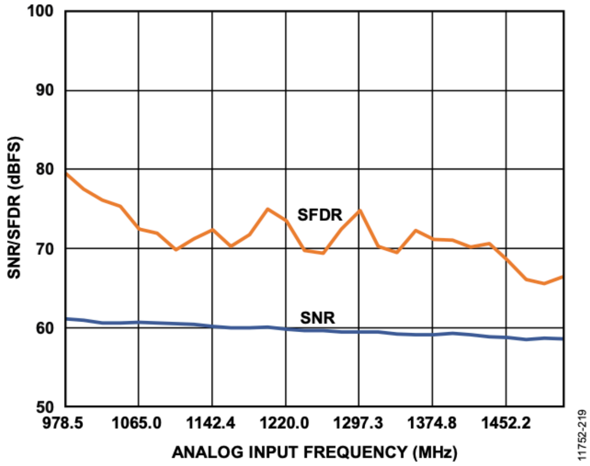


Figure 42. SNR/SFDR vs. f_{IN}; 1 GHz < f_{IN} < 1.5 GHz; Buffer Control 1 (0x018) = 6.0×

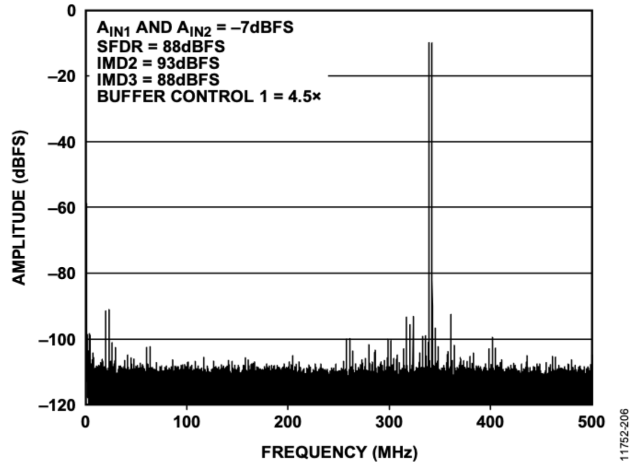


Figure 45. Two-Tone FFT; f_{IN1} = 338 MHz, f_{IN2} = 341 MHz

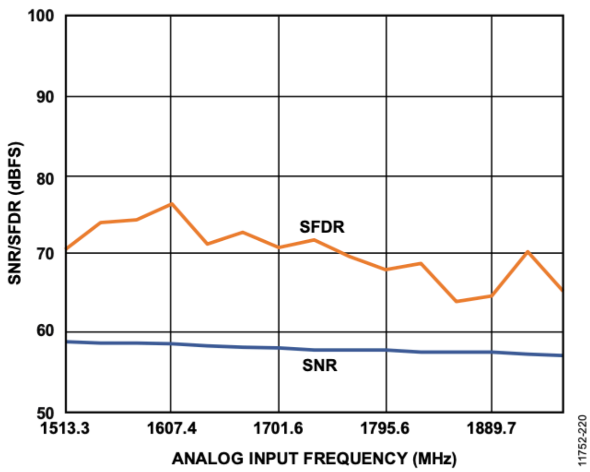


Figure 43. SNR/SFDR vs. f_{IN}; 1.5 GHz < f_{IN} < 2 GHz; Buffer Control 1 (0x018) = 7.5×

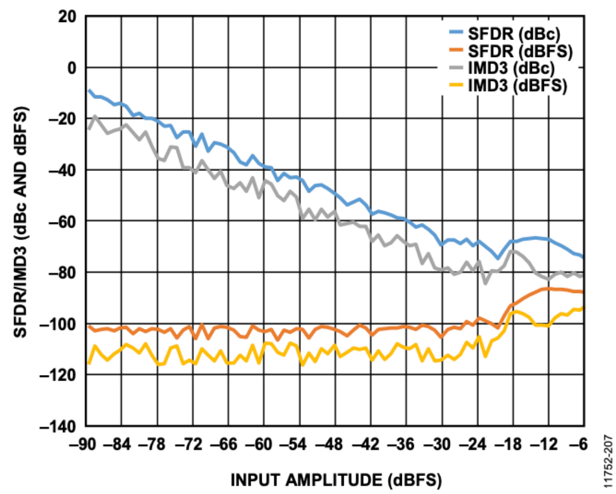


Figure 46. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz 11752-207

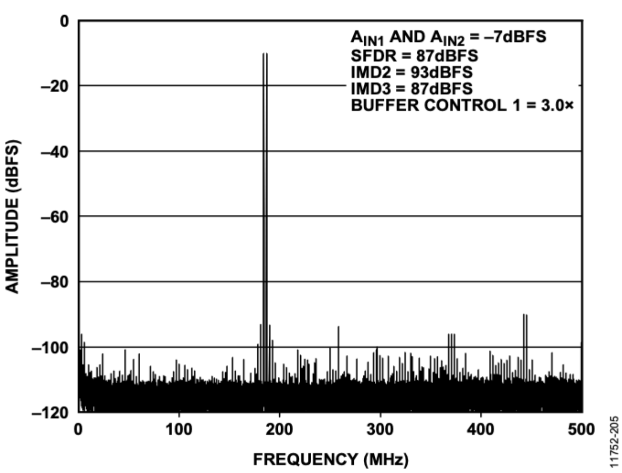


Figure 44. Two-Tone FFT; f_{IN1} = 184 MHz, f_{IN2} = 187 MHz

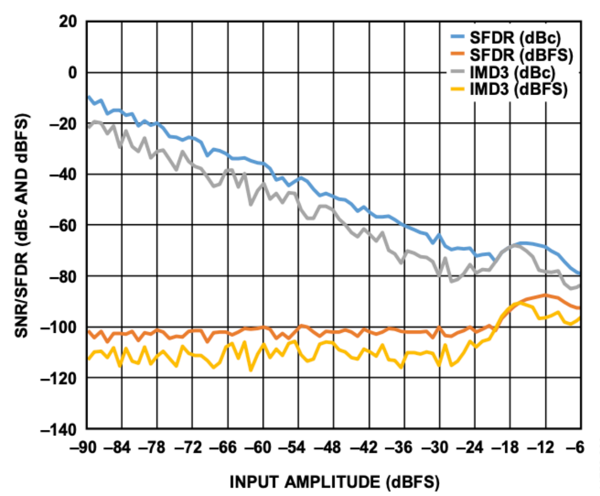


Figure 47. Two-Tone IMD3/SFDR vs. Input Amplitude (A_{IN}) with f_{IN1} = 338 MHz and f_{IN2} = 341 MHz

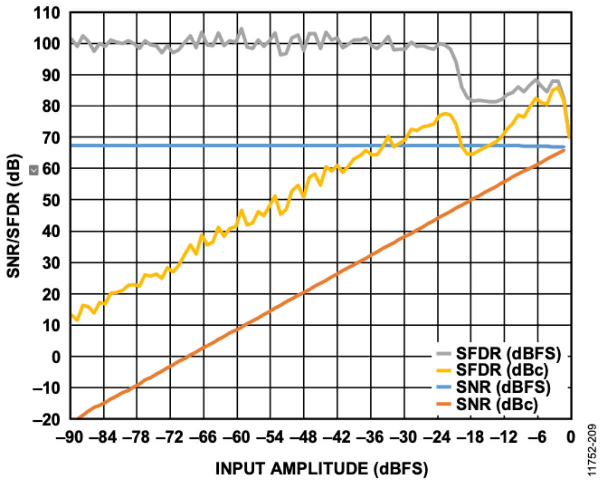


Figure 48. SNR/SFDR vs. Chiplon Input Level, f_{IN} = 170.3 MHz

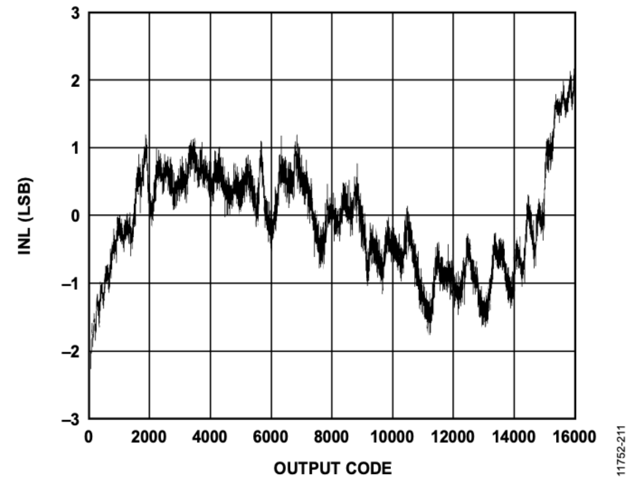


Figure 50. INL, f_{IN} = 10.3 MHz

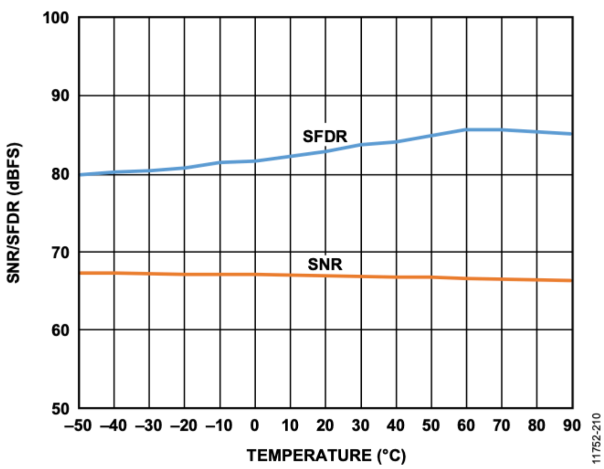


Figure 49. SNR/SFDR vs. Temperature, f_{IN} = 170.3 MHz

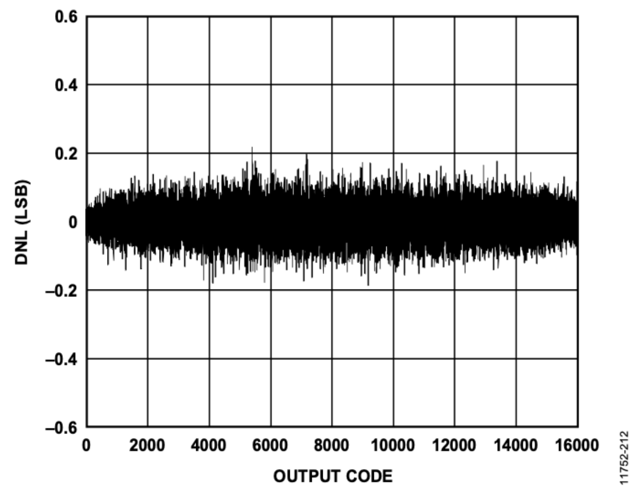


Figure 51. DNL, f_{IN} = 15 MHz

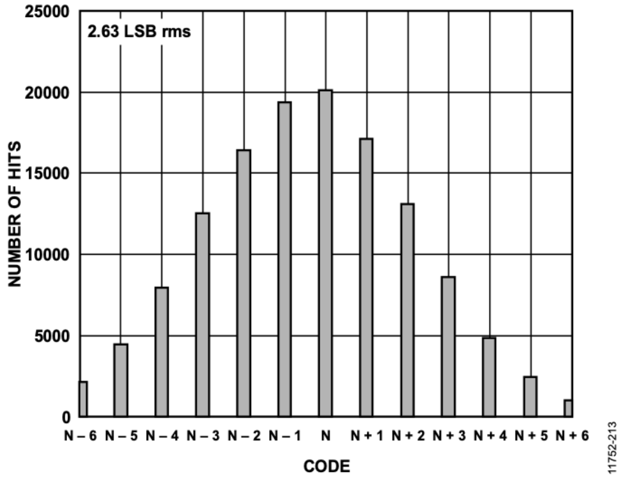


Figure 52. Input-Referred Noise Histogram

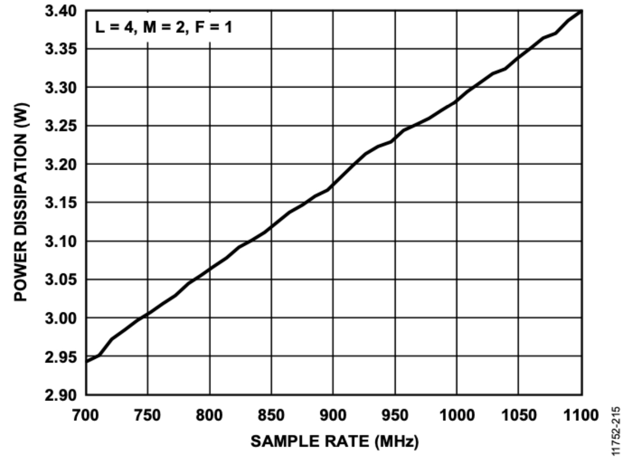


Figure 54. Power Dissipation vs. f_S

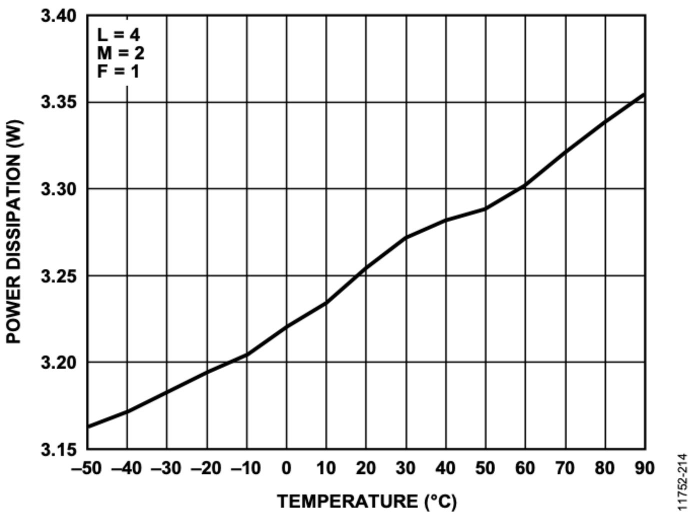


Figure 53. Power Dissipation vs. Temperature

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AVDD1 = 1.25 V, AVDD1_SR = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, 1.7 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, default SPI settings, clock divider = 2, T_A = 25°C, 128k FFT sample, unless otherwise noted. See Table 10 for recommended settings.

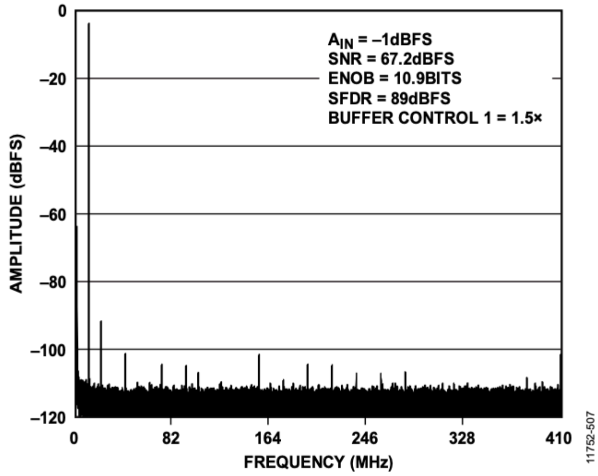

Figure 55. Single-Tone FFT with f_{IN} = 10.3 MHz

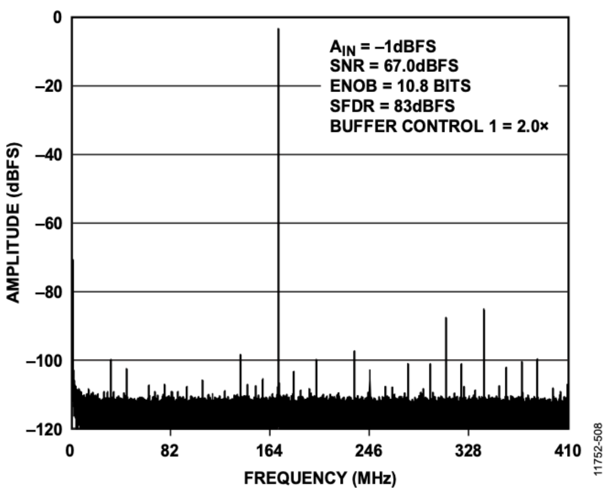

Figure 56. Single-Tone FFT with f_{IN} = 170.3 MHz

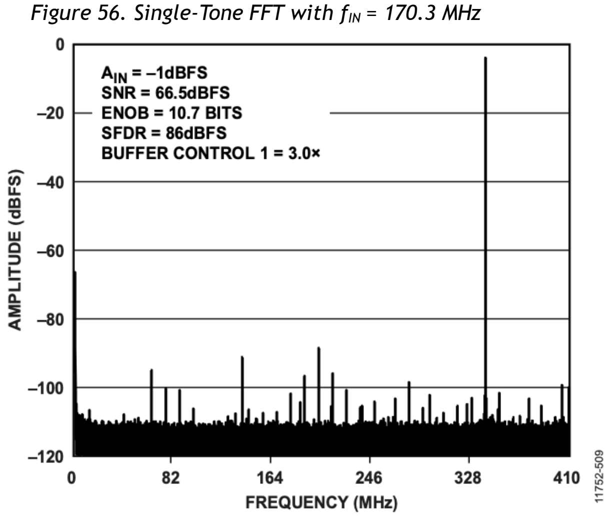

Figure 57. Single-Tone FFT with f_{IN} = 340.3 MHz

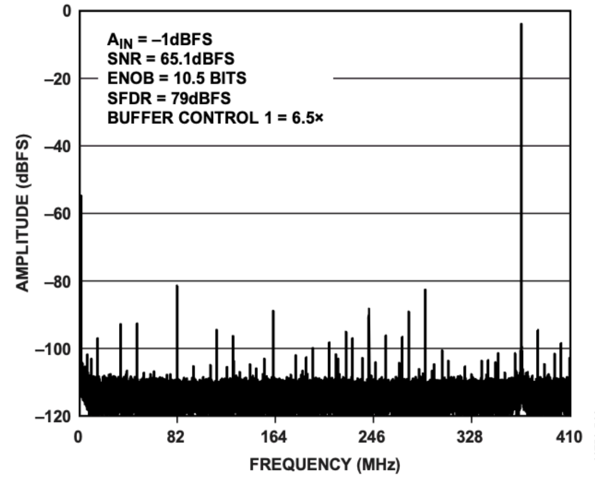

Figure 58. Single-Tone FFT with f_{IN} = 450.3 MHz

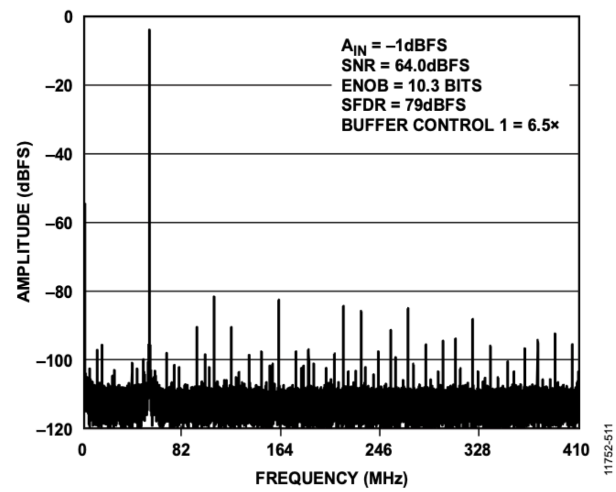

Figure 59. Single-Tone FFT with f_{IN} = 765.3 MHz

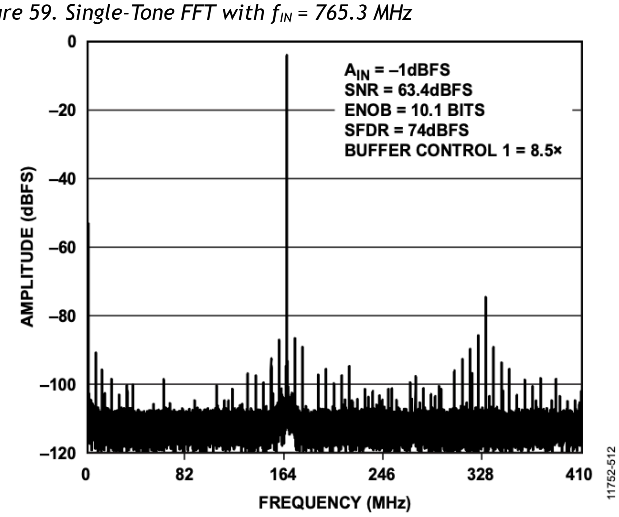

Figure 60. Single-Tone FFT with f_{IN} = 985.3 MHz

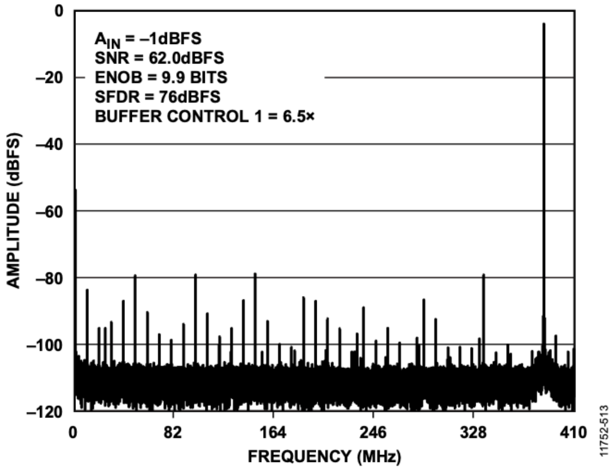

Figure 61. Single-Tone FFT with f_{IN} = 1205.3 MHz

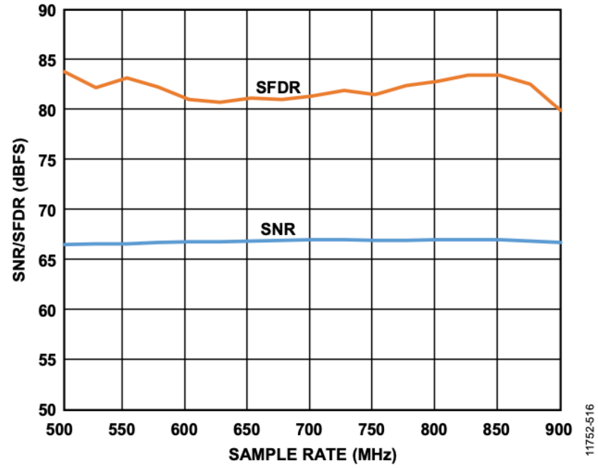

Figure 64. SNR/SFDR vs. f_S, f_{IN} = 170.3 MHz; Buffer Control 1 (0x018) = 3.0×

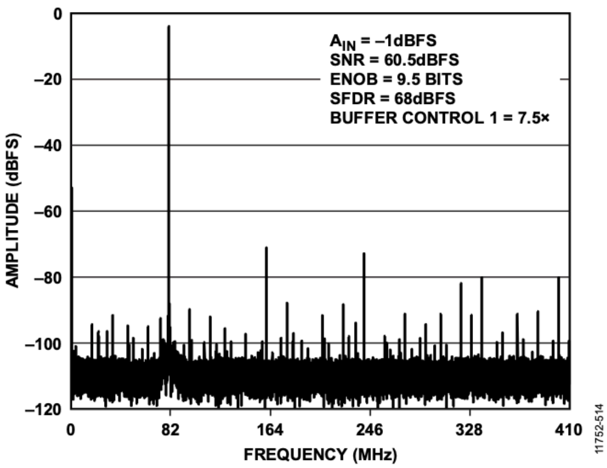

Figure 62. Single-Tone FFT with f_{IN} = 1720.3 MHz

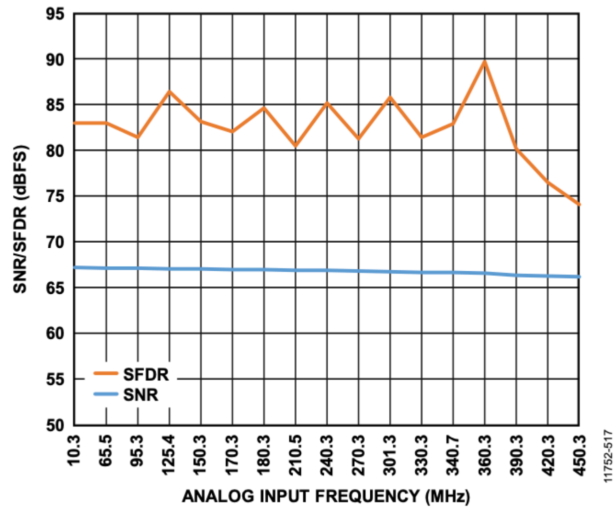

Figure 65. SNR/SFDR vs. f_{IN}; f_{IN} < 450 MHz; Buffer Control 1 (0x018) = 3.0×

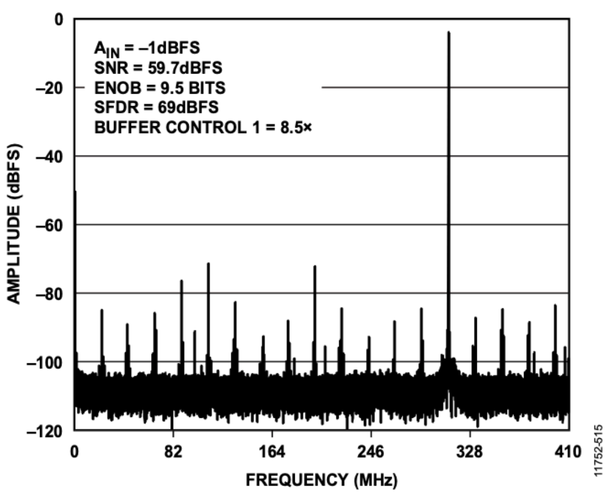

Figure 63. Single-Tone FFT with f_{IN} = 1950.3 MHz

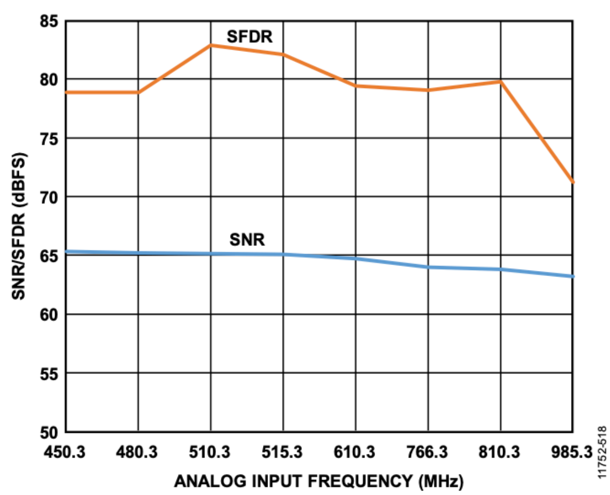

Figure 66. SNR/SFDR vs. f_{IN}; 450 MHz < f_{IN} < 1 GHz; Buffer Control 1 (0x018) = 6.5×

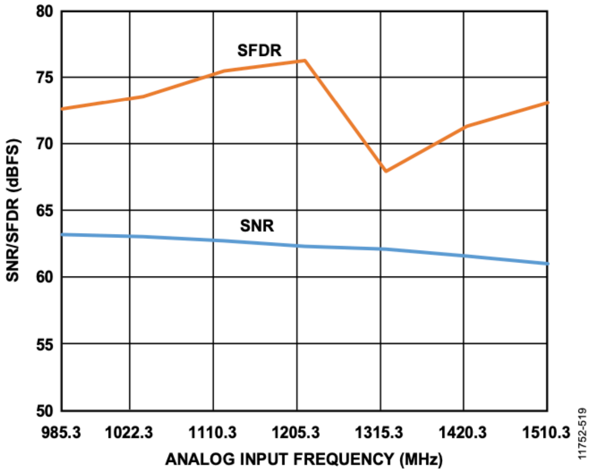

Figure 67. SNR/SFDR vs. f_{IN}; 1 GHz < f_{IN} < 1.5 GHz; Buffer Control 1 (0x018) = 6.5×

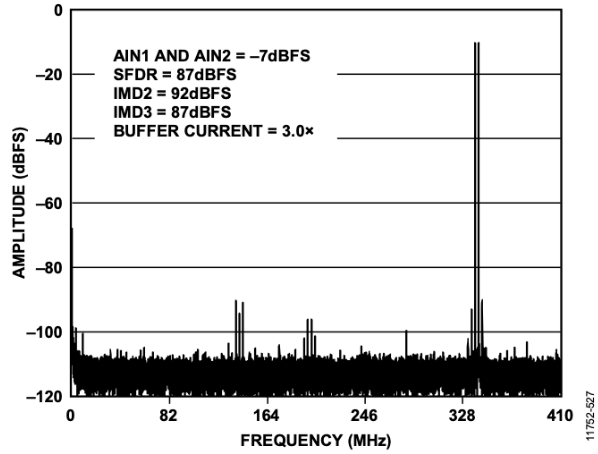

Figure 70. Two-Tone FFT; f_{IN1} = 338 MHz, f_{IN2} = 341 MHz

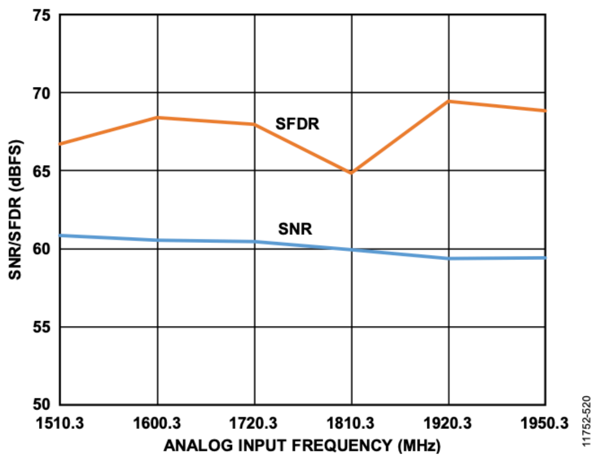

Figure 68. SNR/SFDR vs. f_{IN}; 1.5 GHz < f_{IN} < 2 GHz; Buffer Control 1 (0x018) = 8.5×

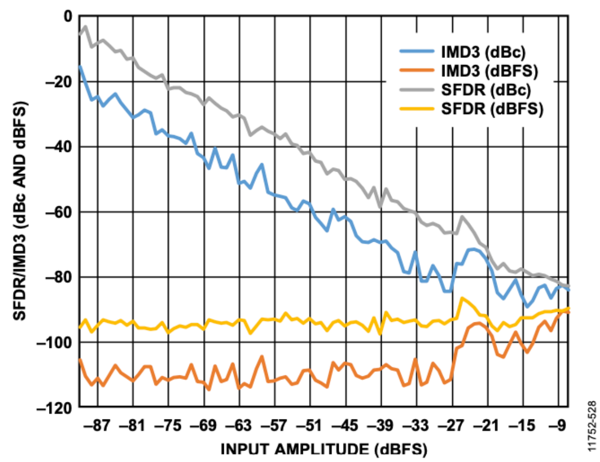

Figure 71. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

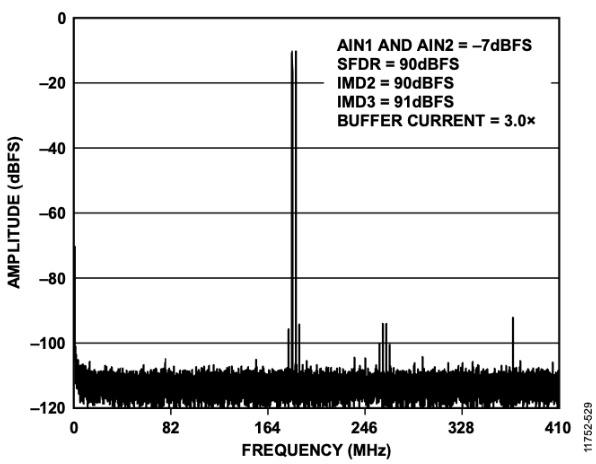

Figure 69. Two-Tone FFT; f_{IN1} = 184 MHz, f_{IN2} = 187 MHz

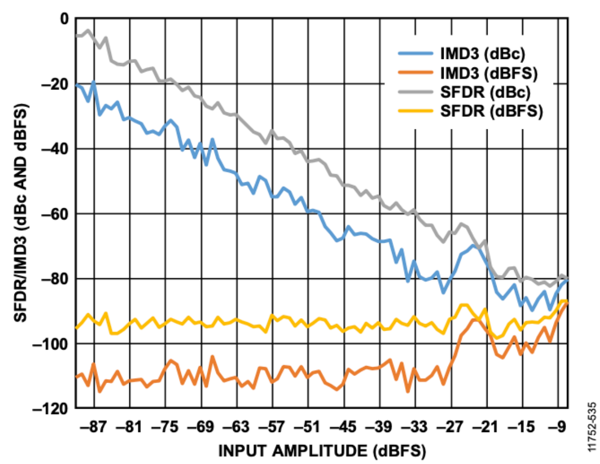

Figure 72. Two-Tone IMD3/SFDR vs. Input Amplitude (A_{IN}) with f_{IN1} = 338 MHz and f_{IN2} = 341 MHz

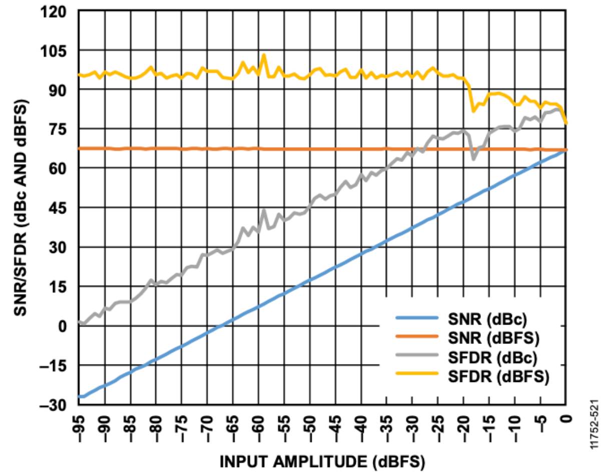

Figure 73. SNR/SFDR vs. Chiplon Input Level, f_{IN} = 170.3 MHz

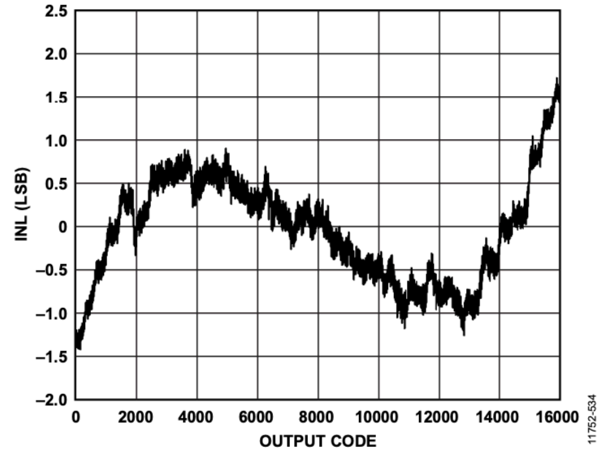

Figure 75. INL, f_{IN} = 10.3 MHz

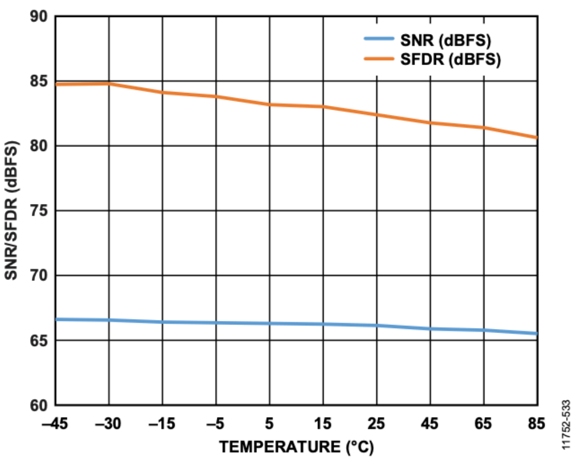

Figure 74. SNR/SFDR vs. Temperature, f_{IN} = 170.3 MHz

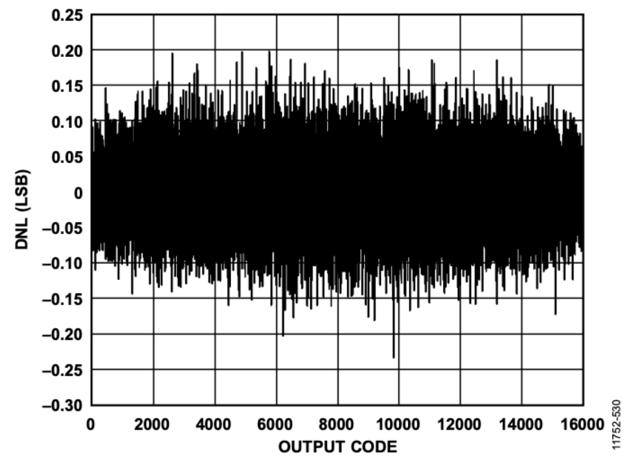

Figure 76. DNL, f_{IN} = 15 MHz

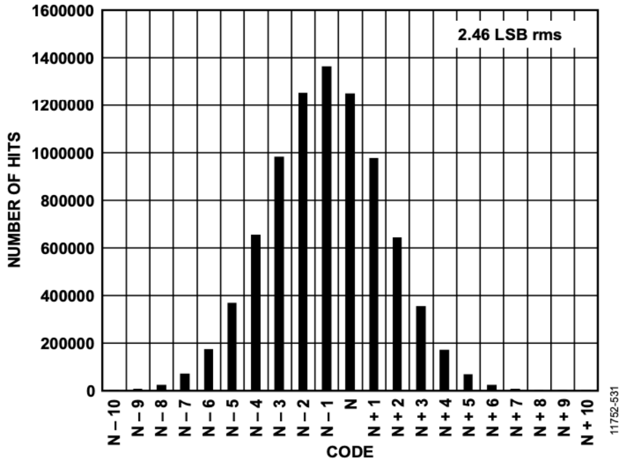

Figure 77. Input-Referred Noise Histogram

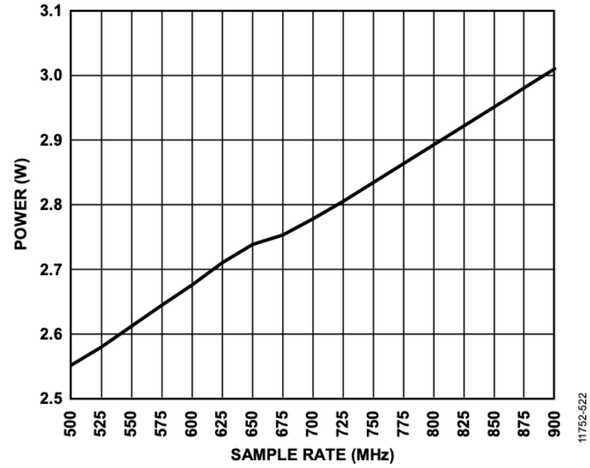

Figure 79. Power Dissipation vs. f_S ; L = 4, M = 2, F = 1 for $f_S \geq$ 625 MSPS and L = 2, M = 2, F = 2 for $f_S <$ 625 MSPS (Default SPI)

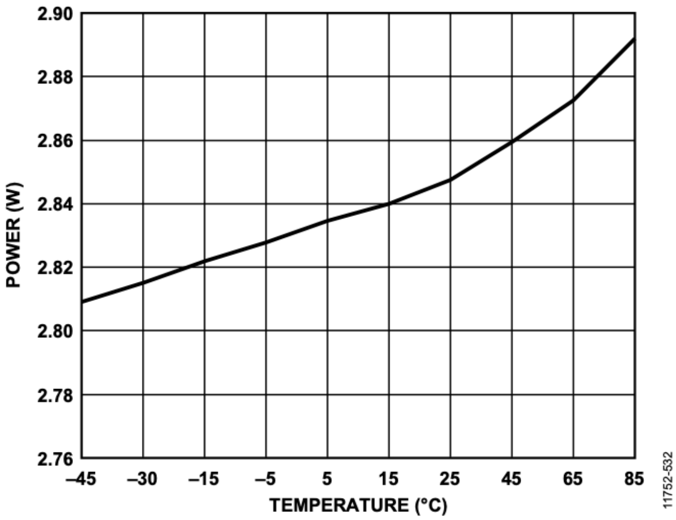

Figure 78. Power Dissipation vs. Temperature

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AVDD1 = 1.25 V, AVDD1_SR = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, 2.06 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, default SPI settings, clock divider = 2, T_A = 25°C, 128k FFT sample, unless otherwise noted. See Table 10 for recommended settings.

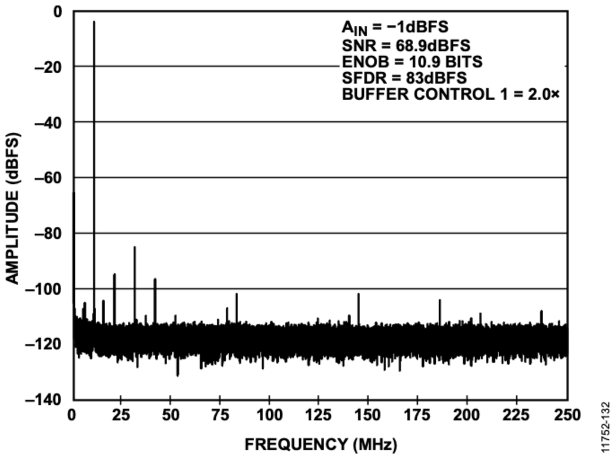


Figure 80. Single-Tone FFT with f_{IN} = 10.3 MHz

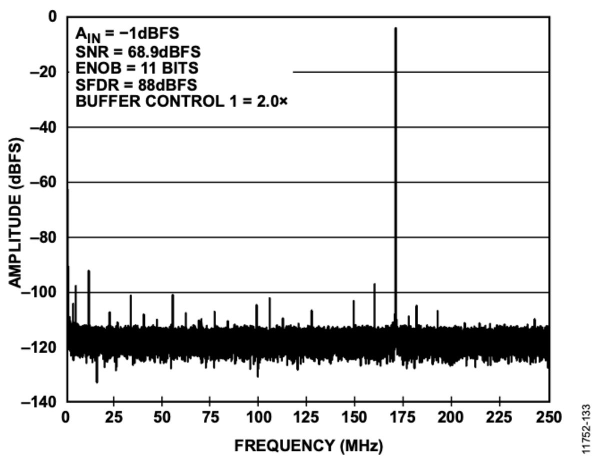


Figure 81. Single-Tone FFT with f_{IN} = 170.3 MHz

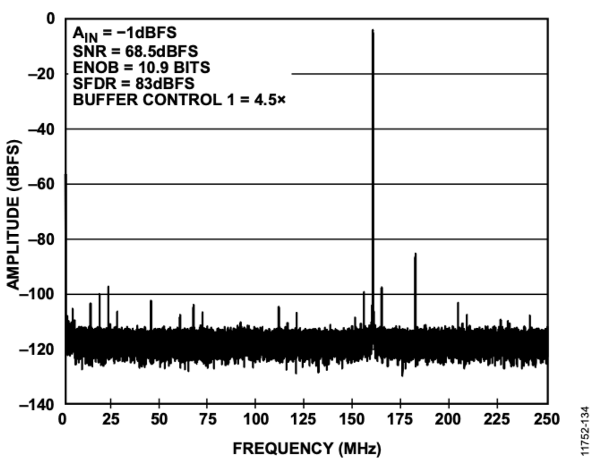


Figure 82. Single-Tone FFT with f_{IN} = 340.3 MHz

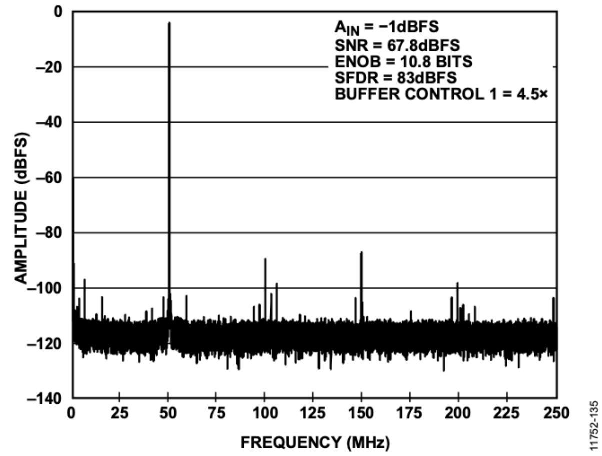


Figure 83. Single-Tone FFT with f_{IN} = 450.3 MHz

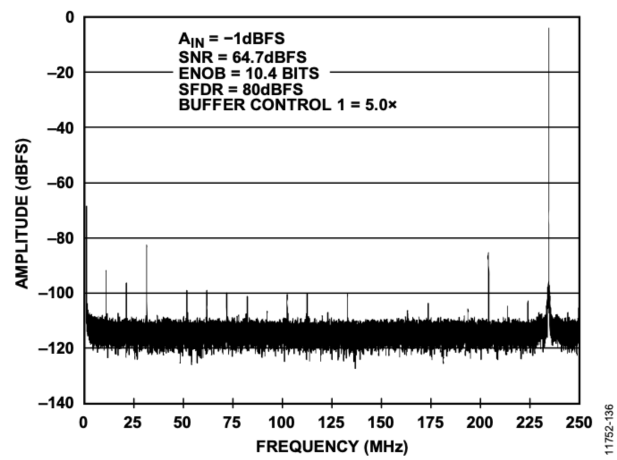


Figure 84. Single-Tone FFT with f_{IN} = 765.3 MHz

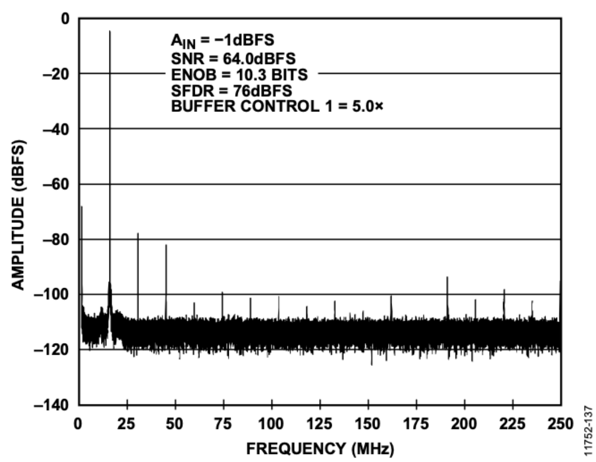


Figure 85. Single-Tone FFT with f_{IN} = 985.3 MHz

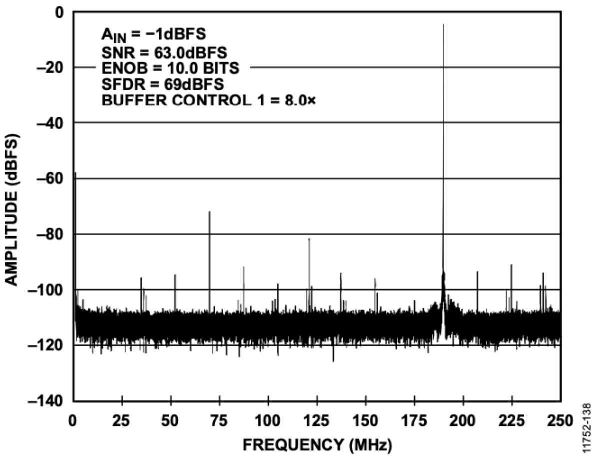


Figure 86. Single-Tone FFT with f_{IN} = 1310.3 MHz

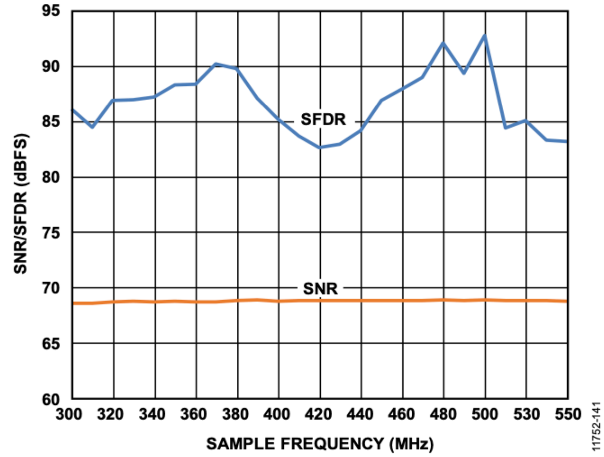


Figure 89. SNR/SFDR vs. f_S, f_{IN} = 170.3 MHz; Buffer Control 1 = 2.0×

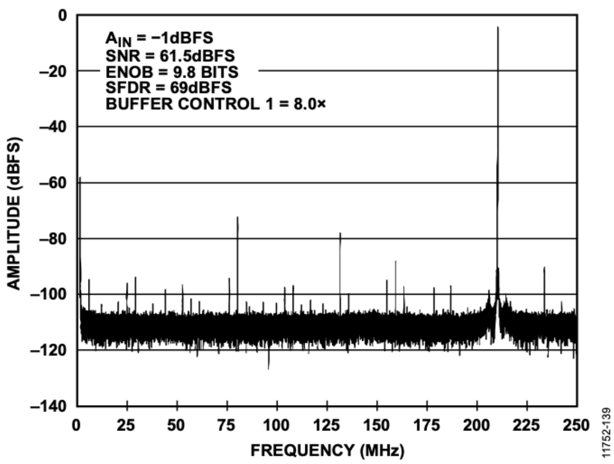


Figure 87. Single-Tone FFT with f_{IN} = 1710.3 MHz

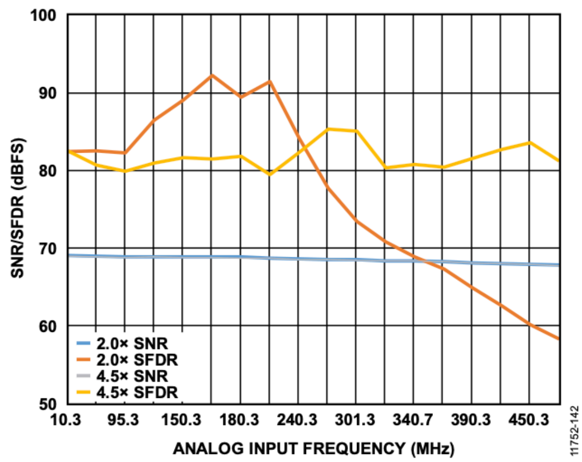


Figure 90. SNR/SFDR vs. f_{IN}; f_{IN} < 500 MHz; Buffer Control 1 (0x018) = 2.0× and 4.5×

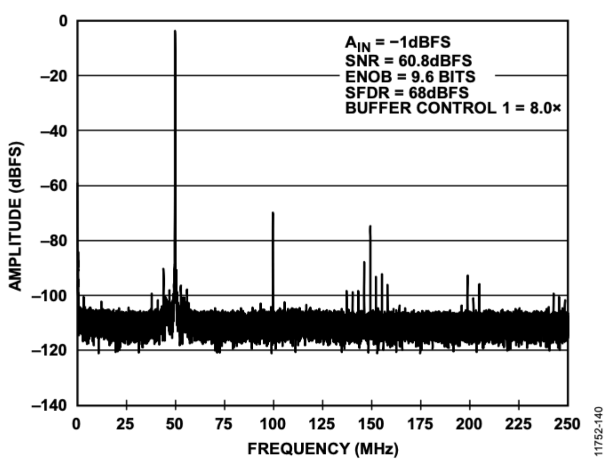


Figure 88. Single-Tone FFT with f_{IN} = 1950.3 MHz

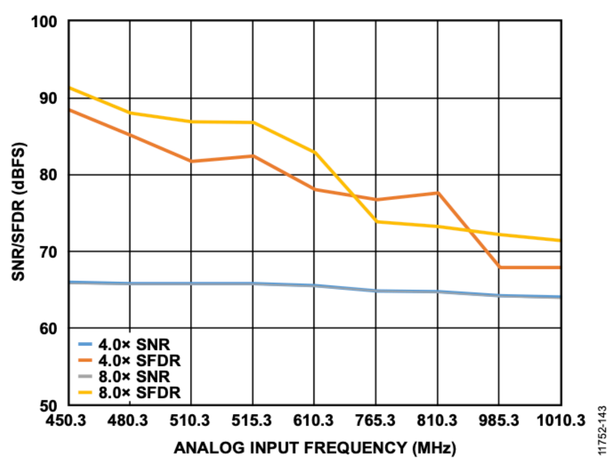


Figure 91. SNR/SFDR vs. f_{IN}; 500 MHz < f_{IN} < 1 GHz; Buffer Control 1 (0x018) = 4.0× and 8.0×

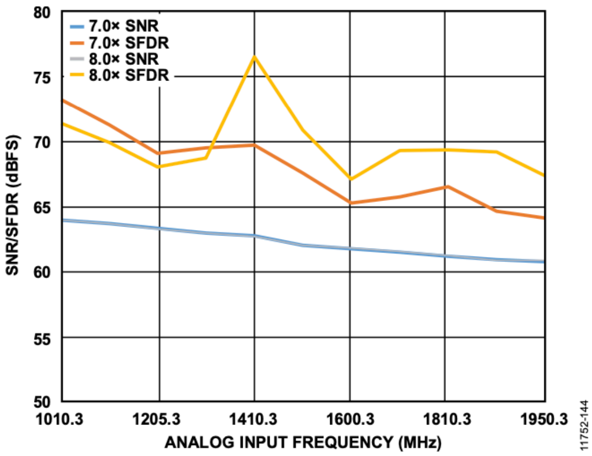


Figure 92. SNR/SFDR vs. f_{IN}; 1 GHz < f_{IN} < 2 GHz; Buffer Control 1 (0x018) = 7.0× and 8.0×

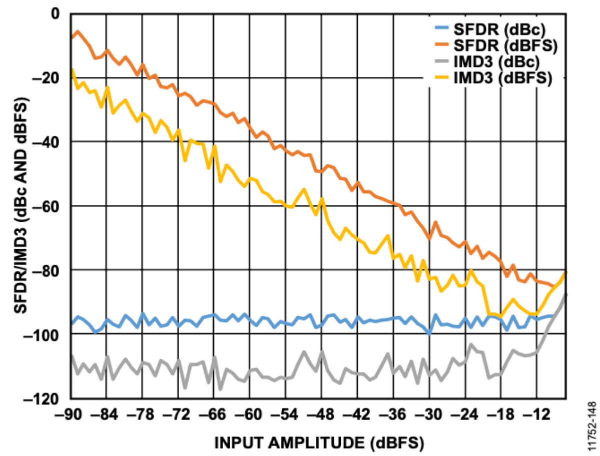


Figure 95. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

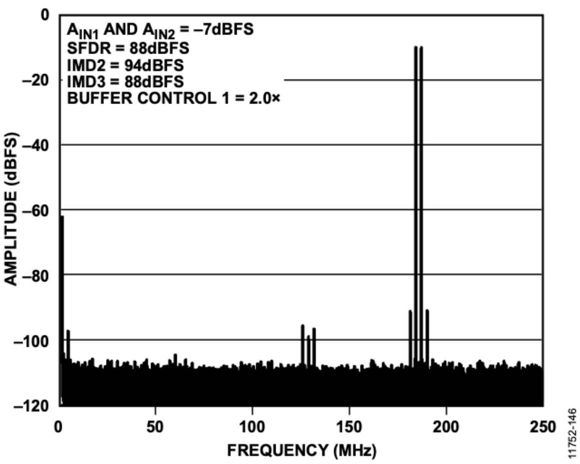


Figure 93. Two-Tone FFT; f_{IN1} = 184 MHz, f_{IN2} = 187 MHz

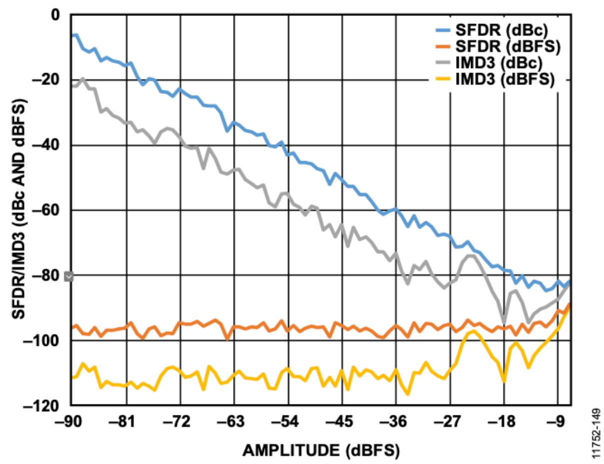


Figure 96. Two-Tone IMD3/SFDR vs. Input Amplitude (A_{IN}) with f_{IN1} = 338 MHz and f_{IN2} = 341 MHz

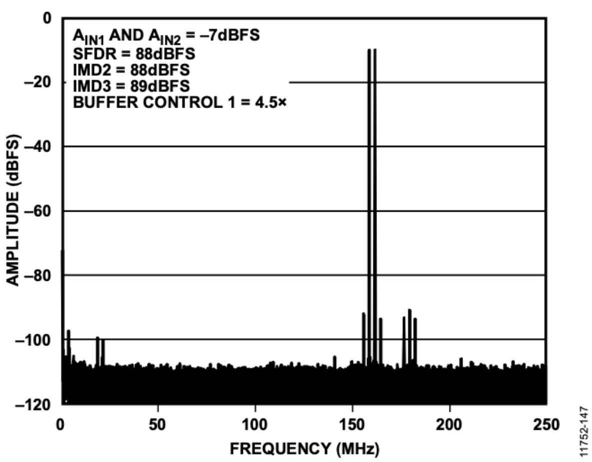


Figure 94. Two-Tone FFT; f_{IN1} = 338 MHz, f_{IN2} = 341 MHz

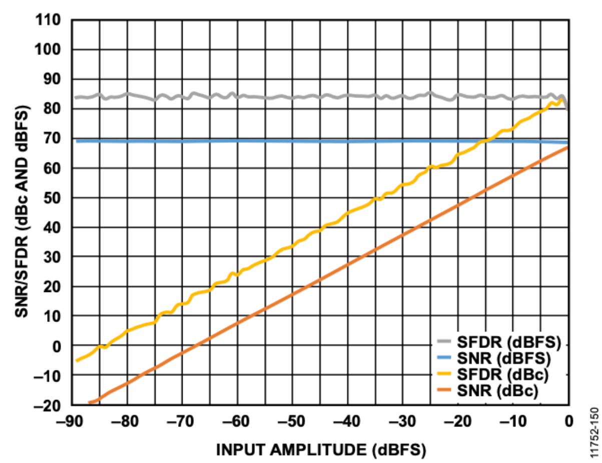


Figure 97. SNR/SFDR vs. Chiplon Input Level, f_{IN} = 170.3 MHz

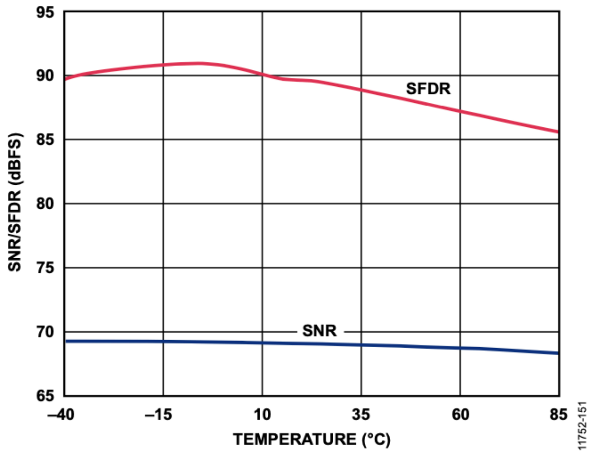


Figure 98. SNR/SFDR vs. Temperature, f_{IN} = 170.3 MHz

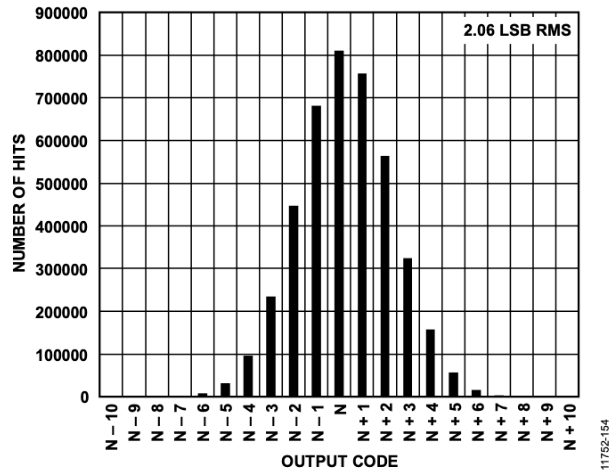


Figure 101. Input-Referred Noise Histogram

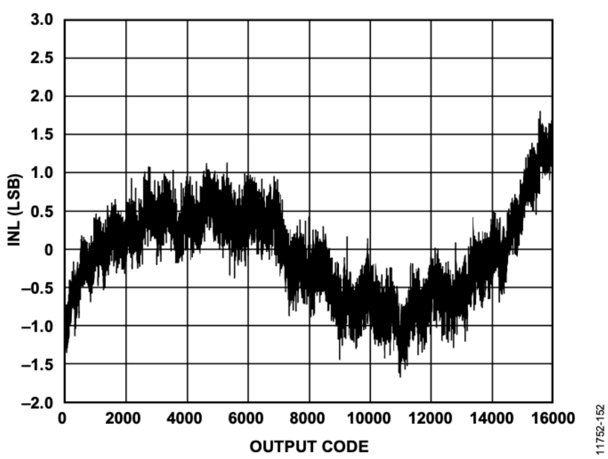


Figure 99. INL, f_{IN} = 10.3 MHz

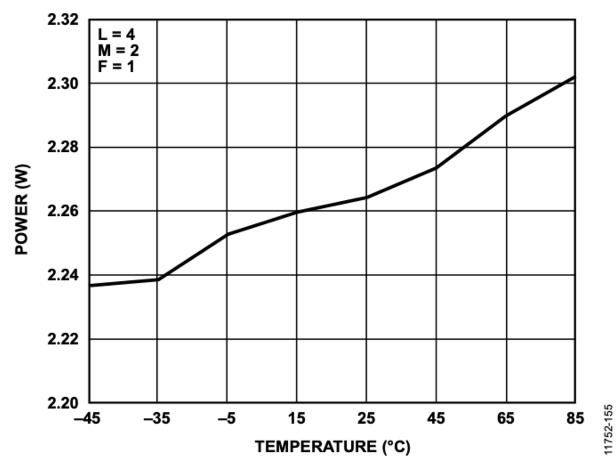


Figure 102. Power Dissipation vs. Temperature

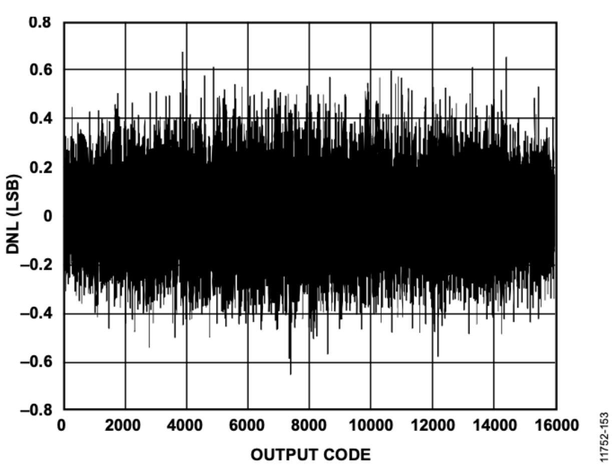


Figure 100. DNL, f_{IN} = 15 MHz

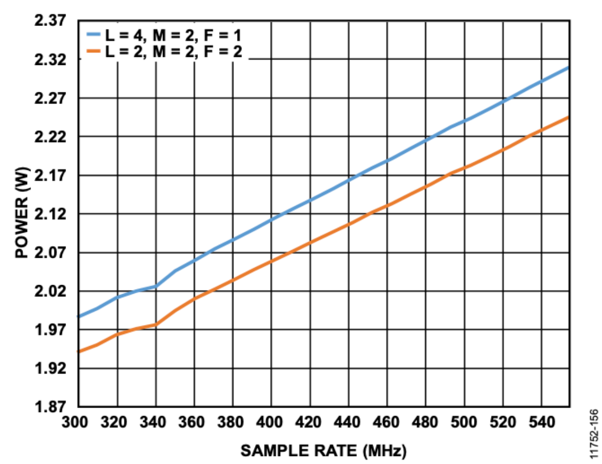


Figure 103. Power Dissipation vs. f_S

EQUIVALENT CIRCUITS

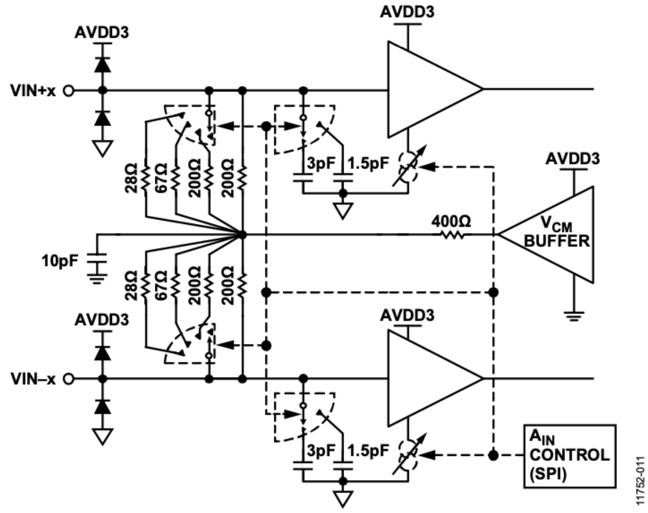


Figure 104. Chiplon Inputs

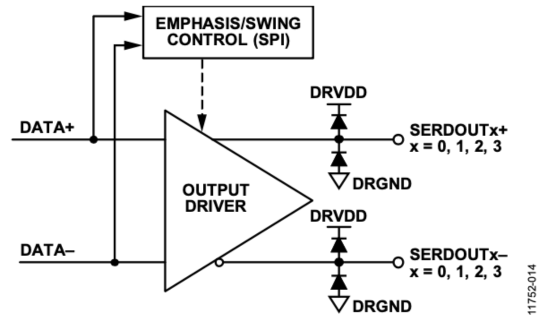


Figure 107. Digital Outputs

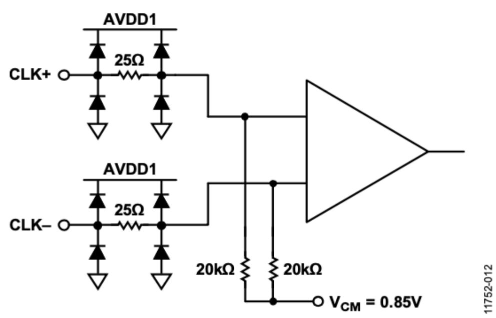


Figure 105. Clock Inputs

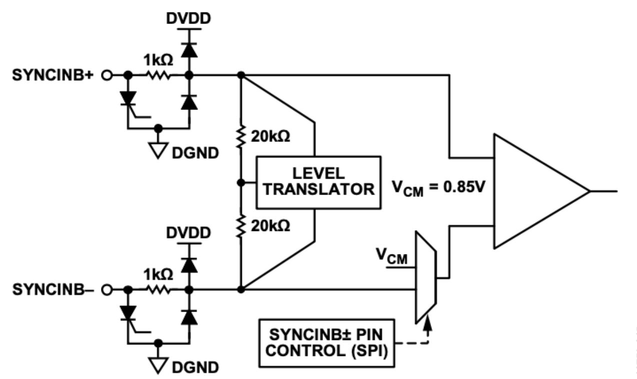


Figure 108. SYNCINB± Inputs

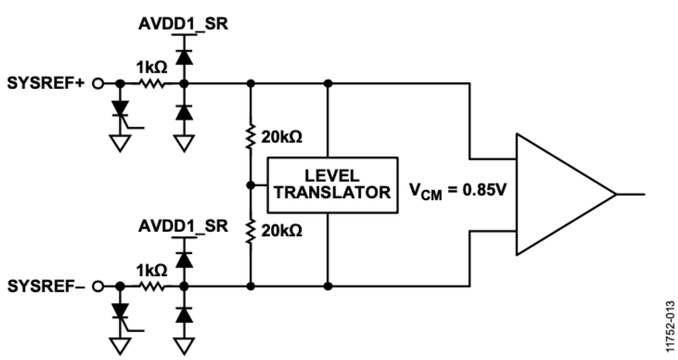


Figure 106. SYSREF± Inputs

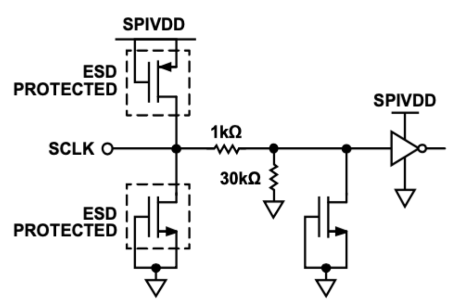


Figure 109. SCLK Input

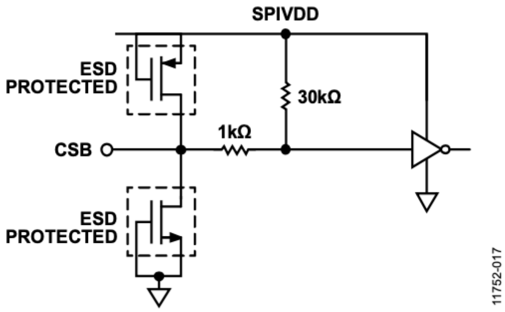


Figure 110. CSB Input

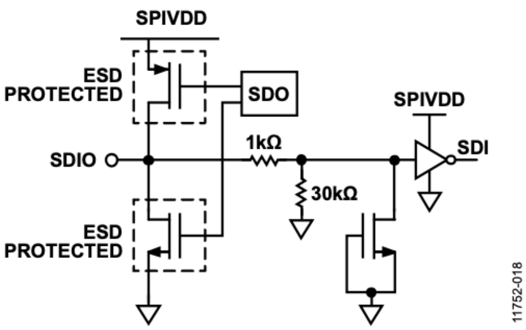


Figure 111. SDIO Input

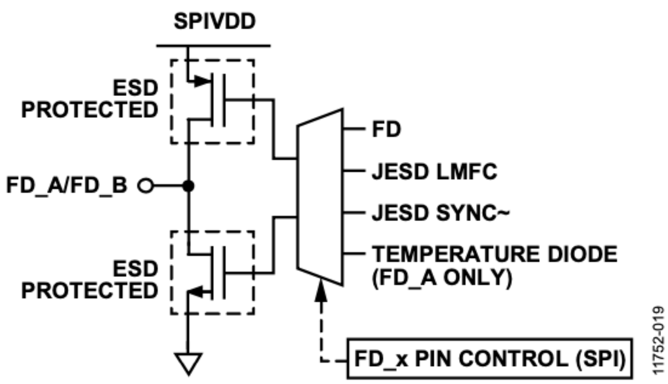


Figure 112. FD_A/FD_B Outputs

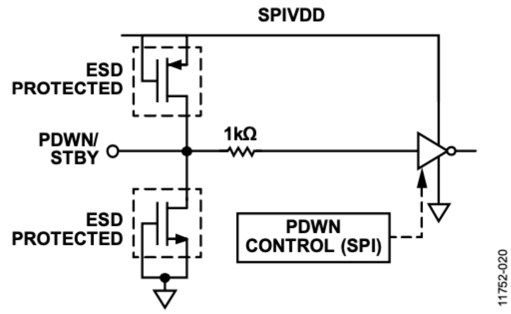


Figure 113. PDWN/STBY Input

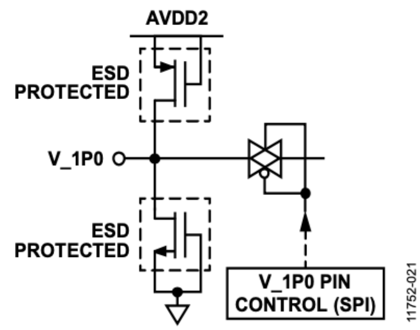


Figure 114. V_1P0 Input/Output

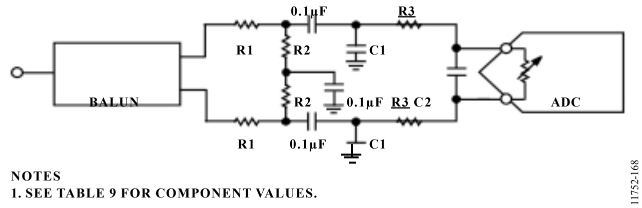


Figure 115. Differential Transformer-Coupled Configuration for CLM9680BCPZ

Table 9. Differential Transformer-Coupled Input Configuration Component Values

Device	Frequency Range	Transformer	R1 (Ω)	R2 (Ω)	R3 (Ω)	C1 (pF)	C2 (pF)
CLM9680BCPZ-500	DC to 250 MHz	ETC1-1-13	10	50	10	4	2
	250 MHz to 2 GHz	BAL-0006/BAL-0006SMG	10	50	10	4	2
CLM9680BCPZ-820	DC to 410 MHz	ETC1-1-13	10	50	10	4	2
	410 MHz to 2 GHz	BAL-0006/BAL-0006SMG	10	50	10	4	2
CLM9680BCPZ-1000	DC to 500 MHz	ETC1-1-13/BAL-0006SMG	25	25	10	4	2
	500 MHz to 2 GHz	BAL-0006/BAL-0006SMG	25	25	0	Open	Open
CLM9680BCPZ-1250	DC to 625 MHz	BAL-0006SMG	10	50	15	4	2
	625 MHz to 2 GHz	BAL-0006SMG	10	50	0	Open	Open

Input Common Mode

The Chiplon inputs of the CLM9680BCPZ are internally biased to the common mode as shown in Figure 116. The common-mode buffer has a limited range in that the performance suffers greatly if the common-mode voltage drops by more than 100 mV. Therefore, in dc-coupled applications, set the common-mode voltage to 2.05 V, ±100 mV to ensure proper ADC operation. The full-scale voltage setting must be at a 1.7 V p-p differential

if running in a dc-coupled application.

Chiplon Input Buffer Controls and SFDR Optimization

The CLM9680BCPZ input buffer offers flexible controls for the Chiplon inputs, such as input termination, buffer current, and input full- scale adjustment. All the available controls are shown in Figure 116.

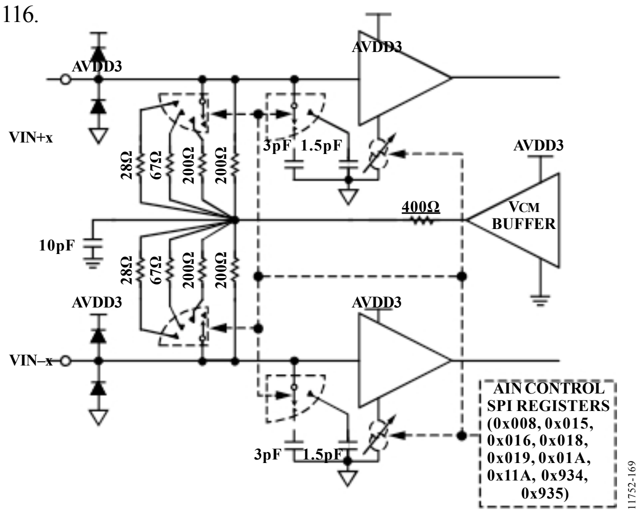


Figure 116. Chiplon Input Controls

Using the 0x018, 0x019, 0x01A, 0x11A, 0x934, and 0x935 registers, the buffer behavior on each channel can be adjusted to optimize the SFDR over various input frequencies and bandwidths of interest.

Input Buffer Control Registers (0x018, 0x019, 0x01A, 0x935, 0x934, 0x11A)

The input buffer has many registers that set the bias currents and other settings for operation at different frequencies. These bias currents and settings can be changed to suit the input frequency range of operation. Register 0x018 controls the buffer bias current to help with the kickback from the ADC core. This setting can be scaled from a low setting of 1.0× to a high setting of 8.5×. The default setting is 3.0× for the CLM9680BCPZ-1000 and CLM9680BCPZ-820, and 2.0× for the CLM9680BCPZ-500. These settings are sufficient for operation in the first Nyquist zone for the products. When the input buffer current in Register 0x018 is set, the amount of current required by the AVDD3 supply changes. This relationship is shown in Figure 117. For a complete list of buffer current

settings, see Table 39.

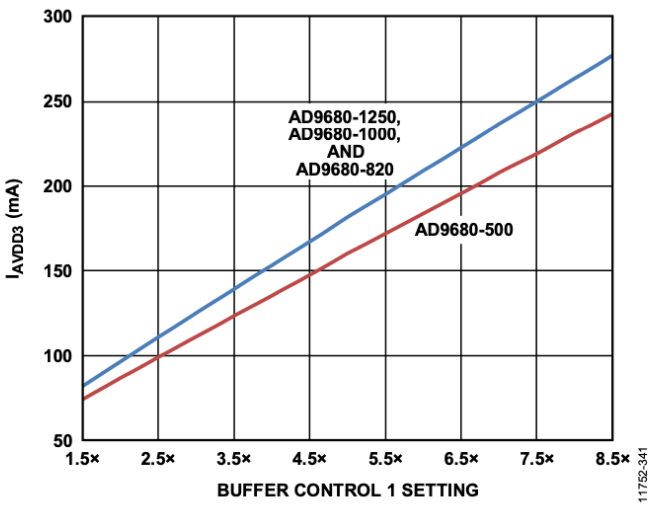


Figure 117. I_{AVDD3} vs. Buffer Control 1 Setting in Register 0x018

The 0x019, 0x01A, 0x11A, and 0x935 registers offer secondary bias controls for the input buffer for frequencies >500 MHz. Register 0x934 can be used to reduce input capacitance to achieve wider signal bandwidth but may result in slightly lower linearity and noise performance. These register settings do not impact the AVDD3 power as much as Register 0x018 does. For frequencies <500 MHz, it is recommended to use the default settings for these registers. Table 10 shows the recommended values for the buffer current control registers for various speed grades.

Register 0x11A is used when sampling in higher Nyquist zones (>500 MHz for the CLM9680BCPZ-1000). This setting enables the ADC sampling network to optimize the sampling and settling times internal to the ADC for high frequency operation. For frequencies greater than 500 MHz, it is recommended to operate the ADC core at a 1.46 V full-scale setting irrespective of the speed grade. This setting offers better SFDR without any significant penalty in SNR.

Figure 118, Figure 119, and Figure 120 show the SFDR vs. Chiplon input frequency for various buffer settings for the CLM9680BCPZ-1250. The recommended settings shown in Table 10 were used to take the data while changing the contents of Register 0x018 only.

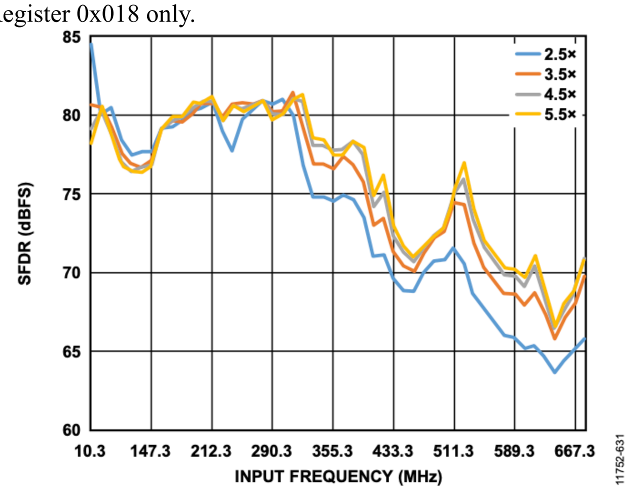


Figure 118. Buffer Current Sweeps, CLM9680BCPZ-1250 (SFDR vs. I_{BUFF}); f_{IN} < 500 MHz; Front-End Network Shown in Figure 115

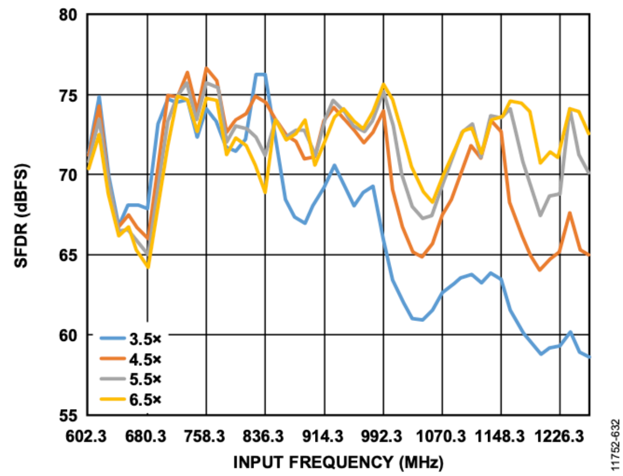


Figure 119. Buffer Current Sweeps, CLM9680BCPZ-1250 (SFDR vs. I_{BUFF}); 600 MHz < f_{IN} < 1300 MHz; Front-End Network Shown in Figure

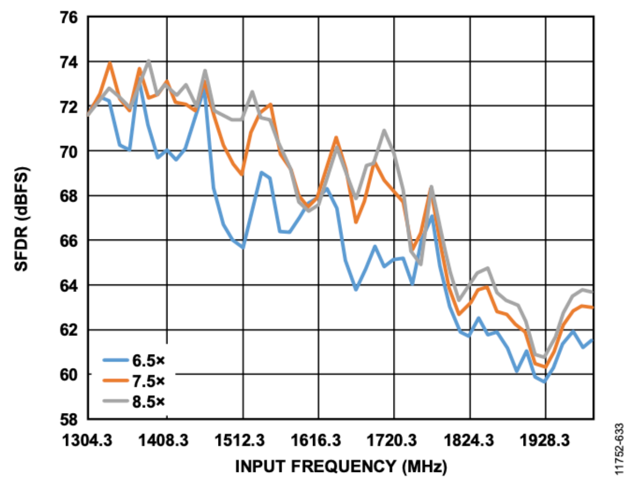


Figure 120. Buffer Current Sweeps, CLM9680BCPZ-1250 (SFDR vs. I_{BUFF}); 1300 MHz < f_{IN} < 2000 MHz; Front-End Network Shown in Figure 115

Figure 121, Figure 122, and Figure 123 show the SFDR vs. Chiplon input frequency for various buffer settings for the CLM9680BCPZ-1000. The recommended settings shown in Table 10 were used to take the data while changing the contents of Register 0x018 only.

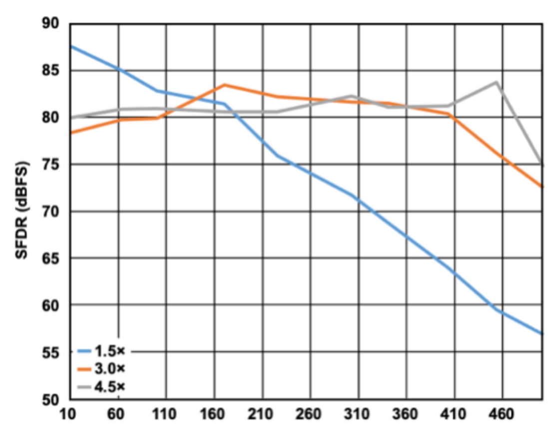


Figure 121. Buffer Current Sweeps, CLM9680BCPZ-1000 (SFDR vs. I_{BUFF}); f_{IN} < 500 MHz; Front-End Network Shown in Figure 115

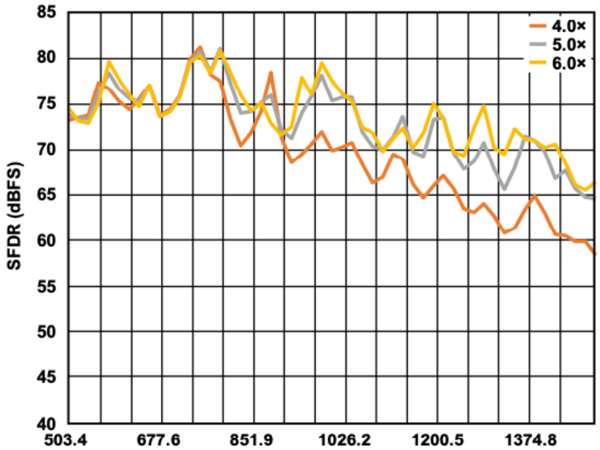


Figure 122. Buffer Current Sweeps, CLM9680BCPZ-1000 (SFDR vs. I_{BUFF}); 500 MHz < f_{IN} < 1500 MHz; Front-End Network Shown in Figure 115

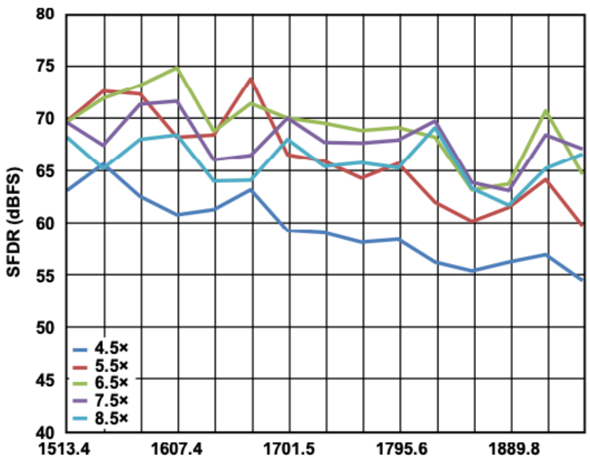


Figure 123. Buffer Current Sweeps, CLM9680BCPZ-1000 (SFDR vs. I_{BUFF}); 1500 MHz < f_{IN} < 2000 MHz; Front-End Network Shown in Figure 115

In certain high frequency applications, the SFDR can be improved by reducing the full-scale setting, as shown in Table 10. At high frequencies, the performance of the ADC core is limited by jitter. The SFDR can be improved by backing off of the full scale level. Figure 124 shows the SFDR and SNR vs. full-scale input level at different high frequencies for the CLM9680BCPZ-1000.

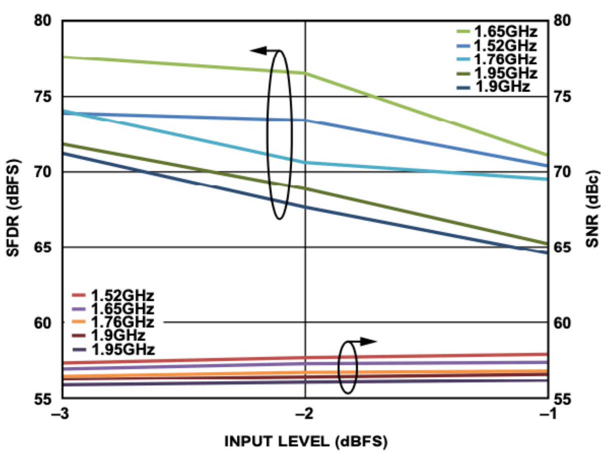


Figure 124. SNR/SFDR vs. Chiplon Input Level vs. Input Frequencies, CLM9680BCPZ-1000

Figure 125, Figure 126, and Figure 127 show the SFDR vs. Chiplon input frequency for various buffer settings for the CLM9680BCPZ-820. The recommended settings shown in Table 10 were used to take the data while changing the contents of Register 0x018 only.

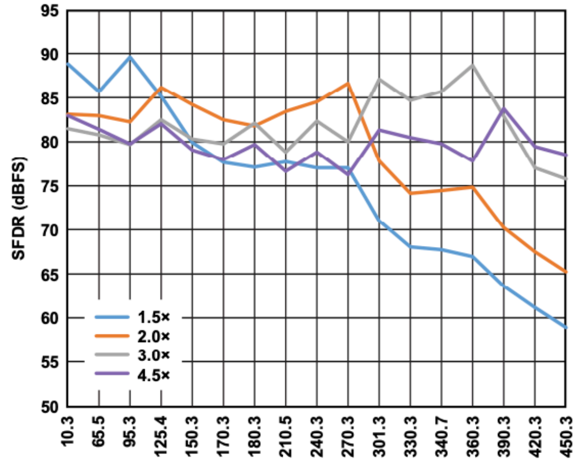


Figure 125. Buffer Current Sweeps, CLM9680BCPZ-820 (SFDR vs. I_{BUFF}); f_{IN} < 500 MHz; Front-End Network Shown in Figure 115

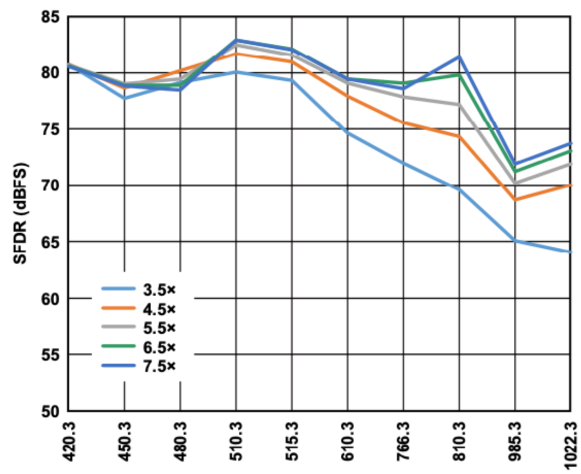


Figure 126. Buffer Current Sweeps, CLM9680BCPZ-820 (SFDR vs. I_{BUFF}); 500 MHz < f_{IN} < 1000 MHz; Front-End Network Shown in Figure 115

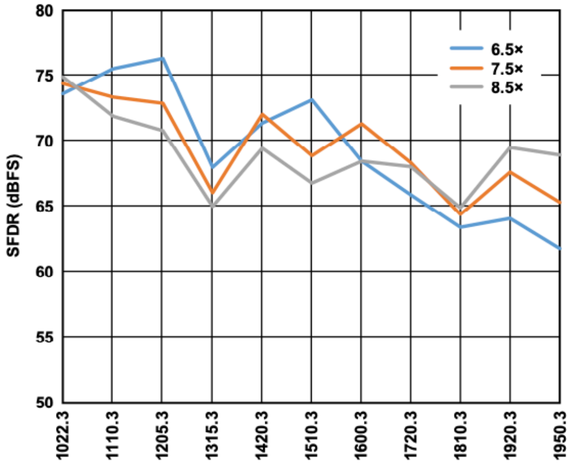


Figure 127. Buffer Current Sweeps, CLM9680BCPZ-820 (SFDR vs. I_{BUFF}); 1000 MHz < f_{IN} < 2000 MHz; Front-End Network Shown in Figure 115

Figure 128, Figure 129, and Figure 130 show the SFDR vs. Chiplon input frequency for various buffer settings for the CLM9680BCPZ-500. The recommended settings shown in Table 10 were used to take the data while changing the contents of Register 0x018 only.

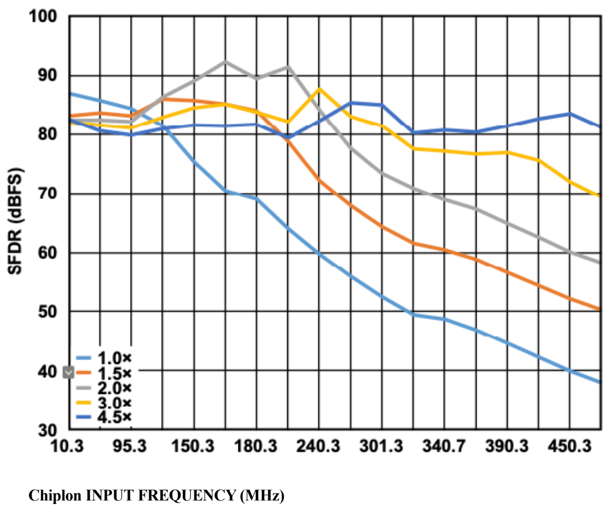


Figure 128. Buffer Current Sweeps, CLM9680BCPZ-500 (SFDR vs. I_{BUFF}); f_{IN} < 500 MHz; Front-End Network Shown in Figure 115 Buffer Control 1

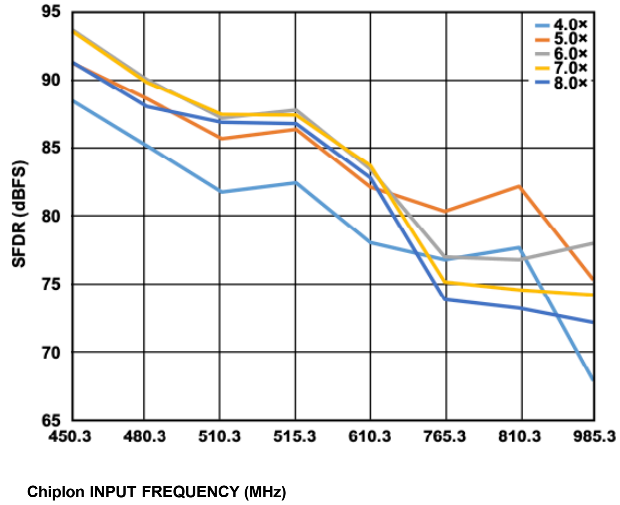


Figure 129. Buffer Current Sweeps, CLM9680BCPZ-500 (SFDR vs. I_{BUFF}); 450 MHz < f_{IN} < 1000 MHz; Front-End Network Shown in Figure 115

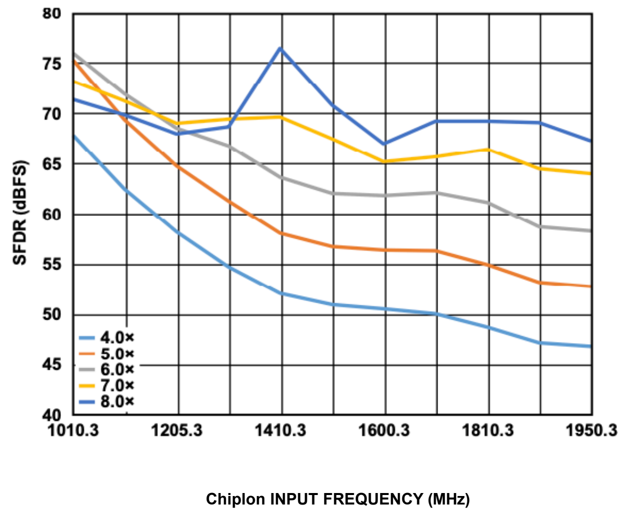


Figure 130. Buffer Current Sweeps, CLM9680BCPZ-500 (SFDR vs. I_{BUFF}); 1 GHz < f_{IN} < 2 GHz; Front-End Network Shown in Figure 115

Table 10. Recommended Register Settings for SFDR Optimization at Different Input Frequencies

		Buffer Control1 (0x018)—Buffer Current Control	Buffer Control2 (0x019)—Buffer Bias Setting	Buffer Control3 (0x01A)—Buffer Bias Setting	Buffer Control4 (0x11A)—High Frequency Setting	Buffer Control5 (0x935)—Low Frequency Setting	Input Full-Scale Range (0x025)	Input Full-Scale Control (0x030)	Input Termination	Input Capacitance
CLM9680BCPZ-500	DC to 250 MHz	0x20 (2.0×)	0x60 (Setting 3)	0x0A (Setting 3)	0x00 (off)	0x04 (on)	0x0C (2.06 V p-p)	0x04	0x0C/0x1C/…	0x1F
	250 MHz to 500 MHz	0x70 (4.5×)	0x60 (Setting 3)	0x0A (Setting 3)	0x00 (off)	0x04 (on)	0x0C (2.06 V p-p)	0x04	0x0C/0x1C/…	0x1F
	500 MHz to 1 GHz	0x80 (5.0×)	0x40 (Setting 1)	0x08 (Setting 1)	0x00 (off)	0x00 (off)	0x08 (1.46 V p-p)	0x18	0x0C/0x1C/…	0x1F or 0x00[2]
	1 GHz to 2 GHz	0xF0 (8.5×)	0x40 (Setting 1)	0x08 (Setting 1)	0x00 (off)	0x00 (off)	0x08 (1.46 V p-p)	0x18	0x0C/0x1C/…	0x1F or 0x00[1]
CLM9680BCPZ-820	DC to 200 MHz	0x10 (1.5×)	0x40 (Setting 1)	0x09 (Setting 2)	0x00 (off)	0x04 (on)	0x0A (1.70 V p-p)	0x14	0x0C/0x1C/…	0x1F
	DC to 410 MHz	0x40 (3.0×)	0x40 (Setting 1)	0x09 (Setting 2)	0x00 (off)	0x04 (on)	0x0A (1.70 V p-p)	0x14	0x0C/0x1C/…	0x1F
	500 MHz to 1 GHz	0x80 (5.0×)	0x40 (Setting 1)	0x08 (Setting 1)	0x00 (off)	0x00 (off)	0x08 (1.46 V p-p)	0x18	0x0C/0x1C/…	0x1F or 0x00[2]
	1 GHz to 2 GHz	0xF0 (8.5×)	0x40 (Setting 1)	0x08 (Setting 1)	0x00 (off)	0x00 (off)	0x08 (1.46 V p-p)	0x18	0x0C/0x1C/…	0x1F or 0x00[1]
CLM9680BCPZ-1000	DC to 150 MHz	0x10 (1.5×)	0x50 (Setting 2)	0x09 (Setting 2)	0x00 (off)	0x04 (on)	0x0A (1.70 V p-p)	0x18	0x0E/0x1E/…	0x1F
	DC to 500 MHz	0x40 (3.0×)	0x50 (Setting 2)	0x09 (Setting 2)	0x00 (off)	0x04 (on)	0x0A (1.70 V p-p)	0x18	0x0E/0x1E/…	0x1F
	500 MHz to 1 GHz	0xA0 (6.0×)	0x60 (Setting 3)	0x09 (Setting 2)	0x20 (on)	0x00 (off)	0x08 (1.46 V p-p)	0x18	0x0E/0x1E/…	0x1F or 0x00[1]
	1 GHz to 2 GHz	0xD0 (7.5×)	0x70 (Setting 4)	0x09 (Setting 2)	0x20 (on)	0x00 (off)	0x08 (1.46 V p-p)	0x18	0x0E/0x1E/…	0x1F or 0x00[1]
CLM9680BCPZ-1250	DC to 625 MHz	0x50 (3.5×)	0x50 (Setting 2)	0x09 (Setting 2)	0x00 (off)	0x04 (on)	0x0A (1.58 V p-p)	0x18	0x0E/0x1E/…	0x1F
	>625 MHz	0xA0 (6.0×)	0x50 (Setting 2)	0x09 (Setting 2)	N/A[3]	0x00 (off)	0x08 (1.46 V p-p)	0x18	0x0E/0x1E/…	0x1F or 0x00[1]

[1] The input termination can be changed to accommodate the application with little or no impact to ac performance.
[2] The input capacitance can be set to 1.5 pF to achieve wider input bandwidth but results in slightly lower ac performance.
[3] N/A means not applicable.

Absolute Maximum Input Swing

The absolute maximum input swing allowed at the inputs of the CLM9680BCPZ is 4.3 V p-p differential. Signals operating near or at this level can cause permanent damage to the ADC.

VOLTAGE REFERENCE

A stable and accurate 1.0 V voltage reference is built into the CLM9680BCPZ. This internal 1.0 V reference is used to set the full- scale input range of the ADC. The full-scale input range can be adjusted via the ADC Function Register 0x025. For more information on adjusting the input swing, see Table 39. Figure 131 shows the block diagram of the internal 1.0 V reference controls.

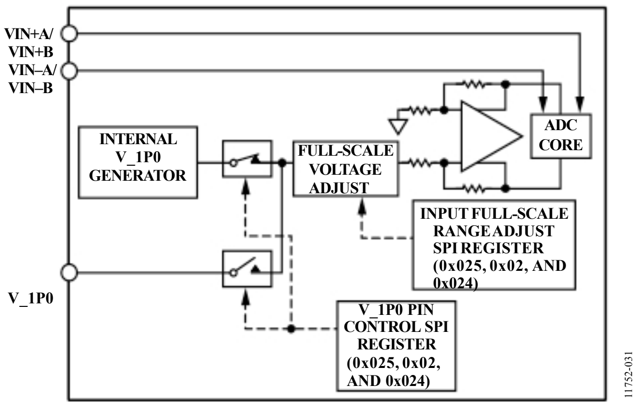


Figure 131. Internal Reference Configuration and Controls

The SPI Register 0x024 enables the user to either use this internal 1.0 V reference, or to provide an external 1.0 V reference. When using an external voltage reference, provide a 1.0 V reference. The full-scale adjustment is made using the SPI, irrespective of the reference voltage. For more information on adjusting the full-scale level of the CLM9680BCPZ, refer to the Memory Map Register Table section.

The use of an external reference may be necessary, in some applications, to enhance the gain accuracy of the ADC or to improve thermal drift characteristics. Figure 132 shows the typical drift characteristics of the internal 1.0 V reference.

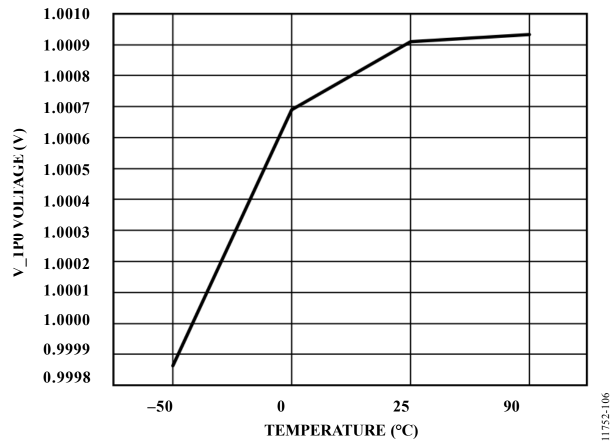


Figure 132. Typical V_1P0 Drift

The external reference must be a stable 1.0 V reference. The ADR130 is a good option for providing the 1.0 V reference. Figure 133 shows how the ADR130 can be used to provide the external 1.0 V reference to the CLM9680BCPZ. The grayed out areas show unused blocks within the CLM9680BCPZ while using the ADR130 to provide the external reference.

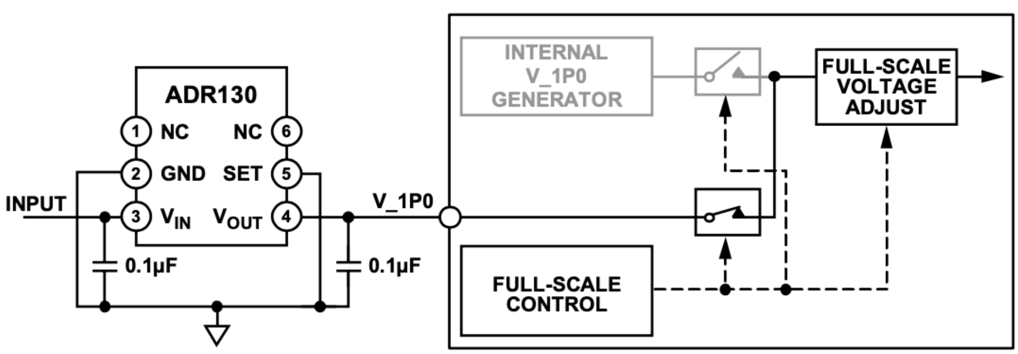


Figure 133. External Reference Using ADR130

CLOCK INPUT CONSIDERATIONS

For optimum performance, drive the CLM9680BCPZ sample clock inputs (CLK+ and CLK−) with a differential signal. This signal is typically ac-coupled to the CLK+ and CLK− pins via a transformer or clock drivers. These pins are biased internally and require no additional biasing.

Figure 134 shows a preferred method for clocking the CLM9680BCPZ. The low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer.

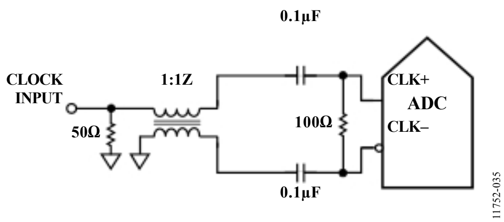


Figure 134. Transformer-Coupled Differential Clock

Another option is to ac couple a differential CML or LVDS signal to the sample clock input pins, as shown in Figure 135 and Figure 136.

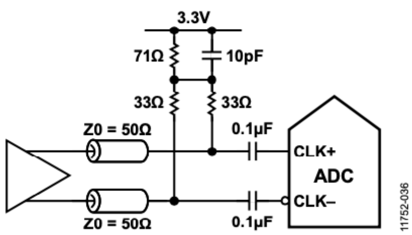


Figure 135. Differential CML Sample Clock

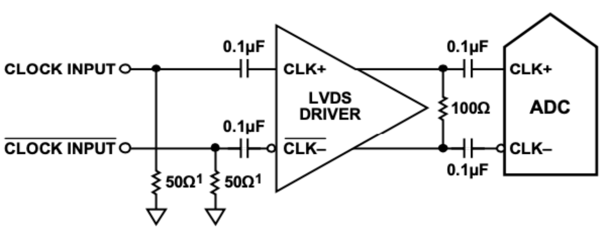


Figure 136. Differential LVDS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. In applications where the clock duty cycle cannot be guaranteed to be 50%, a higher multiple frequency clock can be supplied to the device. The CLM9680BCPZ can be clocked at 2 GHz with the internal clock divider set to 2. The output of the divider offers a 50% duty cycle, high slew rate (fast edge) clock signal to the internal ADC. See the Memory Map section for more details on using this feature.

Input Clock Divider

The CLM9680BCPZ contains an input clock divider with the ability to divide the Nyquist input clock by 1, 2, 4, and 8. The divider ratios can be selected using Register 0x10B. This is shown in Figure 137.

The maximum frequency at the CLK± inputs is 4 GHz. This is the limit of the divider. In applications where the clock input is a multiple of the sample clock, care must be taken to program the appropriate divider ratio into the clock divider before applying the clock signal. This ensures that the current transients during device startup are controlled.

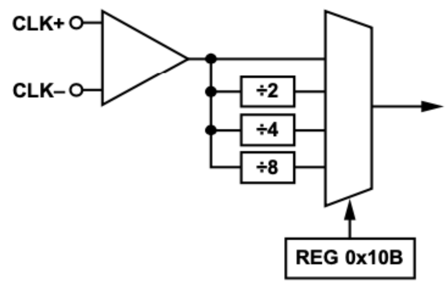


Figure 137. Clock Divider Circuit

The CLM9680BCPZ clock divider can be synchronized using the external SYSREF± input. A valid SYSREF± causes the clock divider to reset to a programmable state. This synchronization feature allows multiple devices to have their clock dividers aligned to guarantee simultaneous input sampling. See the Memory Map section for more information.

Input Clock Divider 1⁄2 Period Delay Adjust

The input clock divider inside the CLM9680BCPZ provides phase delay in increments of 1⁄2 the input clock cycle. Register 0x10C can be programmed to enable this delay independently for each channel. Changing this register does not affect the stability of the JESD204B link.

Clock Fine Delay Adjust

The CLM9680BCPZ sampling edge instant can be adjusted by writing to Register 0x117 and Register 0x118. Setting Bit 0 of Register 0x117 enables the feature, and Bits[7:0] of Register 0x118 set the value of the delay. This value can be programmed individually for each channel. The clock delay can be adjusted from −151.7 ps to +150 ps in ~1.7 ps increments. The clock delay adjust takes effect immediately when it is enabled via SPI writes. Enabling the clock fine delay adjust in Register 0x117 causes a datapath reset. However, the contents of Register 0x118 can be changed without affecting the stability of the JESD204B link.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (fA) due only to aperture jitter (tJ) can be calculated by

$SNR = 20 \times \log 10(2 \times \pi \times fA \times tJ)$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, Chiplon input signal, and ADC aperture jitter specifications.

IF undersampling applications are particularly sensitive to jitter (see Figure 138).

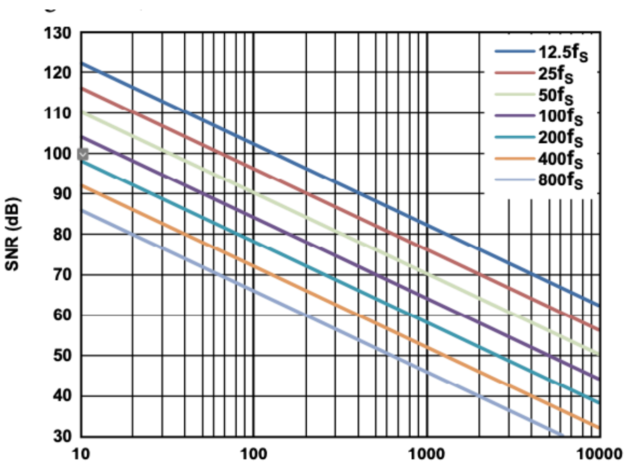


Figure 138. Ideal SNR vs. Input Frequency and Jitter

Treat the clock input as an Chiplon signal in cases where aperture jitter may affect the dynamic range of the CLM9680BCPZ. Separate power supplies for clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. If the clock is generated from another type of source (by gating, dividing, or other methods), retime the clock by the original clock at the last step. Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs.

Figure 139 shows the estimated SNR of the CLM9680BCPZ-1000 across input frequency for different clock induced jitter values. The SNR can be estimated by using the following equation:

$$SNR\,(\text{dBFS}) = 10\log\left[10^{\left(\frac{-SNR_{ADC}}{10}\right)} + 10^{\left(\frac{-SNR_{JITTER}}{10}\right)}\right]$$

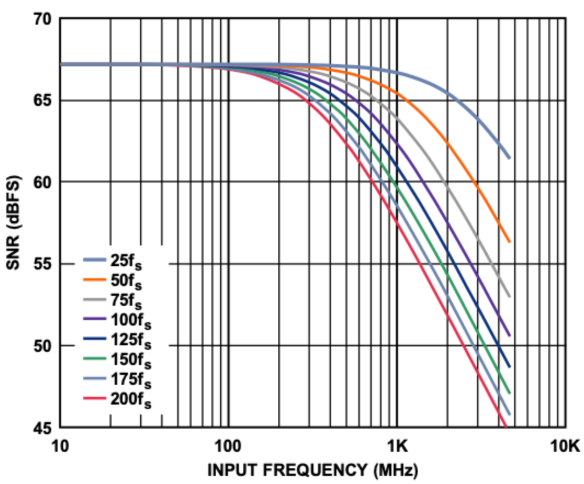


Figure 139. Estimated SNR Degradation for the CLM9680BCPZ-1000 vs. Input Frequency and RMS Jitter

Power-Down/Standby Mode

The CLM9680BCPZ has a PDWN/STBY pin that can be used to configure the device in power-down or standby mode. The default operation is PDWN. The PDWN/STBY pin is a logic high pin. When in power-down mode, the JESD204B link is

Power-Down/Standby Mode

The CLM9680BCPZ has a PDWN/STBY pin that can be used to configure the device in power-down or standby mode. The default operation is PDWN. The PDWN/STBY pin is a logic high pin. When in power-down mode, the JESD204B link is disrupted. The power-down option can also be set via Register 0x03F and Register 0x040.

In standby mode, the JESD204B link is not disrupted and transmits zeros for all converter samples. This can be changed using Register 0x571, Bit 7 to select /K/ characters.

Temperature Diode

The CLM9680BCPZ contains a diode-based temperature sensor for measuring the temperature of the die. This diode can output a voltage and serve as a coarse temperature sensor to monitor the internal die temperature.

The temperature diode voltage can be output to the FD_A pin using the SPI. Use Register 0x028, Bit 0 to enable or disable the diode. Register 0x028 is a local register. Channel A must be selected in the device index register (0x008) to enable the temperature diode readout. Configure the FD_A pin to output the diode voltage by programming Register 0x040[2:0]. See Table 39 for more information.

The voltage response of the temperature diode (SPIVDD = 1.8 V) is shown in Figure 140.

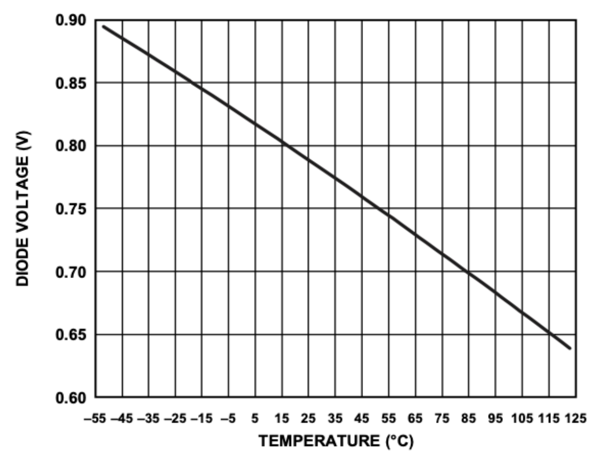


Figure 140. Temperature Diode Voltage vs. Temperature

ADC OVERRANGE AND FAST DETECT

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to be clipped. The standard overrange bit in the JESD204B outputs provides information on the state of the Chiplon input that is of limited usefulness. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip actually occurs. In addition, because input signals can have significant slew rates, the latency of this function is of major concern. Highly pipelined converters can have significant latency. The CLM9680BCPZ contains fast detect circuitry for individual channels to monitor the threshold and assert the FD_A and FD_B pins.

ADC OVERRANGE

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange indicator can be embedded within the JESD204B link as a control bit (when CSB > 0). The latency of this overrange indicator matches the sample latency.

The CLM9680BCPZ also records any overrange condition in any of the eight virtual converters. For more information on the virtual converters, refer to Figure 146. The overrange status of each virtual converter is registered as a sticky bit in Register 0x563. The contents of Register 0x563 can be cleared using Register 0x562, by toggling the bits corresponding to the virtual converter to set and reset position.

FAST THRESHOLD DETECTION (FD_A AND FD_B)

The FD bit is immediately set whenever the absolute value of the input signal exceeds the programmable upper threshold level. The FD bit is only cleared when the absolute value of the input signal drops below the lower threshold level for greater than the programmable dwell time. This feature provides hysteresis and prevents the FD bit from excessively toggling.

The operation of the upper threshold and lower threshold registers, along with the dwell time registers, is shown in Figure 141.

The FD indicator is asserted if the input magnitude exceeds the value programmed in the fast detect upper threshold registers, located at Register 0x247 and Register 0x248. The selected threshold register is compared with the signal magnitude at the output of the ADC. The fast upper threshold detection has a latency of 28 clock cycles (maximum). The approximate upper threshold magnitude is defined by

$$\text{Upper Threshold Magnitude (dBFS)} = 20 \log (\text{Threshold Magnitude}/2^{13})$$

The FD indicators are not cleared until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold registers, located at Register 0x249 and Register 0x24A. The fast detect lower threshold register is a 13-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC pipeline latency, but is accurate in terms of converter resolution. The lower threshold magnitude is defined by

$$\text{Lower Threshold Magnitude (dBFS)} = 20 \log (\text{Threshold Magnitude}/2^{13})$$

For example, to set an upper threshold of −6 dBFS, write 0xFFF to Register 0x247 and Register 0x248. To set a lower threshold of −10 dBFS, write 0xA1D to Register 0x249 and Register 0x24A.

The dwell time can be programmed from 1 to 65,535 sample clock cycles by placing the desired value in the fast detect dwell time registers, located at Register 0x24B and Register 0x24C. See the Memory Map section (Register 0x040, and Register 0x245 to Register 0x24C in Table 39) for more details.

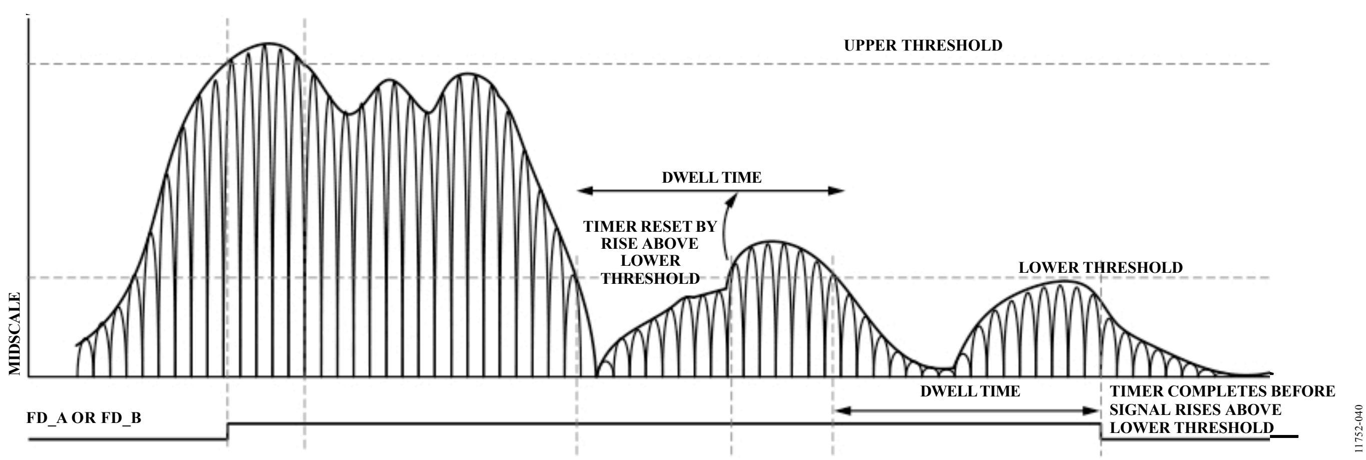


Figure 141. Threshold Settings for FD_A and FD_B Signals

SIGNAL MONITOR

The signal monitor block provides additional information about the signal being digitized by the ADC. The signal monitor computes the peak magnitude of the digitized signal. This information can be used to drive an AGC loop to optimize the range of the ADC in the presence of real-world signals.

The results of the signal monitor block can be obtained either by reading back the internal values from the SPI port or by embedding the signal monitoring information into the JESD204B interface as special control bits. A global, 24-bit programmable period controls the duration of the measurement. Figure 142 shows the simplified block diagram of the signal monitor block.

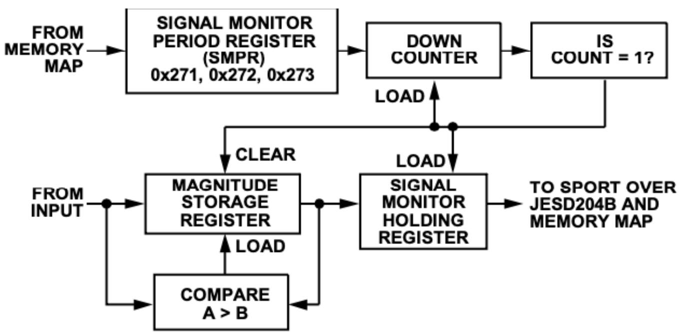


Figure 142. Signal Monitor Block

The peak detector captures the largest signal within the observation period. The detector only observes the magnitude of the signal. The resolution of the peak detector is a 13-bit value, and the observation period is 24 bits and represents converter output samples. The peak magnitude can be derived by using the following equation:

$$\text{Peak Magnitude (dBFS)} = 20\log(\text{Peak Detector Value}/2^{13})$$

The magnitude of the input port signal is monitored over a programmable time period, which is determined by the signal monitor period register (SMPR). The peak detector function is enabled by setting Bit 1 of Register 0x270 in the signal monitor control register. The 24-bit SMPR must be programmed before activating this mode.

After enabling peak detection mode, the value in the SMPR is loaded into a monitor period timer, which decrements at the decimated clock rate. The magnitude of the input signal is compared with the value in the internal magnitude storage register (not accessible to the user), and the greater of the two is updated as the current peak level. The initial value of the magnitude storage register is set to the current ADC input signal magnitude. This comparison continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the 13-bit peak level value is transferred to the signal monitor holding register, which can be read through the memory map or output through the SPORT over the JESD204B interface. The monitor period timer is reloaded with the value in the SMPR, and the countdown restarts. In addition, the magnitude of the first input sample is updated in the magnitude storage register, and the comparison and update procedure, as explained previously, continues.

SPORT OVER JESD204B

The signal monitor data can also be serialized and sent over the JESD204B interface as control bits. These control bits must be deserialized from the samples to reconstruct the statistical data. The signal control monitor function is enabled by setting Bits[1:0] of Register 0x279 and Bit 1 of Register 0x27A. Figure 143 shows two different example configurations for the signal monitor control bit locations inside the JESD204B samples. A maximum of three control bits can be inserted into the JESD204B samples; however, only one control bit is required for the signal monitor. Control bits are inserted from MSB to LSB. If only one control bit is to be inserted (CS = 1), only the most significant control bit is used (see Example Configuration 1 and Example Configuration 2 in Figure 143). To select the SPORT over JESD204B option, program Register 0x559, Register 0x55A, and Register 0x58F. See Table 39 for more information on setting these bits.

Figure 144 shows the 25-bit frame data that encapsulates the peak detector value. The frame data is transmitted MSB first with five 5-bit subframes. Each subframe contains a start bit that can be used by a receiver to validate the deserialized data. Figure 145 shows the SPORT over JESD204B signal monitor data with a monitor period timer set to 80 samples.

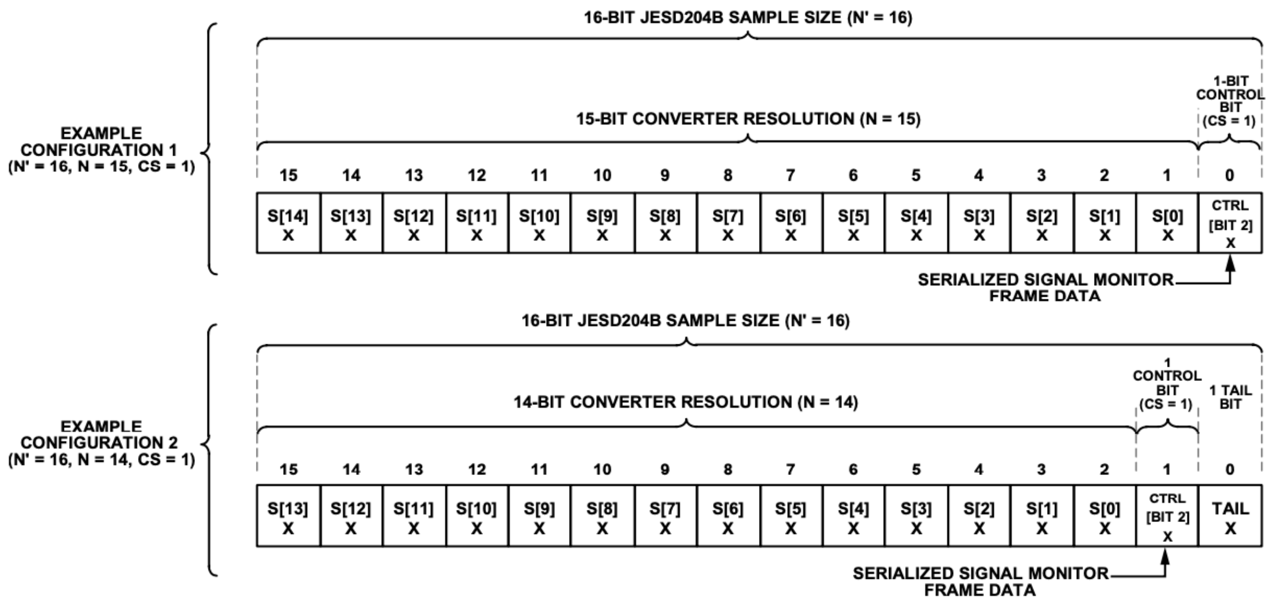


Figure 143. Signal Monitor Control Bit Locations

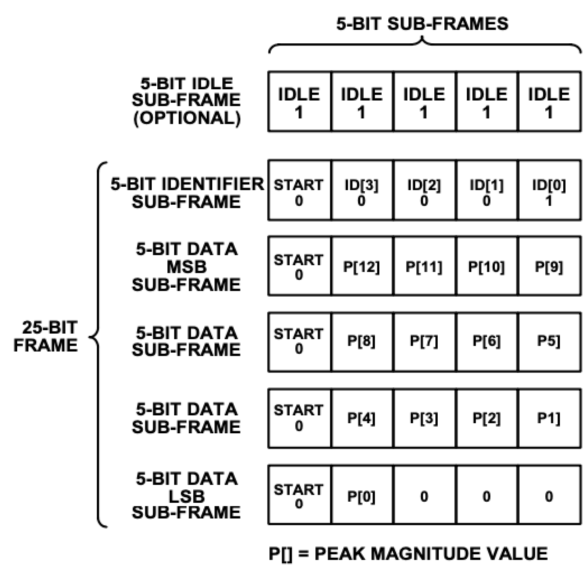


Figure 144. SPORT over JESD204B Signal Monitor Frame Data

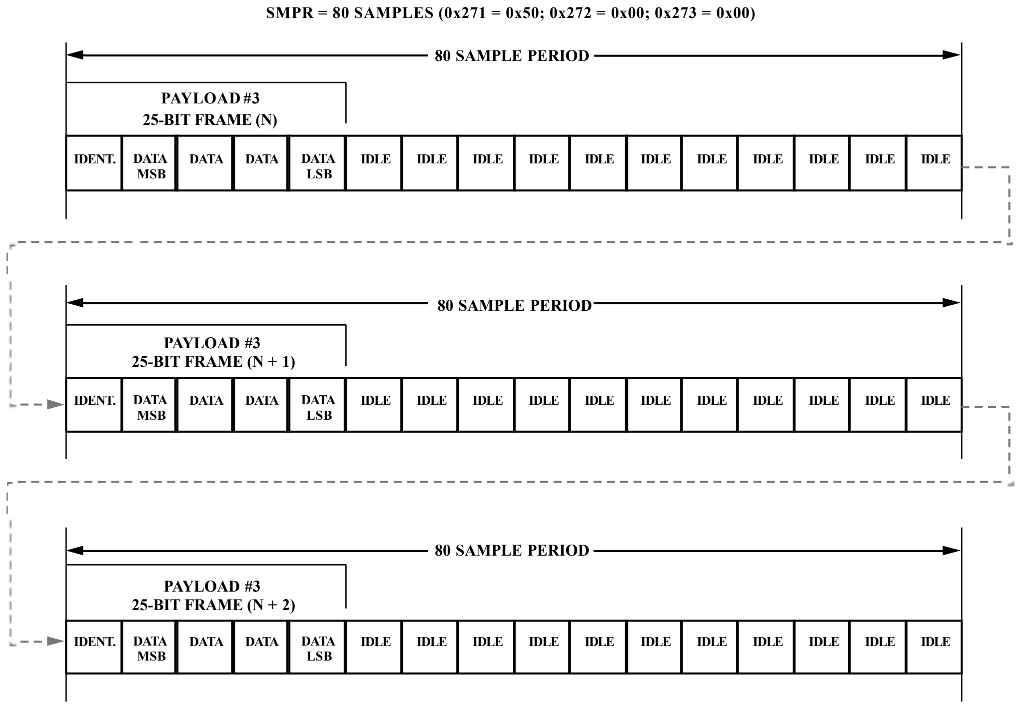


Figure 145. SPORT over JESD204B Signal Monitor Example with Period = 80 Samples

DIGITAL DOWNCONVERTER (DDC)

The CLM9680BCPZ includes four digital downconverters (DDC 0 to DDC 3) that provide filtering and reduce the output data rate. This digital processing section includes an NCO, a half-band decimating filter, an FIR filter, a gain stage, and a complex-real conversion stage. Each of these processing blocks has control lines that allow it to be independently enabled and disabled to provide the desired processing function. The digital downconverter can be configured to output either real data or complex output data.

The DDCs output a 16-bit stream. To enable this operation, the converter number of bits, N, is set to a default value of 16, even though the Chiplon core only outputs 14 bits. In full bandwidth operation, the ADC outputs are the 14-bit word followed by two zeros, unless the tail bits are enabled.

DDC I/Q INPUT SELECTION

The CLM9680BCPZ has two ADC channels and four DDC channels. Each DDC channel has two input ports that can be paired to support both real or complex inputs through the I/Q crossbar mux. For real signals, both DDC input ports must select the same ADC channel (for example, DDC Input Port I = ADC Channel A, and Input Port Q = ADC Channel A). For complex signals, each DDC input port must select different ADC channels (for example, DDC Input Port I = ADC Channel A, and Input Port Q = ADC Channel B).

The inputs to each DDC are controlled by the DDC input selection registers (Register 0x311, Register 0x331, Register 0x351, and Register 0x371). See Table 39 for information on how to configure the DDCs.

DDC I/Q OUTPUT SELECTION

Each DDC channel has two output ports that can be paired to support both real or complex outputs. For real output signals, only the DDC Output Port I is used (the DDC Output Port Q is invalid). For complex I/Q output signals, both DDC Output Port I and DDC Output Port Q are used.

The I/Q outputs to each DDC channel are controlled by the DDC complex to real enable bit (Bit 3) in the DDC control registers (Register 0x310, Register 0x330, Register 0x350, and Register 0x370).

The Chip Q ignore bit (Bit 5) in the chip application mode register (Register 0x200) controls the chip output muxing of all the DDC channels. When all DDC channels use real outputs, this bit must be set high to ignore all DDC Q output ports. When any of the DDC channels are set to use complex I/Q outputs, the user must clear this bit to use both DDC Output Port I and DDC Output Port Q. For more information, see Figure 154.

DDC GENERAL DESCRIPTION

The four DDC blocks are used to extract a portion of the full digital spectrum captured by the ADC(s). They are intended for IF sampling or oversampled baseband radios requiring wide bandwidth input signals.

Each DDC block contains the following signal processing stages.

Frequency Translation Stage (Optional)

The frequency translation stage consists of a 12-bit complex NCO and quadrature mixers that can be used for frequency translation of both real or complex input signals. This stage shifts a portion of the available digital spectrum down to baseband.

Filtering Stage

After shifting down to baseband, the filtering stage decimates the frequency spectrum using a chain of up to four half-band low-pass filters for rate conversion. The decimation process lowers the output data rate, which in turn reduces the output interface rate.

Gain Stage (Optional)

Due to losses associated with mixing a real input signal down to baseband, the gain stage compensates by adding an additional 0 dB or 6 dB of gain.

Complex to Real Conversion Stage (Optional)

When real outputs are necessary, the complex to real conversion stage converts the complex outputs back to real by performing an $f_S/4$ mixing operation plus a filter to remove the complex component of the signal.

Figure 146 shows the detailed block diagram of the DDCs implemented in the CLM9680BCPZ.

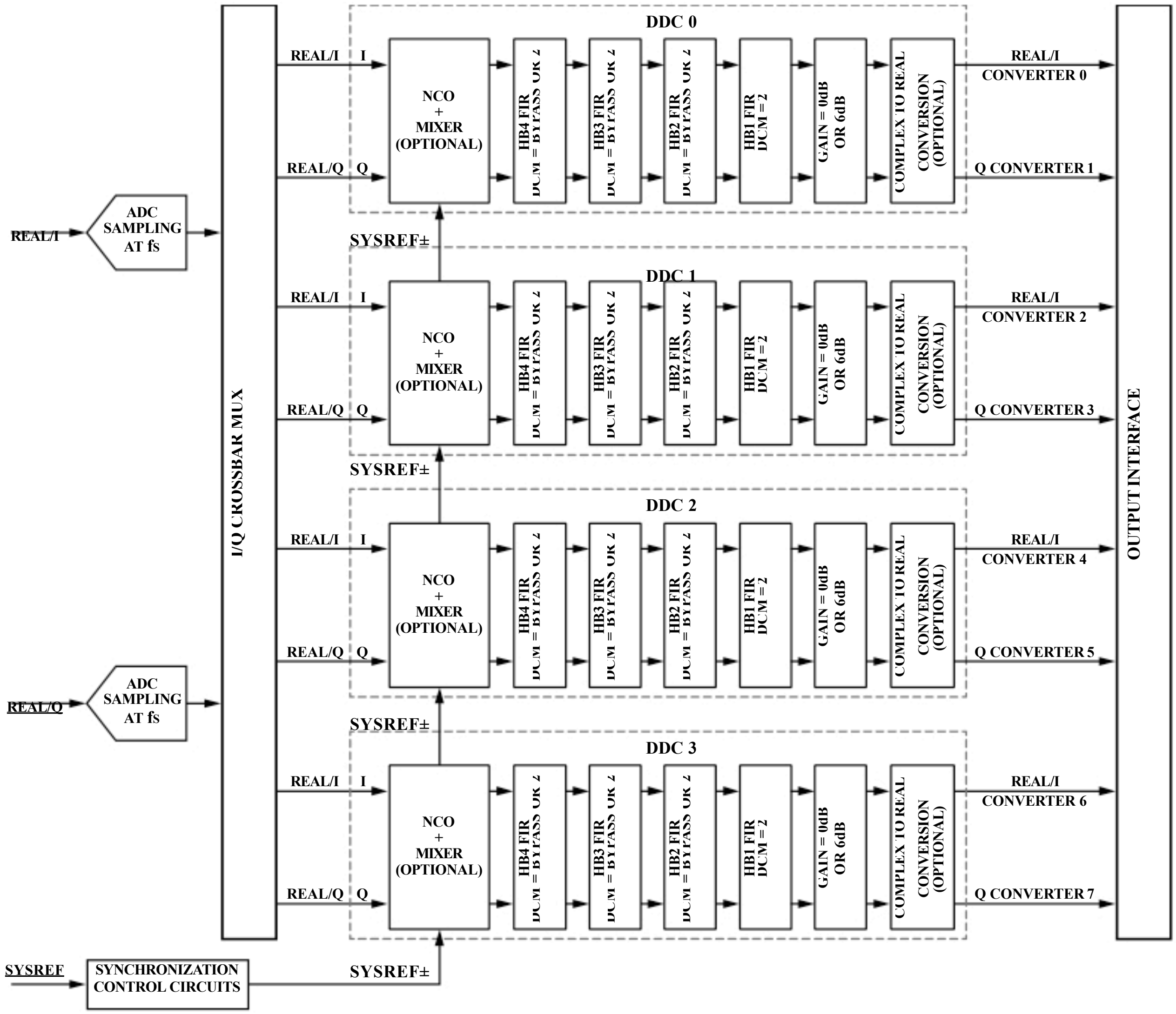


Figure 146. DDC Detailed Block Diagram

Figure 147 shows an example usage of one of the four DDC blocks with a real input signal and four half-band filters (HB4, HB3, HB2, and HB1). It shows both complex (decimate by 16) and real (decimate by 8) output options.

When DDCs have different decimation ratios, the chip decimation ratio (Register 0x201) must be set to the lowest decimation ratio of all the DDC blocks. In this scenario, samples of higher decimation ratio DDCs are repeated to match the chip decimation ratio sample rate. Whenever the NCO frequency is set or changed, the DDC soft reset must be issued. If the DDC soft reset is not issued, the output may potentially show amplitude variations.

Table 11, Table 12, Table 13, Table 14, and Table 15 show the DDC samples when the chip decimation ratio is set to 1, 2, 4, 8, or 16, respectively.

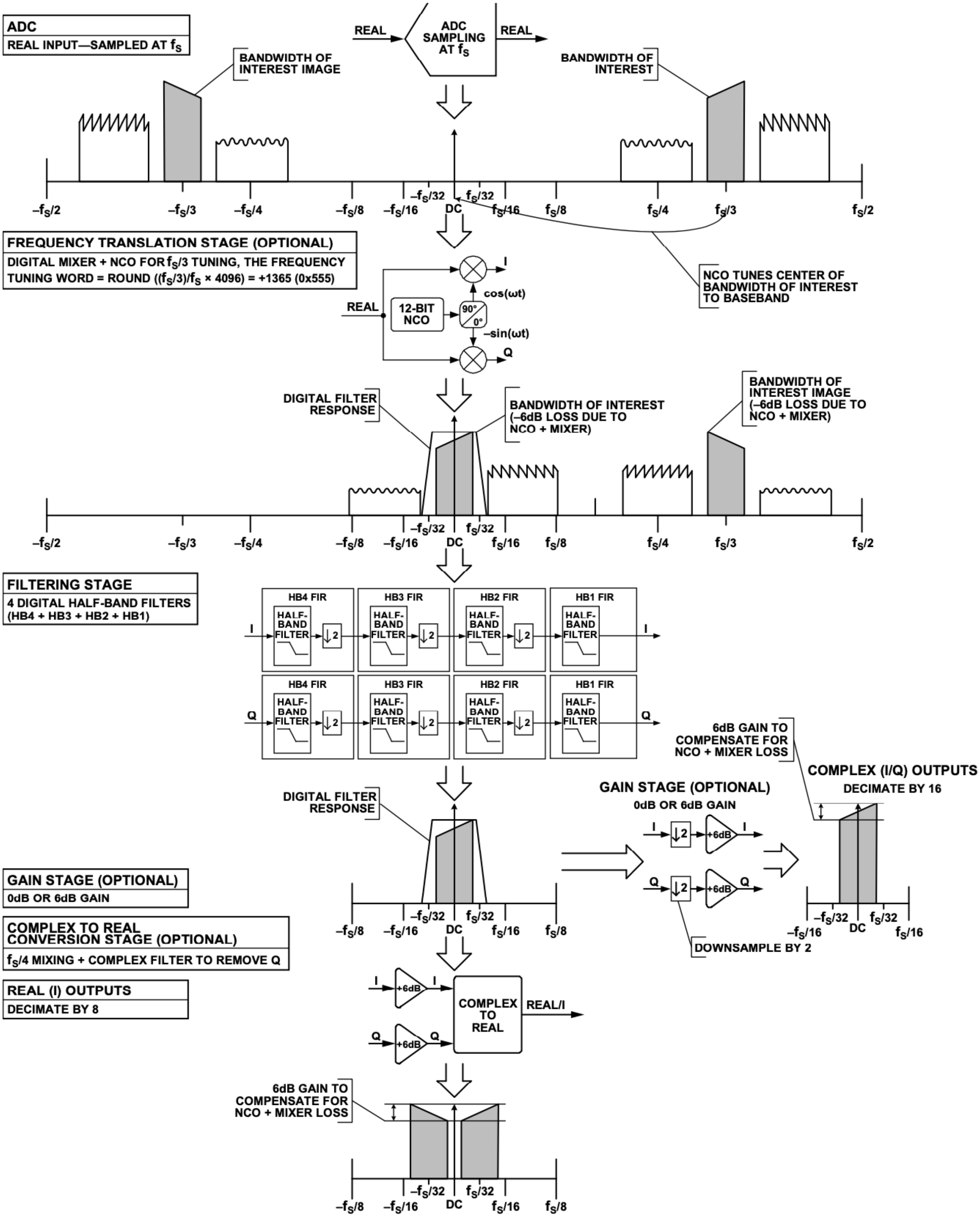


Figure 147. DDC Theory of Operation Example (Real Input—Decimate by 16)

Table 11. DDC Samples, Chip Decimation Ratio = 1

Real (I) Output (Complex to Real Enabled)				Complex (I/Q) Outputs (Complex to Real Disabled)			
HB1 FIR (DCM[1] = 1)	HB2 FIR + HB1 FIR (DCM[1] = 2)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB1 FIR (DCM[1] = 2)	HB2 FIR + HB1 FIR (DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N	N	N	N	N	N	N	N
N + 1	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1
N + 2	N	N	N	N	N	N	N
N + 3	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1
N + 4	N + 2	N	N	N + 2	N	N	N
N + 5	N + 3	N + 1	N + 1	N + 3	N + 1	N + 1	N + 1
N + 6	N + 2	N	N	N + 2	N	N	N
N + 7	N + 3	N + 1	N + 1	N + 3	N + 1	N + 1	N + 1
N + 8	N + 4	N + 2	N	N + 4	N + 2	N	N
N + 9	N + 5	N + 3	N + 1	N + 5	N + 3	N + 1	N + 1
N + 10	N + 4	N + 2	N	N + 4	N + 2	N	N
N + 11	N + 5	N + 3	N + 1	N + 5	N + 3	N + 1	N + 1
N + 12	N + 6	N + 2	N	N + 6	N + 2	N	N
N + 13	N + 7	N + 3	N + 1	N + 7	N + 3	N + 1	N + 1
N + 14	N + 6	N + 2	N	N + 6	N + 2	N	N
N + 15	N + 7	N + 3	N + 1	N + 7	N + 3	N + 1	N + 1
N + 16	N + 8	N + 4	N + 2	N + 8	N + 4	N + 2	N
N + 17	N + 9	N + 5	N + 3	N + 9	N + 5	N + 3	N + 1
N + 18	N + 8	N + 4	N + 2	N + 8	N + 4	N + 2	N
N + 19	N + 9	N + 5	N + 3	N + 9	N + 5	N + 3	N + 1
N + 20	N + 10	N + 4	N + 2	N + 10	N + 4	N + 2	N
N + 21	N + 11	N + 5	N + 3	N + 11	N + 5	N + 3	N + 1
N + 22	N + 10	N + 4	N + 2	N + 10	N + 4	N + 2	N
N + 23	N + 11	N + 5	N + 3	N + 11	N + 5	N + 3	N + 1
N + 24	N + 12	N + 6	N + 2	N + 12	N + 6	N + 2	N
N + 25	N + 13	N + 7	N + 3	N + 13	N + 7	N + 3	N + 1
N + 26	N + 12	N + 6	N + 2	N + 12	N + 6	N + 2	N
N + 27	N + 13	N + 7	N + 3	N + 13	N + 7	N + 3	N + 1
N + 28	N + 14	N + 6	N + 2	N + 14	N + 6	N + 2	N
N + 29	N + 15	N + 7	N + 3	N + 15	N + 7	N + 3	N + 1
N + 30	N + 14	N + 6	N + 2	N + 14	N + 6	N + 2	N
N + 31	N + 15	N + 7	N + 3	N + 15	N + 7	N + 3	N + 1

[1] DCM means decimation.

Table 12. DDC Samples, Chip Decimation Ratio = 2

Real (I) Output (Complex to Real Enabled)			Complex (I/Q) Outputs (Complex to Real Disabled)			
HB2 FIR + HB1 FIR (DCM[1] = 2)	**HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)**	**HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)**	**HB1 FIR (DCM[1] = 2)**	**HB2 FIR + HB1 FIR (DCM[1] = 4)**	**HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)**	**HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)**
N	N	N	N	N	N	N
N + 1 N	N + 1	N + 1	N + 1 N	N + 1	N + 1	N + 1
+ 2 N +	N	N	+ 2 N +	N	N	N
3 N + 4	N + 1	N + 1	3 N + 4	N + 1	N + 1	N + 1
N + 5 N	N + 2	N	N + 5 N	N + 2	N	N
+ 6 N +	N + 3	N + 1	+ 6 N +	N + 3	N + 1	N + 1
7 N + 8	N + 2	N	7 N + 8	N + 2	N	N
N + 9 N	N + 3	N + 1	N + 9 N	N + 3	N + 1	N + 1
+ 10 N	N + 4	N + 2	+ 10 N	N + 4	N + 2	N
+ 11 N	N + 5	N + 3	+ 11 N	N + 5	N + 3	N + 1
+ 12 N	N + 4	N + 2	+ 12 N	N + 4	N + 2	N
+ 13 N	N + 5	N + 3	+ 13 N	N + 5	N + 3	N + 1
+ 14 N	N + 6	N + 2	+ 14 N	N + 6	N + 2	N
+ 15	N + 7	N + 3	+ 15	N + 7	N + 3	N + 1
	N + 6	N + 2		N + 6	N + 2	N
	N + 7	N + 3		N + 7	N + 3	N + 1

[1] DCM means decimation.

Table 13. DDC Samples, Chip Decimation Ratio = 4

Real (I) Output (Complex to Real Enabled)		Complex (I/Q) Outputs (Complex to Real Disabled)		
HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	**HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)**	**HB2 FIR + HB1 FIR (DCM[1] = 4)**	**HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)**	**HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)**
N	N	N	N	N
N + 1	N + 1	N + 1	N + 1	N + 1
N + 2	N	N + 2	N	N
N + 3	N + 1	N + 3	N + 1	N + 1
N + 4	N + 2	N + 4	N + 2	N
N + 5	N + 3	N + 5	N + 3	N + 1
N + 6	N + 2	N + 6	N + 2	N
N + 7	N + 3	N + 7	N + 3	N + 1

[1] DCM means decimation.

Table 14. DDC Samples, Chip Decimation Ratio = 8

Real (I) Output (Complex to Real Enabled)	Complex (I/Q) Outputs (Complex to Real Disabled)	
HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	**HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)**	**HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)**
N	N	N
N + 1	N + 1	N + 1
N + 2	N + 2	N
N + 3	N + 3	N + 1
N + 4	N + 4	N + 2

Real (I) Output (Complex to Real Enabled)	Complex (I/Q) Outputs (Complex to Real Disabled)	
HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N + 5	N + 5	N + 3
N + 6	N + 6	N + 2
N + 7	N + 7	N + 3

[1] DCM means decimation.

Table 15. DDC Samples, Chip Decimation Ratio = 16

Real (I) Output (Complex to Real Enabled)	Complex (I/Q) Outputs (Complex to Real Disabled)
HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
Not applicable	N
Not applicable	N + 1
Not applicable	N + 2
Not applicable	N + 3

[1] DCM means decimation.

If the chip decimation ratio is set to decimate by 4, DDC 0 is set to use HB2 + HB1 filters (complex outputs decimate by 4), and DDC 1 is set to use HB4 + HB3 + HB2 + HB1 filters (real outputs decimate by 8), then DDC 1 repeats its output data two times for every one DDC 0 output. The resulting output samples are shown in Table 16.

Table 16. DDC Output Samples when Chip DCM[1] = 4, DDC 0 DCM[1] = 4 (Complex), and DDC 1 DCM[1] = 8 (Real)

DDC Input Samples	DDC 0		DDC 1	
	Output Port I	Output Port Q	Output Port I	Output Port Q
N N + 1 N + 2 N + 3	I0 [N]	Q0 [N]	I1 [N]	Not applicable
N + 4 N + 5 N + 6 N + 7	I0 [N + 1]	Q0 [N + 1]	I1 [N + 1]	Not applicable
N + 8 N + 9 N + 10 N + 11	I0 [N + 2]	Q0 [N + 2]	I1 [N]	Not applicable
N + 12 N + 13 N + 14 N + 15	I0 [N + 3]	Q0 [N + 3]	I1 [N + 1]	Not applicable

[1] DCM means decimation.

FREQUENCY TRANSLATION

FREQUENCY TRANSLATION GENERAL DESCRIPTION

Frequency translation is accomplished by using a 12-bit complex NCO along with a digital quadrature mixer. The frequency translation translates either a real or complex input signal from an intermediate frequency (IF) to a baseband complex digital output (carrier frequency = 0 Hz).

The frequency translation stage of each DDC can be controlled individually and supports four different IF modes using Bits[5:4] of the DDC control registers (Register 0x310, Register 0x330, Register 0x350, and Register 0x370). These IF modes are

- Variable IF mode
- 0 Hz IF (ZIF) mode
- fs/4 Hz IF mode
- Test mode

Variable IF Mode

NCO and mixers are enabled. NCO output frequency can be used to digitally tune the IF frequency.

0 Hz IF (ZIF) Mode

Mixers are bypassed and the NCO is disabled.

fs/4 Hz IF Mode

Mixers and NCO are enabled in special down mixing by fs/4 mode to save power.

Test Mode

Input samples are forced to 0.999 to positive full scale. NCO is enabled. This test mode allows the NCOs to directly drive the decimation filters.

Figure 148 and Figure 149 show examples of the frequency translation stage for both real and complex inputs.

NCO FREQUENCY TUNING WORD (FTW) SELECTION
12-BIT NCO FTW = MIXING FREQUENCY/ADC SAMPLE RATE × 4096

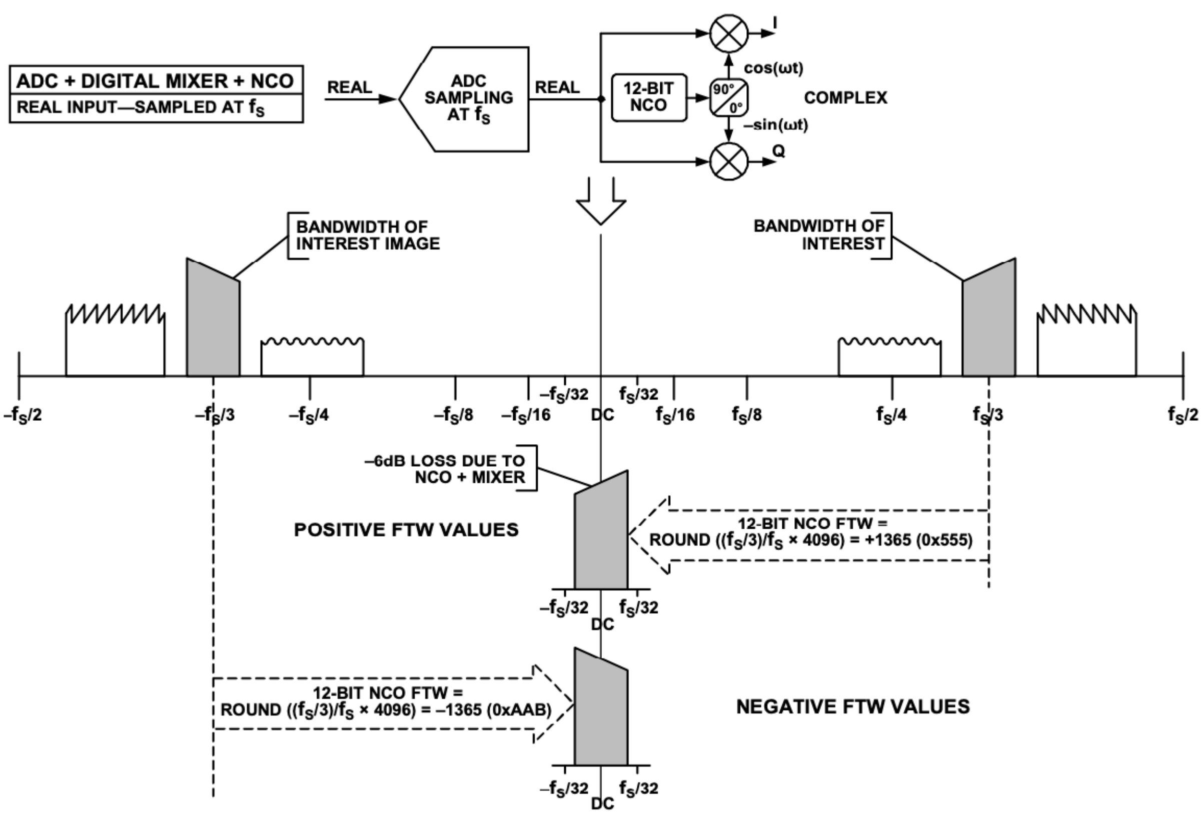


Figure 148. DDC NCO Frequency Tuning Word Selection—Real Inputs

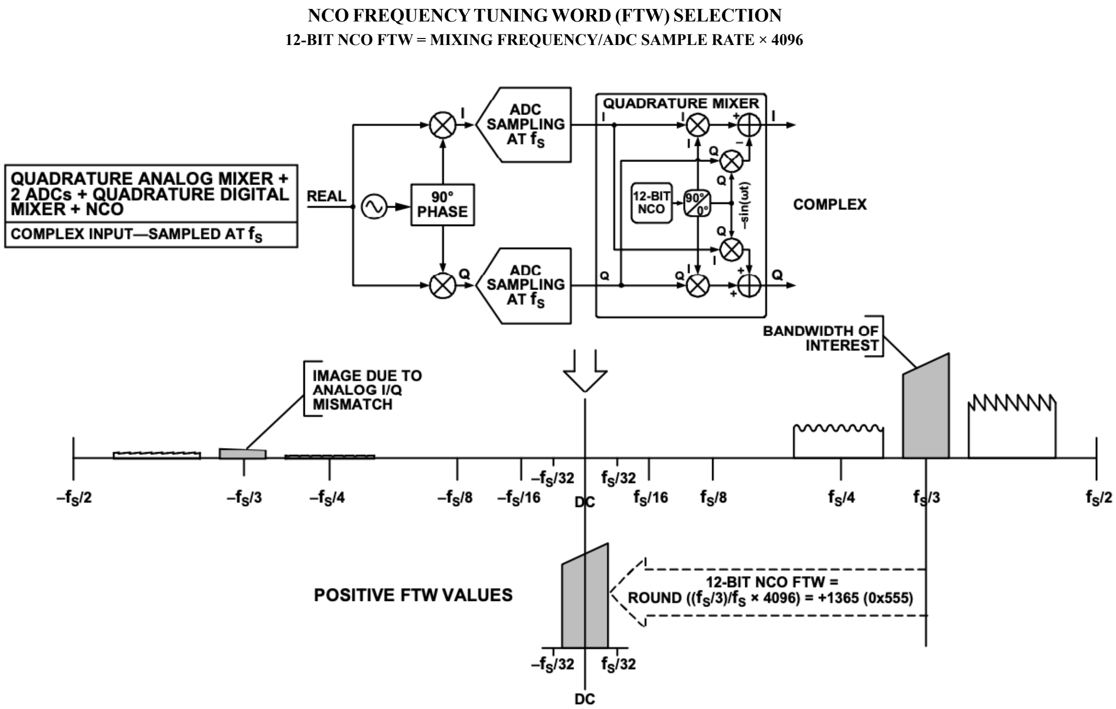


Figure 149. DDC NCO Frequency Tuning Word Selection—Complex Inputs

DDC NCO PLUS MIXER LOSS AND SFDR

When mixing a real input signal down to baseband, 6 dB of loss is introduced in the signal due to filtering of the negative image. An additional 0.05 dB of loss is introduced by the NCO. The total loss of a real input signal mixed down to baseband is 6.05 dB. For this reason, it is recommended that the user compensate for this loss by enabling the additional 6 dB of gain in the gain stage of the DDC to recenter the dynamic range of the signal within the full scale of the output bits.

When mixing a complex input signal down to baseband, the maximum value each I/Q sample can reach is 1.414 × full scale after it passes through the complex mixer. To avoid overrange of the I/Q samples and to keep the data bit widths aligned with real mixing, 3.06 dB of loss (0.707 × full scale) is introduced in the mixer for complex signals. An additional 0.05 dB of loss is introduced by the NCO. The total loss of a complex input signal mixed down to baseband is −3.11 dB.

The worst case spurious signal from the NCO is greater than 102 dBc SFDR for all output frequencies.

NUMERICALLY CONTROLLED OSCILLATOR

The CLM9680BCPZ has a 12-bit NCO for each DDC that enables the frequency translation process. The NCO allows the input spectrum to be tuned to dc, where it can be effectively filtered by the subsequent filter blocks to prevent aliasing. The NCO can be set up by providing a frequency tuning word (FTW) and a phase offset word (POW).

Setting Up the NCO FTW and POW

The NCO frequency value is given by the 12-bit twos complement number entered in the NCO FTW. Frequencies between $-f_S/2$ and $f_S/2$ ($f_S/2$ excluded) are represented using the following frequency words:

- 0x800 represents a frequency of $-f_S/2$.
- 0x000 represents dc (frequency is 0 Hz).
- 0x7FF represents a frequency of $+f_S/2 - f_S/2^{12}$.

The NCO frequency tuning word can be calculated using the following equation:

$$NCO\_FTW = round\left(2^{12}\frac{Mod(f_C, f_S)}{f_S}\right)$$

where:

NCO_FTW is a 12-bit twos complement number representing the NCO FTW.

f_S is the CLM9680BCPZ sampling frequency (clock rate) in Hz.

f_C is the desired carrier frequency in Hz.

Mod( ) is a remainder function. For example, Mod(110,100) = 10, and for negative numbers, Mod(–32, 10) = –2.

round( ) is a rounding function. For example, round(3.6) = 4, and for negative numbers, round(–3.4)= –3.

Note that this equation applies to the aliasing of signals in the digital domain (that is, aliasing introduced when digitizing Chiplon signals).

For example, if the ADC sampling frequency (f_S) is 1250 MSPS and the carrier frequency (f_C) is 416.667 MHz,

$$NCO\_FTW = round\left(2^{12}\frac{Mod(416.667,1250)}{1250}\right) = 1365 \text{ MHz}$$

This, in turn, converts to 0x555 in the 12-bit twos complement representation for NCO_FTW. The actual carrier frequency can be calculated based on the following equation:

$$f_C - actual = \frac{NCO\_FTW \times f_S}{2^{12}} = 416.56 \text{ MHz}$$

A 12-bit POW is available for each NCO to create a known phase relationship between multiple CLM9680BCPZ chips or individual DDC channels inside one CLM9680BCPZ.

The following procedure must be followed to update the FTW and/or POW registers to ensure proper operation of the NCO:

- Write to the FTW registers for all the DDCs.
- Write to the POW registers for all the DDCs.
- Synchronize the NCOs either through the DDC soft reset bit accessible through the SPI, or through the assertion of the SYSREF± pin.

Note that the NCOs must be synchronized either through SPI or through the SYSREF± pin after all writes to the FTW or POW registers have completed. This synchronization is necessary to ensure the proper operation of the NCO.

NCO Synchronization

Each NCO contains a separate phase accumulator word (PAW) that determines the instantaneous phase of the NCO. The initial reset value of each PAW is determined by the POW described in the Setting Up the NCO FTW and POW section. The phase increment value of each PAW is determined by the FTW.

Two methods can be used to synchronize multiple PAWs within the chip:

- Using the SPI. The DDC NCO soft reset bit in the DDC synchronization control register (Register 0x300, Bit 4) can be used to reset all the PAWs in the chip. This is accomplished by toggling the DDC NCO soft reset bit. This method can only be used to synchronize DDC channels within the same CLM9680BCPZ chip.
- Using the SYSREF± pin. When the SYSREF± pin is enabled in the SYSREF± control registers (Register 0x120 and Register 0x121), and the DDC synchronization is enabled in Bits[1:0] in the DDC synchronization control register (Register 0x300), any subsequent SYSREF± event resets all the PAWs in the chip. This method can be used to synchronize DDC channels within the same CLM9680BCPZ chip, or DDC channels within separate CLM9680BCPZ chips.

Mixer

The NCO is accompanied by a mixer, whose operation is similar to an Chiplon quadrature mixer. The mixer performs the downconversion of input signals (real or complex) by using the NCO frequency as a local oscillator. For real input signals, this mixer performs a real mixer operation (with two multipliers). For complex input signals, the mixer performs a complex mixer operation (with four multipliers and two adders). The mixer adjusts its operation based on the input signal (real or complex) provided to each individual channel. The selection of real or complex inputs can be controlled individually for each DDC block by using Bit 7 of the DDC control register (Register 0x310, Register 0x330, Register 0x350, and Register 0x370).

FIR FILTERS

FIR FILTERS GENERAL DESCRIPTION

There are four sets of decimate-by-2, low-pass, half-band, finite impulse response (FIR) filters (HB1 FIR, HB2 FIR, HB3 FIR, and HB4 FIR, shown in Figure 146). These filters follow the frequency translation stage. After the carrier of interest is tuned down to dc (carrier frequency = 0 Hz), these filters efficiently lower the sample rate while providing sufficient alias rejection from unwanted adjacent carriers around the bandwidth of interest.

HB1 FIR is always enabled and cannot be bypassed. The HB2, HB3, and HB4 FIR filters are optional and can be bypassed for higher output sample rates.

Table 17 shows the different bandwidth options by including different half-band filters. In all cases, the DDC filtering stage of the CLM9680BCPZ provides less than −0.001 dB of pass-band ripple and >100 dB of stop-band alias rejection.

Table 18 shows the amount of stop-band alias rejection for multiple pass-band ripple/cutoff points. The decimation ratio of the filtering stage of each DDC can be controlled individually through Bits[1:0] of the DDC control registers (0x310, 0x330, 0x350, and 0x370).

Table 17. DDC Filter Characteristics

ADC Sample Rate (MSPS)	Half Band Filter Selection	Real Output: Decimation Ratio	Real Output: Output Sample Rate (MSPS)	Complex (I/Q) Output: Decimation Ratio	Complex (I/Q) Output: Output Sample Rate (MSPS)	Alias Protected Bandwidth (MHz)	Ideal SNR Improvement (dB)[1]	Pass-Band Ripple (dB)	Alias Rejection (dB)
1250	HB1	1	1250	2	625 (I) + 625 (Q)	481.25	1	<−0.001	>100
	HB1 + HB2	2	625	4	312.5 (I) + 312.5 (Q)	240.62	4		
	HB1 + HB2 + HB3	4	312.5	8	156.25 (I) + 156.25 (Q)	120.31	7		
	HB1 + HB2 + HB3 + HB4	8	156.25	16	78.125 (I) + 78.125 (Q)	60.15	10		
1000	HB1	1 2 4	1000	2 4 8	500 (I) + 500 (Q)	385.0	1 4 7		
	HB1 + HB2	8	500	16	250 (I) + 250 (Q)	192.5	10		
	HB1 + HB2 + HB3		250		125 (I) + 125 (Q)	96.3			
	HB1 + HB2 + HB3 + HB4		125		62.5 (I) + 62.5 (Q)	48.1			
820	HB1	1 2 4	820	2 4 8	410 (I) + 410 (Q)	315.7	1 4 7		
	HB1 + HB2	8	410	16	205 (I) + 205 (Q)	157.8	10		
	HB1 + HB2 + HB3		205		102.5 (I) + 102.5 (Q)	78.9			
	HB1 + HB2 + HB3 + HB4		102.5		51.25 (I) + 51.25 (Q)	39.4			
500	HB1	1 2 4	500	2 4 8	250 (I) + 250 (Q)	192.5	1 4 7		
	HB1 + HB2	8	250	16	125 (I) + 125 (Q)	96.3	10		
	HB1 + HB2 + HB3		125		62.5 (I) + 62.5 (Q)	48.1			
	HB1 + HB2 + HB3 + HB4		62.5		31.25 (I) + 31.25 (Q)	24.1			

[1] Ideal SNR improvement due to oversampling and filtering = 10log(bandwidth/(f_S/2)).

Table 18. DDC Filter Alias Rejection

Alias Rejection (dB)	Pass-Band Ripple/ Cutoff Point (dB)	Alias Protected Bandwidth for Real (I) Outputs[1]	Alias Protected Bandwidth for Complex (I/Q) Outputs[1]
>100	<−0.001	<38.5% × f_{OUT}	<77% × f_{OUT}
90	<−0.001	<38.7% × f_{OUT}	<77.4% × f_{OUT}
85	<−0.001	<38.9% × f_{OUT}	<77.8% × f_{OUT}
63.3	<−0.006	<40% × f_{OUT}	<80% × f_{OUT}
25	−0.5	44.4% × f_{OUT}	88.8% × f_{OUT}
19.3	−1.0	45.6% × f_{OUT}	91.2% × f_{OUT}
10.7	−3.0	48% × f_{OUT}	96% × f_{OUT}

[1] f_{OUT} is the ADC input sample rate f_S/DDC decimation ratio.

HALF-BAND FILTERS

The CLM9680BCPZ offers four half-band filters to enable digital signal processing of the ADC converted data. These half-band filters can be bypassed and can be individually selected.

HB4 Filter

The first decimate-by-2, half-band, low-pass FIR filter (HB4) uses an 11-tap, symmetrical, fixed-coefficient filter implementation, optimized for low power consumption. The HB4 filter is only used when complex outputs (decimate by 16) or real outputs (decimate by 8) are enabled; otherwise, the filter is bypassed. Table 19 and Figure 150 show the coefficients and response of the HB4 filter.

Table 19. HB4 Filter Coefficients

HB4 Coefficient Number	Normalized Coefficient	Decimal Coefficient (15-Bit)
C1, C11	0.006042	99
C2, C10	0	0
C3, C9	−0.049316	−808
C4, C8	0	0
C5, C7	0.293273	4805
C6	0.500000	8192

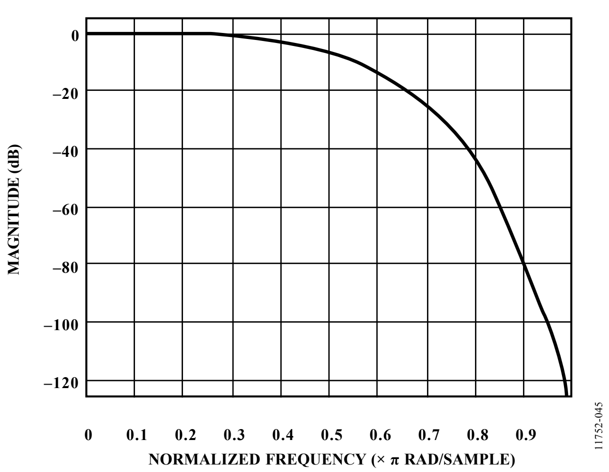


Figure 150. HB4 Filter Response

HB3 Filter

The second decimate-by-2, half-band, low-pass, FIR filter (HB3) uses an 11-tap, symmetrical, fixed coefficient filter implementation, optimized for low power consumption. The HB3 filter is only used when complex outputs (decimate by 8 or 16) or real outputs (decimate by 4 or 8) are enabled; otherwise, the filter is bypassed. Table 20 and Figure 151 show the coefficients and response of the HB3 filter.

Table 20. HB3 Filter Coefficients

HB3 Coefficient Number	Normalized Coefficient	Decimal Coefficient (18-Bit)
C1, C11	0.006554	859
C2, C10	0	0
C3, C9	−0.050819	−6661
C4, C8	0	0
C5, C7	0.294266	38,570
C6	0.500000	65,536

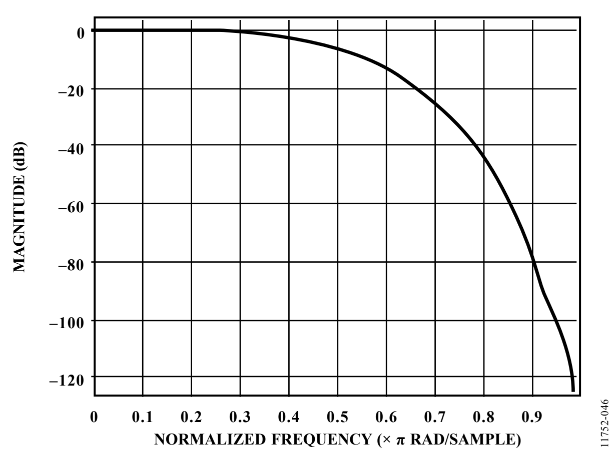


Figure 151. HB3 Filter Response

HB2 Filter

The third decimate-by-2, half-band, low-pass FIR filter (HB2) uses a 19-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB2 filter is only used when complex outputs (decimate by 4, 8, or 16) or real outputs (decimate by 2, 4, or 8) are enabled; otherwise, the filter is bypassed.

Table 21 and Figure 152 show the coefficients and response of the HB2 filter.

Table 21. HB2 Filter Coefficients

HB2 Coefficient Number	Normalized Coefficient	Decimal Coefficient (19-Bit)
C1, C19	0.000614 0	161
C2, C18	−0.005066	0
C3, C17	0 0.022179	−1328
C4, C16	0	0
C5, C15	−0.073517	5814
C6, C14	0 0.305786	0
C7, C13	0.500000	−19,272
C8, C12		0 80,160
C9, C11		131,072
C10		

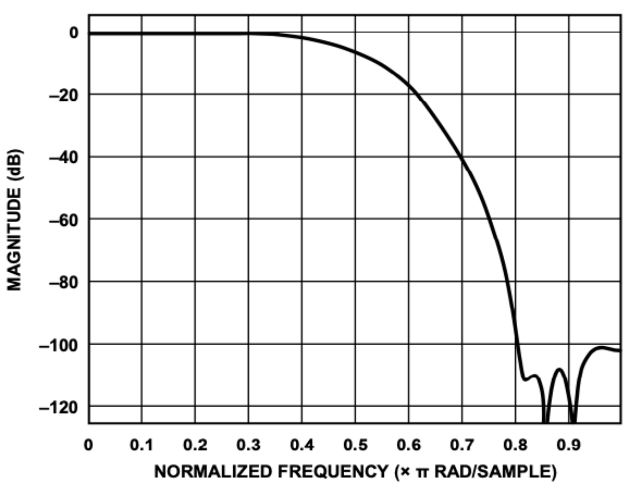


Figure 152. HB2 Filter Response

HB1 Filter

The fourth and final decimate-by-2, half-band, low-pass FIR filter (HB1) uses a 55-tap, symmetrical, fixed coefficient filter implementation, optimized for low power consumption. The HB1 filter is always enabled and cannot be bypassed. Table 22 and Figure 153 show the coefficients and response of the HB1 filter.

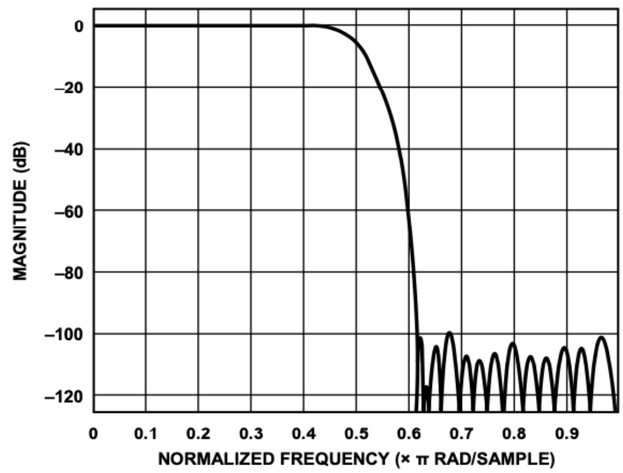


Figure 153. HB1 Filter Response

Table 22. HB1 Filter Coefficients

HB1 Coefficient Number	Normalized Coefficient	Decimal Coefficient (21-Bit)
C1, C55	−0.000023	−24
C2, C54	0	0
C3, C53	0.000097	102
C4, C52	0	0
C5, C51	−0.000288	−302
C6, C50	0	0
C7, C49	0.000696	730
C8, C48	0	0
C9, C47	−0.0014725	−1544
C10, C46	0	0
C11, C45	0.002827	2964
C12, C44	0	0
C13, C43	−0.005039	−5284
C14, C42	0	0
C15, C41	0.008491	8903
C16, C40	0	0
C17, C39	−0.013717	−14,383
C18, C38	0	0
C19, C37	0.021591	22,640
C20, C36	0	0
C21, C35	−0.033833	−35,476
C22, C34	0	0
C23, C33	0.054806	57,468
C24, C32	0	0
C25, C31	−0.100557	−105,442
C26, C30	0	0
C27, C29	0.316421	331,792
C28	0.500000	524,288

DDC GAIN STAGE

Each DDC contains an independently controlled gain stage. The gain is selectable as either 0 dB or 6 dB. When mixing a real input signal down to baseband, it is recommended that the user enable the 6 dB of gain to recenter the dynamic range of the signal within the full scale of the output bits.

When mixing a complex input signal down to baseband, the mixer has already recentered the dynamic range of the signal within the full scale of the output bits and no additional gain is necessary. However, the optional 6 dB gain can be used to compensate for low signal strengths. The downsample by 2 portion of the HB1 FIR filter is bypassed when using the complex to real conversion stage (see Figure 154).

DDC COMPLEX TO REAL CONVERSION

Each DDC contains an independently controlled complex to real conversion block. The complex to real conversion block reuses the last filter (HB1 FIR) in the filtering stage, along with an $f_S/4$ complex mixer to upconvert the signal.

After up converting the signal, the Q portion of the complex mixer is no longer needed and is dropped.

Figure 154 shows a simplified block diagram of the complex to real conversion.

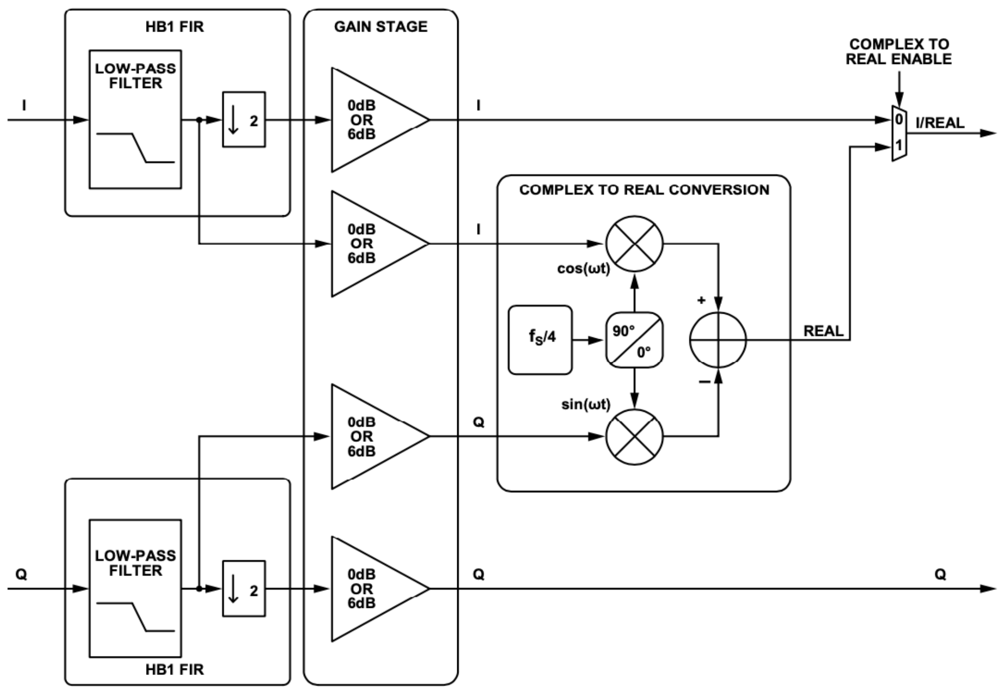


Figure 154. Complex to Real Conversion Block

DDC EXAMPLE CONFIGURATIONS

Table 23 describes the register settings for multiple DDC example configurations.

Table 23. DDC Example Configurations

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth per DDC[1]	No. of Virtual Converters Required	Register Settings[2]
One DDC	2	Complex	Complex	38.5% × fs	2	Register 0x200 = 0x01 (one DDC; I/Q selected) Register 0x201 = 0x01 (chip decimate by 2) Register 0x310 = 0x83 (complex mixer; 0 dB gain; variable IF; complex outputs; HB1 filter) Register 0x311 = 0x04 (DDC I input = ADC Channel A; DDC Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0
Two DDCs	4	Complex	Complex	19.25% × fs	4	Register 0x200 = 0x02 (two DDCs; I/Q selected) Register 0x201 = 0x02 (chip decimate by 4) Register 0x310, Register 0x330 = 0x80 (complex mixer; 0 dB gain; variable IF; complex outputs; HB2 + HB1 filters) Register 0x311, Register 0x331 = 0x04 (DDC I input = ADC Channel A; DDC Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1
Two DDCs	4	Complex	Real	9.63% × fs	2	Register 0x200 = 0x22 (two DDCs; I only selected) Register 0x201 = 0x02 (chip decimate by 4) Register 0x310, Register 0x330 = 0x89 (complex mixer; 0 dB gain; variable IF; real output; HB3 + HB2 + HB1 filters) Register 0x311, Register 0x331 = 0x04 (DDC I Input = ADC Channel A; DDC Q Input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1
Two DDCs	4	Real	Real	9.63% × fs	2	Register 0x200 = 0x22 (two DDCs; I only selected) Register 0x201 = 0x02 (chip decimate by 4) Register 0x310, Register 0x330 = 0x49 (real mixer; 6 dB gain; variable IF; real output; HB3 + HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A; DDC 0 Q input = ADC Channel A) Register 0x331 = 0x05 (DDC 1 I input = ADC Channel B; DDC 1 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth per DDC[1]	No. of Virtual Converters Required	Register Settings[2]
Two DDCs	4	Real	Complex	19.25% × fs	4	Register 0x200 = 0x02 (two DDCs; I/Q selected) Register 0x201 = 0x02 (chip decimate by 4) Register 0x310, Register 0x330 = 0x40 (real mixer; 6 dB gain; variable IF; complex output; HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A; DDC 0 Q input = ADC Channel A) Register 0x331 = 0x05 (DDC 1 I input = ADC Channel B; DDC 1 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1
Two DDCs	8	Real	Real	4.81% × fs	2	Register 0x200 = 0x22 (two DDCs; I only selected) Register 0x201 = 0x03 (chip decimate by 8) Register 0x310, Register 0x330 = 0x4A (real mixer; 6 dB gain; variable IF; real output; HB4 + HB3 + HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A; DDC 0 Q input = ADC Channel A) Register 0x331 = 0x05 (DDC 1 I input = ADC Channel B; DDC 1 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1
Four DDCs	8	Real	Complex	9.63% × fs	8	Register 0x200 = 0x03 (four DDCs; I/Q selected) Register 0x201 = 0x03 (chip decimate by 8) Register 0x310, Register 0x330, Register 0x350, Register 0x370 = 0x41 (real mixer; 6 dB gain; variable IF; complex output; HB3+HB2+HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A; DDC 0 Q input = ADC Channel A) Register 0x331 = 0x00 (DDC 1 I input = ADC Channel A; DDC 1 Q input = ADC Channel A) Register 0x351 = 0x05 (DDC 2 I input = ADC Channel B; DDC 2 Q input = ADC Channel B) Register 0x371 = 0x05 (DDC 3 I input = ADC Channel B; DDC 3 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1 Register 0x354, Register 0x355, Register 0x360, Register 0x361 = FTW and POW set as required by application for DDC 2 Register 0x374, Register 0x375, Register 0x380, Register 0x381 = FTW and POW set as required by application for DDC 3

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth per DDC[1]	No. of Virtual Converters Required	Register Settings[2]
Four DDCs	8	Real	Real	4.81% × fs	4	Register 0x200 = 0x23 (four DDCs; I only selected) Register 0x201 = 0x03 (chip decimate by 8) Register 0x310, Register 0x330, Register 0x350, Register 0x370 = 0x4A (real mixer; 6 dB gain; variable IF; real output; HB4 + HB3 + HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A; DDC 0 Q input = ADC Channel A) Register 0x331 = 0x00 (DDC 1 I input = ADC Channel A; DDC 1 Q input = ADC Channel A) Register 0x351 = 0x05 (DDC 2 I input = ADC Channel B; DDC 2 Q input = ADC Channel B) Register 0x371 = 0x05 (DDC 3 I input = ADC Channel B; DDC 3 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1 Register 0x354, Register 0x355, Register 0x360, Register 0x361 = FTW and POW set as required by application for DDC 2 Register 0x374, Register 0x375, Register 0x380, Register 0x381 = FTW and POW set as required by application for DDC 3
Four DDCs	16	Real	Complex	4.81% × fs	8	Register 0x200 = 0x03 (four DDCs; I/Q selected) Register 0x201 = 0x04 (chip decimate by 16) Register 0x310, Register 0x330, Register 0x350, Register 0x370 = 0x42 (real mixer; 6 dB gain; variable IF; complex output; HB4 + HB3 + HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A; DDC 0 Q input = ADC Channel A) Register 0x331 = 0x00 (DDC 1 I input = ADC Channel A; DDC 1 Q input = ADC Channel A) Register 0x351 = 0x05 (DDC 2 I input = ADC Channel B; DDC 2 Q input = ADC Channel B) Register 0x371 = 0x05 (DDC 3 I input = ADC Channel B; DDC 3 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1 Register 0x354, Register 0x355, Register 0x360, Register 0x361 = FTW and POW set as required by application for DDC 2 Register 0x374, Register 0x375, Register 0x380, Register 0x381 = FTW and POW set as required by application for DDC 3

[1] f_S is the ADC sample rate. Bandwidths listed are <−0.001 dB of pass-band ripple and >100 dB of stop-band alias rejection.
[2] The NCOs must be synchronized either through the SPI or through the SYSREF± pin after all writes to the FTW or POW registers have completed, to ensure the proper operation of the NCO. See the NCO Synchronization section for more information.

DIGITAL OUTPUTS

INTRODUCTION TO THE JESD204B INTERFACE

The CLM9680BCPZ digital outputs are designed to the JEDEC standard JESD204B, serial interface for data converters. JESD204B is a
protocol to link the CLM9680BCPZ to a digital processing device over a serial interface with lane rates of up to 12.5 Gbps. The benefits of the JESD204B interface over LVDS include a reduction in required board area for data interface routing, and an ability to enable smaller packages for converter and logic devices.

JESD204B OVERVIEW

The JESD204B data transmit block assembles the parallel data from the ADC into frames and uses 8-bit/10-bit encoding as well as optional scrambling to form serial output data. Lane synchronization is supported through the use of special control characters during the initial establishment of the link. Additional control characters are embedded in the data stream to maintain synchronization thereafter. A JESD204B receiver is required to complete the serial link. For additional details on the JESD204B interface, refer to the JESD204B standard.

The CLM9680BCPZ JESD204B data transmit block maps up to two physical ADCs or up to eight virtual converters (when DDCs are enabled) over a link. A link can be configured to use one, two, or four JESD204B lanes. The JESD204B specification refers to a number of parameters to define the link, and these parameters must match between the JESD204B transmitter (the CLM9680BCPZ output) and the JESD204B receiver (the logic device input).

The JESD204B link is described according to the following parameters:

- L is the number of lanes/converter device (lanes/link) (CLM9680BCPZ value = 1, 2, or 4)
- M is the number of converters/converter device (virtual converters/link) (CLM9680BCPZ value = 1, 2, 4, or 8)
- F is the octets/frame (CLM9680BCPZ value = 1, 2, 4, 8, or 16)
- N´ is the number of bits per sample (JESD204B word size) (CLM9680BCPZ value = 8 or 16)
- N is the converter resolution (CLM9680BCPZ value = 7 to 16)
- CS is the number of control bits/sample (CLM9680BCPZ value = 0, 1, 2, or 3)
- K is the number of frames per multiframe (CLM9680BCPZ value = 4, 8, 12, 16, 20, 24, 28, or 32)
- S is the samples transmitted/single converter/frame cycle (CLM9680BCPZ value = set automatically based on L, M, F, and N´)
- HD is the high density mode (CLM9680BCPZ = set automatically based on L, M, F, and N´)
- CF is the number of control words/frame clock cycle/ converter device (CLM9680BCPZ value = 0)

Figure 155 shows a simplified block diagram of the CLM9680BCPZ JESD204B link. By default, the CLM9680BCPZ is configured to use two converters and four lanes. Converter A data is output to SERDOUT0± and/or SERDOUT1±, and Converter B is output to SERDOUT2± and/or SERDOUT3±. The CLM9680BCPZ allows other configurations such as combining the outputs of both converters onto a single lane, or changing the mapping of the
A and B digital output paths. These modes are set up via a quick configuration register in the SPI register map, along with additional customizable options.

By default in the CLM9680BCPZ, the 14-bit converter word from each converter is broken into two octets (eight bits of data). Bit 13 (MSB) through Bit 6 are in the first octet. The second octet contains Bit 5 through Bit 0 (LSB) and two tail bits. The tail bits can be configured as zeros or a pseudorandom number sequence. The tail bits can also be replaced with control bits indicating overrange, SYSREF±, or fast detect output.

The two resulting octets can be scrambled. Scrambling is optional; however, it is recommended to avoid spectral peaks when transmitting similar digital data patterns. The scrambler uses a self-synchronizing, polynomial-based algorithm defined by the equation $1 + x_{14} + x_{15}$. The descrambler in the receiver is a self-synchronizing version of the scrambler polynomial.

The two octets are then encoded with an 8-bit/10-bit encoder. The 8-bit/10-bit encoder works by taking eight bits of data (an octet) and encoding them into a 10-bit symbol. Figure 156 shows how the 14-bit data is taken from the ADC, how the tail bits are added, how the two octets are scrambled, and how the octets are encoded into two 10-bit symbols. Figure 156 illustrates the default data format.

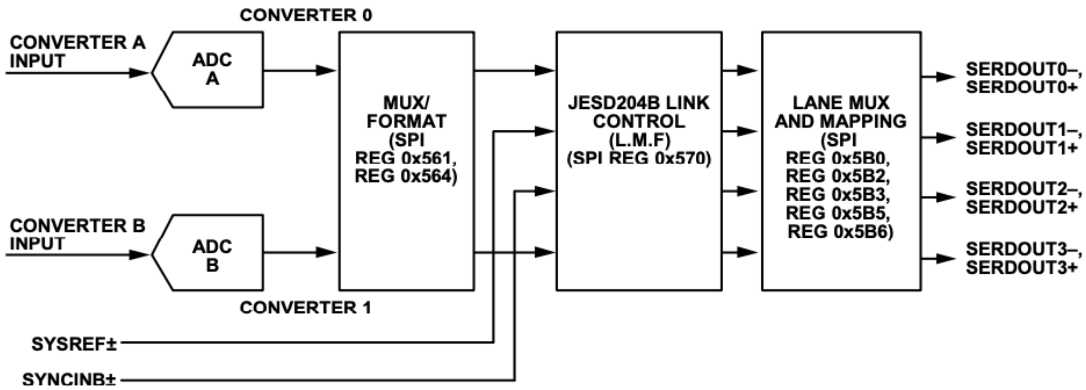


Figure 155. Transmit Link Simplified Block Diagram Showing Full Bandwidth Mode (Register 0x200 = 0x00)

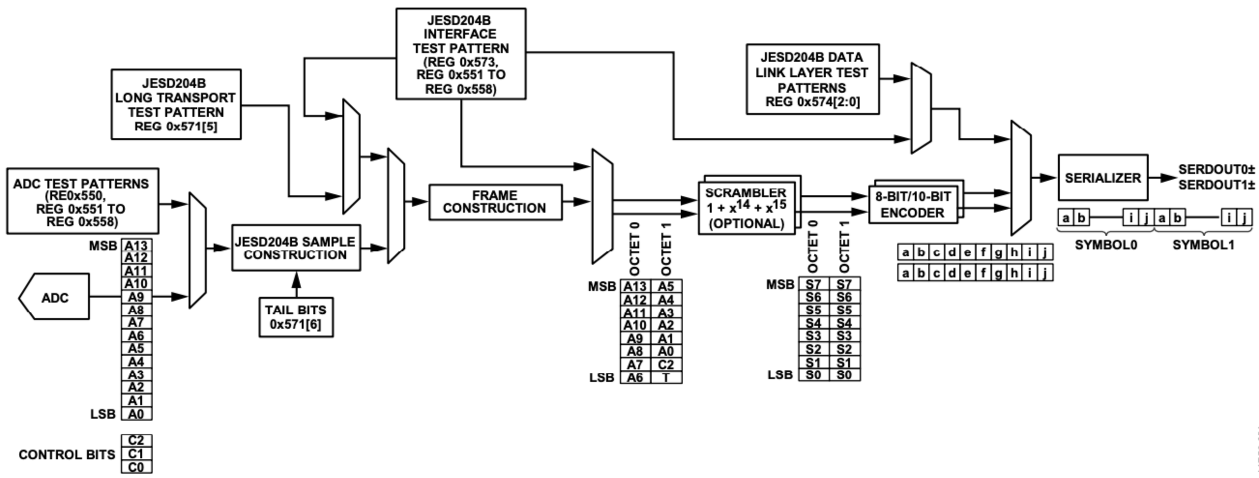


Figure 156. ADC Output Data Path Showing Data Framing

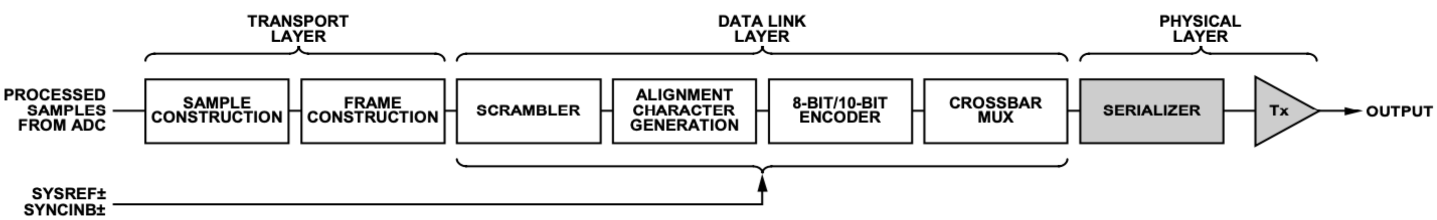


Figure 157. Data Flow

FUNCTIONAL OVERVIEW

The block diagram in Figure 157 shows the flow of data through the JESD204B hardware from the sample input to the physical output. The processing can be divided into layers that are derived from the open source initiative (OSI) model widely used to describe the abstraction layers of communications systems. These layers are the transport layer, data link layer,

and physical layer (serializer and output driver).

Transport Layer

The transport layer handles packing the data (consisting of samples and optional control bits) into JESD204B frames that are mapped to 8-bit octets. These octets are sent to the data link layer. The transport layer mapping is controlled by rules derived from the link parameters. Tail bits are added to fill gaps where required. The following equation can be used to determine the number of tail bits within a sample (JESD204B word):

$$T = N' - N - CS$$

Data Link Layer

The data link layer is responsible for the low level functions of passing data across the link. These include optionally scrambling the data, inserting control characters for multichip synchronization/lane alignment/monitoring, and encoding 8-bit octets into 10-bit symbols. The data link layer is also responsible for sending the initial lane alignment sequence (ILAS), which contains the link configuration data used by the receiver to verify the settings in the transport layer.

Physical Layer

The physical layer consists of the high speed circuitry clocked at the serial clock rate. In this layer, parallel data is converted into one, two, or four lanes of high speed differential serial data.

JESD204B LINK ESTABLISHMENT

The CLM9680BCPZ JESD204B transmitter (Tx) interface operates in Subclass 1 as defined in the JEDEC Standard 204B (July 2011 specification). The link establishment process is divided into the following steps: code group synchronization and SYNCINB±, initial lane alignment sequence, and user data and error correction.

Code Group Synchronization (CGS) and SYNCINB±

The CGS is the process by which the JESD204B receiver finds the boundaries between the 10-bit symbols in the stream of data. During the CGS phase, the JESD204B transmit block transmits /K28.5/ characters. The receiver must locate /K28.5/ characters in its input data stream using clock and data recovery (CDR) techniques.

The receiver issues a synchronization request by asserting the SYNCINB± pin of the CLM9680BCPZ low. The JESD204B Tx then begins sending /K/ characters. Once the receiver has synchronized, it waits for the correct reception of at least four consecutive /K/ symbols. It then deasserts SYNCINB±. The CLM9680BCPZ then transmits an ILAS on the following local multiframe clock (LMFC) boundary. For more information on the code group synchronization phase, refer to the JEDEC Standard JESD204B, July 2011, Section 5.3.3.1.

The SYNCINB± pin operation can also be controlled by the SPI. The SYNCINB± signal is a differential dc-coupled LVDS mode signal by default, but it can also be driven single-ended. For more information on configuring the SYNCINB± pin operation, refer to Register 0x572.

The SYNCINB± pins can also be configured to run in CMOS (single-ended) mode, by setting Bit[4] in Register 0x572. When running SYNCINB± in CMOS mode, connect the CMOS SYNCINB signal to Pin 21 (SYNCINB+) and leave Pin 20 (SYNCINB−) floating.

Initial Lane Alignment Sequence (ILAS)

The ILAS phase follows the CGS phase and begins on the next LMFC boundary. The ILAS consists of four multiframes, with an /R/ character marking the beginning and an /A/ character marking the end. The ILAS begins by sending an /R/ character followed by 0 to 255 ramp data for one multiframe. On the second multiframe, the link configuration data is sent, starting with the third character. The second character is a /Q/ character to confirm that the link configuration data follows. All undefined data slots are filled with ramp data. The ILAS sequence is never scrambled.

The ILAS sequence construction is shown in Figure 158. The four multiframes include the following:

- Multiframe 1. Begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 2. Begins with an /R/ character followed by a /Q/ character (/K28.4/), followed by link configuration parameters over 14 configuration octets (see Table 24) and ends with an /A/ character. Many of the parameter values are of the value – 1 notation.
- Multiframe 3. Begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 4. Begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).

User Data and Error Detection

After the initial lane alignment sequence is complete, the user data is sent. Normally, within a frame, all characters are considered user data. However, to monitor the frame clock and multiframe clock synchronization, there is a mechanism for replacing characters with /F/ or /A/ alignment characters when the data meets certain conditions. These conditions are different for unscrambled and scrambled data. The scrambling operation is enabled by default, but it can be disabled using the SPI.

For scrambled data, any 0xFC character at the end of a frame is replaced by an /F/, and any 0x7C character at the end of a multiframe is replaced with an /A/. The JESD204B receiver (Rx) checks for /F/ and /A/ characters in the received data stream and verifies that they only occur in the expected locations. If an unexpected /F/ or /A/ character is found, the receiver handles the situation by using dynamic realignment or asserting the SYNCINB± signal for more than four frames to initiate a resynchronization. For unscrambled data, if the final character of two subsequent frames is equal, the second character is replaced with an /F/ if it is at the end of a frame, and an /A/ if it is at the end of a multiframe.

Insertion of alignment characters can be modified using SPI. The frame alignment character insertion (FACI) is enabled by default. More information on the link controls is available in the Memory Map section, Register 0x571.

8-Bit/10-Bit Encoder

The 8-bit/10-bit encoder converts 8-bit octets into 10-bit symbols and inserts control characters into the stream when needed.

The control characters used in JESD204B are shown in Table 24. The 8-bit/10-bit encoding ensures that the signal is dc balanced by using the same number of ones and zeros across multiple symbols.

The 8-bit/10-bit interface has options that can be controlled via the SPI. These operations include bypass and invert. These options are troubleshooting tools for the verification of the digital front end (DFE). See the Memory Map section, Register 0x572[2:1] for information on configuring the 8-bit/10-bit encoder.

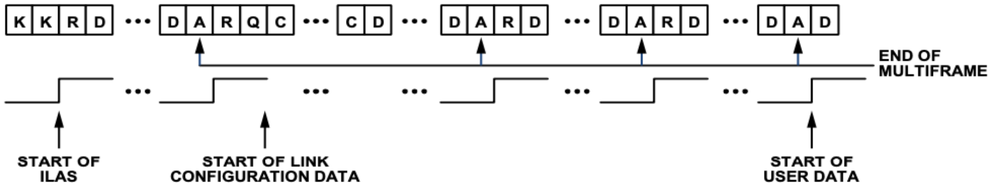


Figure 158. Initial Lane Alignment Sequence

Table 24. CLM9680BCPZ Control Characters used in JESD204B

Abbreviation	Control Symbol	8-Bit Value	10-Bit Value, RD[1] = −1	10-Bit Value, RD[1] = +1	Description
/R/	/K28.0/	000 11100	001111 0100	110000 1011	Start of multiframe
/A/	/K28.3/	011 11100	001111 0011	110000 1100	Lane alignment
/Q/	/K28.4/	100 11100	001111 0100	110000 1101	Start of link configuration data
/K/	/K28.5/	101 11100	001111 1010	110000 0101	Group synchronization
/F/	/K28.7/	111 11100	001111 1000	110000 0111	Frame alignment

[1] RD means running disparity.

PHYSICAL LAYER (DRIVER) OUTPUTS

Digital Outputs, Timing, and Controls

The CLM9680BCPZ physical layer consists of drivers that are defined in the JEDEC Standard JESD204B, July 2011. The differential digital outputs are powered up by default. The drivers use a dynamic 100 Ω internal termination to reduce unwanted reflections.

Place a 100 Ω differential termination resistor at each receiver input to result in a nominal 300 mV p-p swing at the receiver (see Figure 159). Alternatively, single-ended 50 Ω termination can be used. When single-ended termination is used, the termination voltage is DRVDD/2. Otherwise, 0.1 µF ac coupling capacitors can be used to terminate to any single-ended voltage.

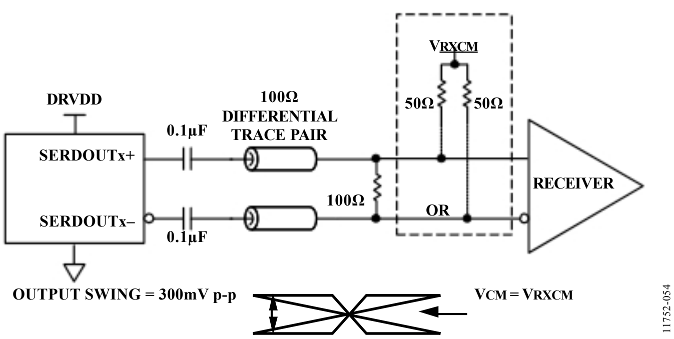


Figure 159. AC-Coupled Digital Output Termination Example

The CLM9680BCPZ digital outputs can interface with custom ASICs and FPGA receivers, providing superior switching performance in noisy environments. Single point-to-point network topologies are recommended with a single differential 100 Ω termination resistor placed as close to the receiver inputs as possible. The common mode of the digital output automatically biases itself to half the DRVDD supply of 1.2 V (V_{CM} = 0.6 V). See Figure 160 for dc coupling the outputs to the receiver logic.

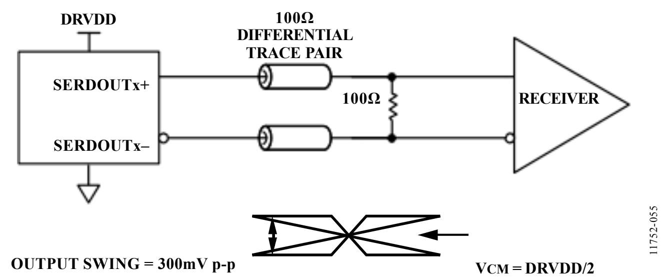


Figure 160. DC-Coupled Digital Output Termination Example

If there is no far-end receiver termination, or if there is poor differential trace routing, timing errors can result. To avoid such timing errors, it is recommended that the trace length be less than six inches, and that the differential output traces be close together and at equal lengths.

Figure 161 to Figure 166 show an example of the digital output data eye, time interval error (TIE) jitter histogram, and bathtub curve for one CLM9680BCPZ lane running at 10 Gbps and 6 Gbps, respectively. The format of the output data is twos complement by default. To change the output data format, see the Memory Map section (Register 0x561 in Table 39).

De-Emphasis

De-emphasis enables the receiver eye diagram mask to be met in conditions where the interconnect insertion loss does not meet the JESD204B specification. Use the de-emphasis feature only when the receiver is unable to recover the clock due to excessive insertion loss. Under normal conditions, it is disabled to conserve power. Additionally, enabling and setting too high a de-emphasis value on a short link can cause the receiver eye diagram to fail. Use the de-emphasis setting with caution because it can increase electromagnetic interference (EMI). See the Memory Map section (Register 0x5C1 to Register 0x5C5 in Table 39) for more details.

Phase-Locked Loop

The phase-locked loop (PLL) is used to generate the serializer clock, which operates at the JESD204B lane rate. The status of the PLL lock can be checked in the PLL locked status bit (Register 0x56F, Bit 7). This read only bit lets the user know if the PLL has achieved a lock for the specific setup. The JESD204B lane rate control, Bit 4 of Register 0x56E, must be set to correspond with the lane rate.

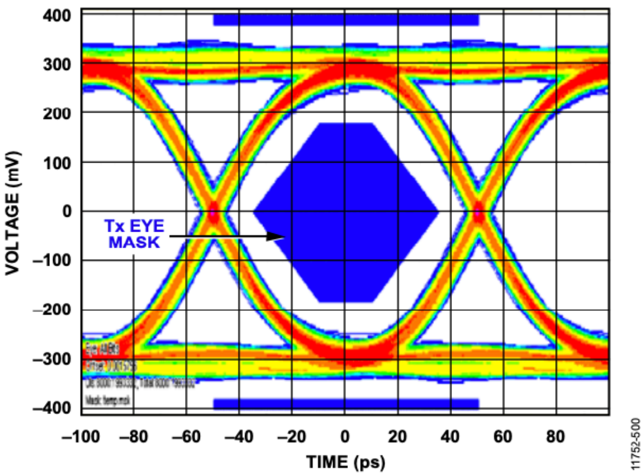


Figure 161. Digital Outputs Data Eye, External 100 Ω Terminations at 10 Gbps

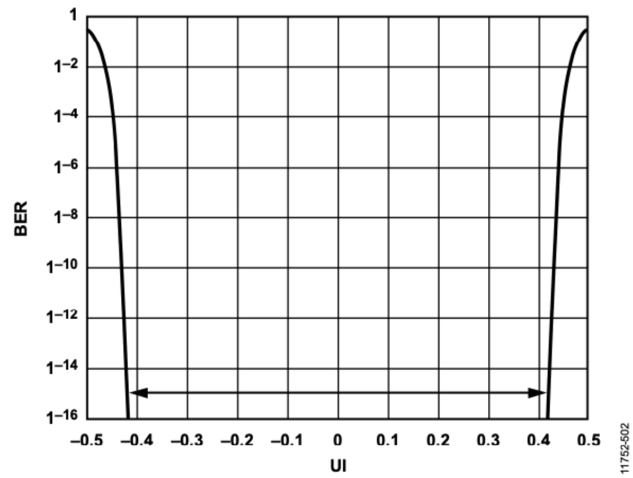


Figure 163. Digital Outputs Bathtub Curve, External 100 Ω Terminations at 10 Gbps

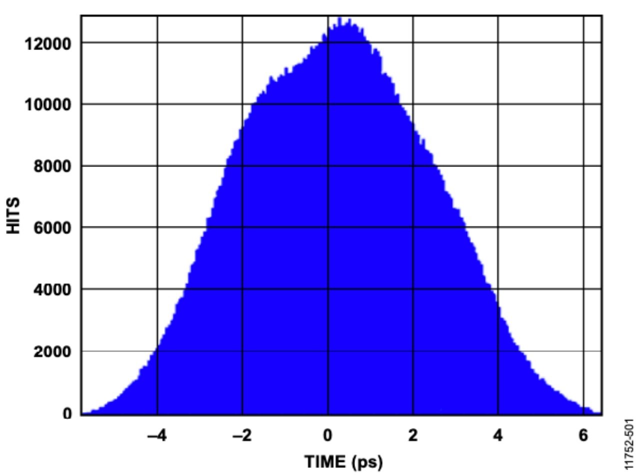


Figure 162. Digital Outputs Histogram, External 100 Ω Terminations at 10 Gbps

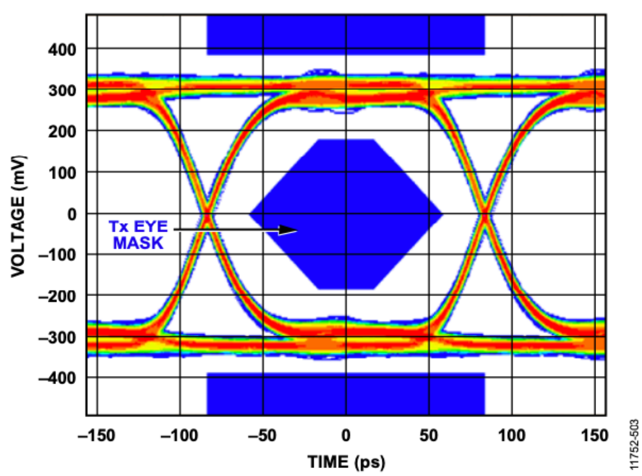


Figure 164. Digital Outputs Data Eye, External 100 Ω Terminations at 6 Gbps

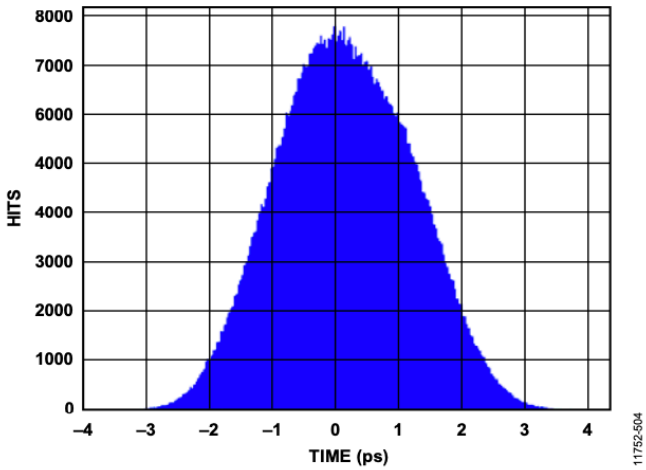


Figure 165. Digital Outputs Histogram, External 100 Ω Terminations at 6 Gbps

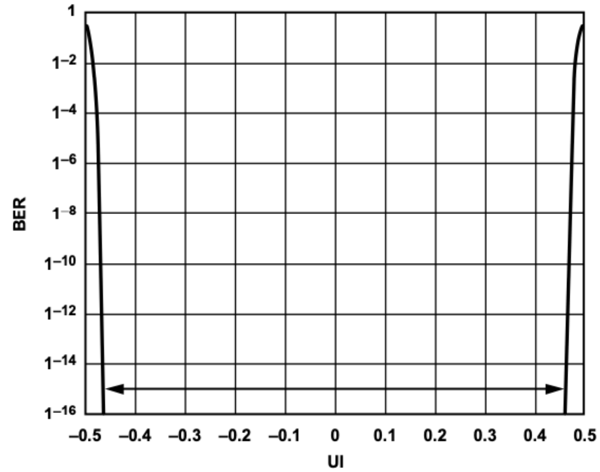


Figure 166. Digital Outputs Bathtub Curve, External 100 Ω Terminations at 6 Gbps

JESD204B TX CONVERTER MAPPING

To support the different chip operating modes, the CLM9680BCPZ design treats each sample stream (real or I/Q) as originating from separate virtual converters. The I/Q samples are always mapped in pairs with the I samples mapped to the first virtual converter and the Q samples mapped to the second virtual converter. With this transport layer mapping, the number of virtual converters are the same whether

- A single real converter is used along with a digital downconverter block producing I/Q outputs, or
- An Chiplon downconversion is used with two real converters producing I/Q outputs.

Figure 167 shows a block diagram of the two scenarios described for I/Q transport layer mapping.

The JESD204B Tx block for CLM9680BCPZ supports up to four DDC blocks. Each DDC block outputs either two sample streams (I/Q) for the complex data components (real + imaginary), or one sample stream for real (I) data. The JESD204B interface can be configured to use up to eight virtual converters depending on the DDC configuration. Figure 168 shows the virtual converters and their relationship to the DDC outputs when complex outputs are used. Table 25 shows the virtual converter mapping for each chip operating mode when channel swapping is disabled.

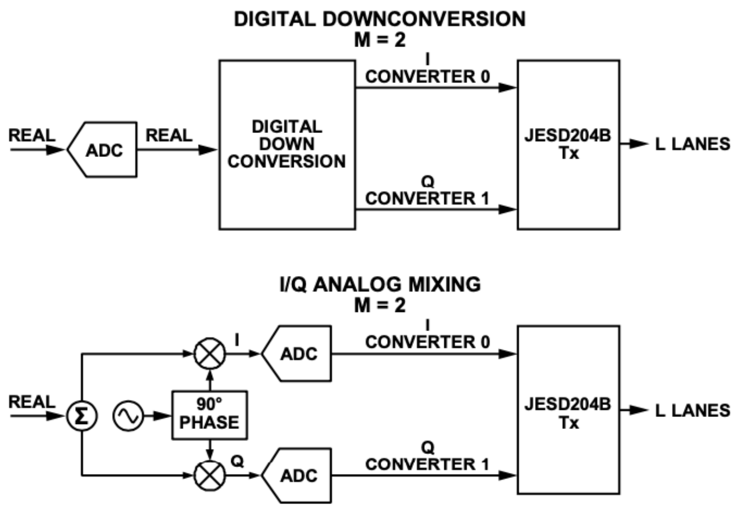


Figure 167. I/Q Transport Layer Mapping

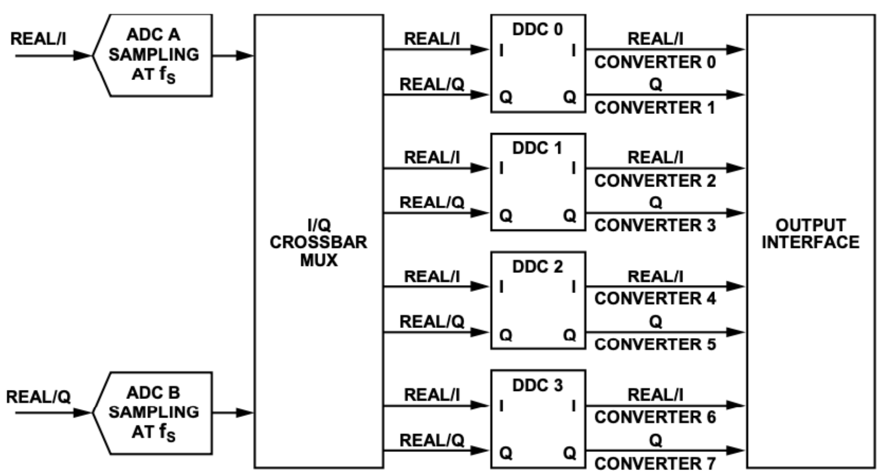


Figure 168. DDCs and Virtual Converter Mapping

Table 25. Virtual Converter Mapping

Number of Virtual Converters Supported	Chip Operating Mode (0x200, Bits[1:0])	Chip Q Ignore (0x200, Bit 5)	Virtual Converter Mapping							
			0	1	2	3	4	5	6	7
1 to 2	Full bandwidth mode (0x0)	Real or complex (0x0)	ADCA samples	ADCB samples	Unused	Unused	Unused	Unused	Unused	Unused
1	One DDC mode (0x1)	Real (I only) (0x1)	DDC 0 I samples	Unused	Unused	Unused	Unused	Unused	Unused	Unused
2	One DDC mode (0x1)	Complex (I/Q) (0x0)	DDC 0 I samples	DDC 0 Q samples	Unused	Unused	Unused	Unused	Unused	Unused
2	Two DDC mode (0x2)	Real (I only) (0x1)	DDC 0 I samples	DDC 1 I samples	Unused	Unused	Unused	Unused	Unused	Unused
4	Two DDC mode (0x2)	Complex (I/Q) (0x0)	DDC 0 I samples	DDC 0 Q samples	DDC 1 I samples	DDC 1 Q samples	Unused	Unused	Unused	Unused
4	Four DDC mode (0x3)	Real (I only) (0x1)	DDC 0 I samples	DDC 1 I samples	DDC 2 I samples	DDC 3 I samples	Unused	Unused	Unused	Unused
8	Four DDC mode (0x3)	Complex (I/Q) (0x0)	DDC 0 I samples	DDC 0 Q samples	DDC 1 I samples	DDC 1 Q samples	DDC 2 I samples	DDC 2 Q samples	DDC 3 I samples	DDC 3 Q samples

CONFIGURING THE JESD204B LINK

The CLM9680BCPZ has one JESD204B link. The device offers an easy way to set up the JESD204B link through the JESD04B quick configuration register (Register 0x570). The serial outputs (SERDOUT0± to SERDOUT3±) are considered to be part of one JESD204B link. The basic parameters that determine the link setup are

- Number of lanes per link (L)
- Number of converters per link (M)
- Number of octets per frame (F)

If the internal DDCs are used for on-chip digital processing, M represents the number of virtual converters. The virtual converter mapping setup is shown in Figure 168.

The maximum lane rate allowed by the JESD204B specification is 12.5 Gbps. The lane line rate is related to the JESD204B parameters using the following equation:

$$\text{Lane Line Rate} = \frac{M \times N' \times \left(\frac{10}{8}\right) \times f_{OUT}}{L}$$

where $f_{OUT} = \frac{f_{ADC\_CLOCK}}{\text{Decimation Ratio}}$

The decimation ratio (DCM) is the parameter programmed in Register 0x201.

The following steps can be used to configure the output:

1. Power down the link.
2. Select quick configuration options.
3. Configure detailed options.
4. Set output lane mapping (optional).
5. Set additional driver configuration options (optional).
6. Power up the link.

If the lane line rate calculated is less than 6.25 Gbps, select the low line rate option by programming a value of 0x10 to Register 0x56E.

Table 26 and Table 27 show the JESD204B output configurations supported for both N′ = 16 and N′ = 8 for a given number of virtual converters. Take care to ensure that the serial line rate for a given configuration is within the supported range of 3.125 Gbps to 12.5 Gbps.

Table 26. JESD204B Output Configurations for N′ = 16

Number of Virtual Converters Supported (Same Value as M)	JESD204B Quick Configuration (0x570)	JESD204B Serial Line Rate[1]	JESD204B Transport Layer Settings[2]								
			L	M	F	S	HD	N	N′	CS	K[3]
1	0x01	20 × f_{OUT}	1	1	2	1	0	8 to 16	16	0 to 3	Only valid K values that are divisible by 4 are supported
	0x40	10 × f_{OUT}	2	1	1	1	1	8 to 16	16	0 to 3	
	0x41	10 × f_{OUT}	2	1	2	2	0	8 to 16	16	0 to 3	
	0x80	5 × f_{OUT}	4	1	1	2	1	8 to 16	16	0 to 3	
	0x81	5 × f_{OUT}	4	1	2	4	0	8 to 16	16	0 to 3	
2	0x0A	40 × f_{OUT}	1	2	4	1	0	8 to 16	16	0 to 3	
	0x49	20 × f_{OUT}	2	2	2	1	0	8 to 16	16	0 to 3	
	0x88	10 × f_{OUT}	4	2	1	1	1	8 to 16	16	0 to 3	
	0x89	10 × f_{OUT}	4	2	2	2	0	8 to 16	16	0 to 3	
4	0x13	80 × f_{OUT}	1	4	8	1	0	8 to 16	16	0 to 3	
	0x52	40 × f_{OUT}	2	4	4	1	0	8 to 16	16	0 to 3	
	0x91	20 × f_{OUT}	4	4	2	1	0	8 to 16	16	0 to 3	
8	0x1C	160 × f_{OUT}	1	8	16	1	0	8 to 16	16	0 to 3	
	0x5B	80 × f_{OUT}	2	8	8	1	0	8 to 16	16	0 to 3	
	0x9A	40 × f_{OUT}	4	8	4	1	0	8 to 16	16	0 to 3	

[1] f_{OUT} = output sample rate = ADC sample rate/chip decimation ratio. The JESD204B serial line rate must be ≥3125 Mbps and ≤12,500 Mbps; when the serial line rate is ≤12.5 Gbps and ≥ 6.25 Gbps, the low line rate mode must be disabled (set Bit 4 to 0x0 in 0x56E). When the serial line rate is <6.25 Gbps and ≥3.125 Gbps, the low line rate mode must be enabled (set Bit 4 to 0x1 in 0x56E).

[2] JESD204B transport layer descriptions are as described in the JESD204B Overview section.

[3] For F = 1, K = 20, 24, 28, and 32. For F = 2, K = 12, 16, 20, 24, 28, and 32. For F = 4, K = 8, 12, 16, 20, 24, 28, and 32. For F = 8 and F = 16, K = 4, 8, 12, 16, 20, 24, 28, and 32.

Table 27. JESD204B Output Configurations for N′ = 8

Number of Virtual Converters Supported (Same Value as M)	JESD204B Quick Configuration (0x570)	Serial Line Rate[1]	JESD204B Transport Layer Settings[2]								
			L	M	F	S	HD	N	N′	CS	K[3]
1	0x00	10 × f_{OUT}	1	1	1	1	0	7 to 8	8	0 to 1	Only valid K values which are divisible by 4 are supported
	0x01	10 × f_{OUT}	1	1	2	2	0	7 to 8	8	0 to 1	
	0x40	5 × f_{OUT}	2	1	1	2	0	7 to 8	8	0 to 1	
	0x41	5 × f_{OUT}	2	1	2	4	0	7 to 8	8	0 to 1	
	0x42	5 × f_{OUT}	2	1	4	8	0	7 to 8	8	0 to 1	
	0x80	2.5 × f_{OUT}	4	1	1	4	0	7 to 8	8	0 to 1	
	0x81	2.5 × f_{OUT}	4	1	2	8	0	7 to 8	8	0 to 1	
2	0x09	20 × f_{OUT}	1	2	2	1	0	7 to 8	8	0 to 1	
	0x48	10 × f_{OUT}	2	2	1	1	0	7 to 8	8	0 to 1	
	0x49	10 × f_{OUT}	2	2	2	2	0	7 to 8	8	0 to 1	
	0x88	5 × f_{OUT}	4	2	1	2	0	7 to 8	8	0 to 1	
	0x89	5 × f_{OUT}	4	2	2	4	0	7 to 8	8	0 to 1	
	0x8A	5 × f_{OUT}	4	2	4	8	0	7 to 8	8	0 to 1	

[1] f_{OUT} = output sample rate = ADC sample rate/chip decimation ratio. The JESD204B serial line rate must be ≥3125 Mbps and ≤12,500 Mbps; when the serial line rate is ≤12.5 Gbps and ≥6.25 Gbps, the low line rate mode must be disabled (set Bit 4 to 0x0 in Register 0x56E). When the serial line rate is <6.25 Gbps and ≥3.125 Gbps, the low line rate mode must be enabled (set Bit 4 to 0x1 in Register 0x56E).
[2] JESD204B transport layer descriptions are as described in the JESD204B Overview section.
[3] For F = 1, K = 20, 24, 28, and 32. For F = 2, K = 12, 16, 20, 24, 28, and 32. For F = 4, K = 8, 12, 16, 20, 24, 28, and 32. For F = 8 and F = 16, K = 4, 8, 12, 16, 20, 24, 28, and 32.

See the Example 1: Full Bandwidth Mode section and the Example 2: ADC with DDC Option (Two ADCs Plus Four DDCs) section for two examples describing which JESD204B transport layer settings are valid for a given chip mode.

Example 1: Full Bandwidth Mode

Chip application mode = full bandwidth mode (see Figure 169).

· Two 14-bit converters at 1000 MSPS
· Full bandwidth application layer mode
· No decimation

JESD204B output configuration is as follows:

· Two virtual converters required (see Table 26)
· Output sample rate (f_{OUT}) = 1000/1 = 1000 MSPS

JESD204B supported output configurations (see Table 26) include:

· N′ = 16 bits
· N = 14 bits
· L = 4, M = 2, and F = 1, or L = 4, M = 2, and F = 2 (quick configuration = 0x88 or 0x89)
· CS = 0 to 2
· K = 32
· Output serial line rate = 10 Gbps per lane, low line rate mode disabled

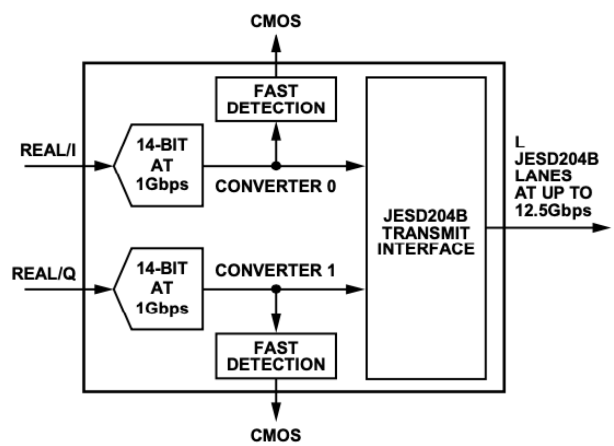


Figure 169. Full Bandwidth Mode

Example 2: ADC with DDC Option (Two ADCs Plus Four DDCs)

Chip application mode = four-DDC mode. (see Figure 170).

· Two 14-bit converters at 1 GSPS
· Four DDC application layer mode with complex outputs (I/Q)
· Chip decimation ratio = 16
· DDC decimation ratio = 16 (see Table 15).

JESD204B output configuration is as follows:

· Virtual converters required = 8 (see Table 26)
· Output sample rate (f_{OUT}) = 1000/16 = 62.5 MSPS

JESD204B supported output configurations (see Table 26):

- N′ = 16 bits
- N = 14 bits
- L = 1, M = 8, and F = 16, or L = 2, M = 8, and F = 8 (quick configuration = 0x1C or 0x5B)
- CS = 0 to 1
- K = 32
- Output serial line rate = 10 Gbps per lane (L = 1) or 5 Gbps per lane (L = 2)

For L = 1, low line rate mode is disabled. For L = 2, low line rate mode is enabled.

Example 2 shows the flexibility in the digital and lane configurations for the CLM9680BCPZ. The sample rate is 1 GSPS; however, the outputs are all combined in either one or two lanes, depending on the I/O speed capability of the receiving device.

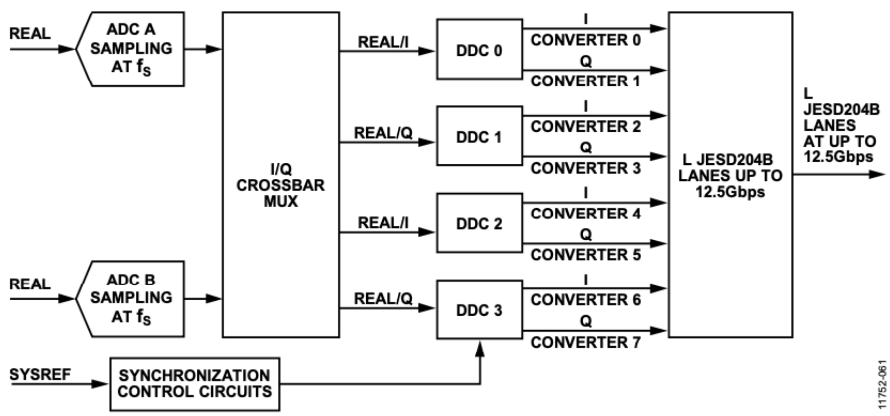


Figure 170. Two ADC Plus Four DDC Mode

DETERMINISTIC LATENCY

Both ends of the JESD204B link contain various clock domains distributed throughout each system. Data traversing from one clock domain to a different clock domain can lead to ambiguous delays in the JESD204B link. These ambiguities lead to nonrepeatable latencies across the link from one power cycle or link reset to the next. Section 6 of the JESD204B specification addresses the issue of deterministic latency with mechanisms defined as Subclass 1 and Subclass 2.

The CLM9680BCPZ supports JESD204B Subclass 0 and Subclass 1 operation. Register 0x590, Bit 5 sets the subclass mode for the CLM9680BCPZ; the default mode is the Subclass 1 operating mode (Register 0x590, Bit 5 = 1). If deterministic latency is not a system requirement, Subclass 0 operation is recommended and the SYSREF± signal may not be required. Even in Subclass 0 mode, the SYSREF± signal may be required in an application where multiple CLM9680BCPZ devices must be synchronized with each other. This topic is addressed in the Timestamp Mode section.

SUBCLASS 0 OPERATION

If there is no requirement for multichip synchronization while operating in Subclass 0 mode (Register 0x590, Bit 5 = 0), the SYSREF± input can be left disconnected. In this mode, the relationship of the JESD204B clocks between the JESD204B transmitter and receiver are arbitrary but does not affect the ability of the receiver to capture and align the lanes within the link.

SUBCLASS 1 OPERATION

The JESD204B protocol organizes data samples into octets, frames, and multiframes as described in the Transport Layer section. The local multiframe clock (LMFC) is synchronous with the beginnings of these multiframes. In Subclass 1 operation, the SYSREF± signal synchronizes the LMFCs for each device in a link or across multiple links (within the CLM9680BCPZ, SYSREF± also synchronizes the internal sample dividers), as shown in Figure 171. The JESD204B receiver uses the multiframe boundaries and buffering to achieve consistent latency across lanes (or even multiple devices), and also to achieve a fixed latency between power cycles and link reset conditions.

Deterministic Latency Requirements

Several key factors are required for achieving deterministic latency in a JESD204B Subclass 1 system:

- SYSREF± signal distribution skew within the system must be less than the desired uncertainty for the system.
- SYSREF± setup and hold time requirements must be met for each device in the system.
- The total latency variation across all lanes, links, and devices must be ≤1 LMFC period (see Figure 171). This includes both variable delays and the variation in fixed delays from lane to lane, link to link, and device to device in the system.

Setting Deterministic Latency Registers

The JESD204B receive buffer in the logic device buffers data starting on the LMFC boundary. If the total link latency in the system is near an integer multiple of the LMFC period, it is possible that from one power cycle to the next, the data arrival time at the receive buffer may straddle an LMFC boundary. To ensure deterministic latency in this case, a phase adjustment of the LMFC at either the transmitter or receiver must be performed. Typically, adjustments to accommodate the receive buffer are made to the LMFC of the receiver. In the CLM9680BCPZ, this adjustment can be made using the LMFC offset bits (Register 0x578, Bits[4:0]). These bits delay the LMFC in frame clock increments, depending on the F parameter, which is the number of octets per lane per frame). For F = 1, every 4th setting (0, 4, 8, …, and so on) results in a 1-frame clock shift. For F = 2, every other setting (0, 2, 4, …, and so on) results in a 1-frame clock shift. For all other values of F, each setting results in a 1-frame clock shift.

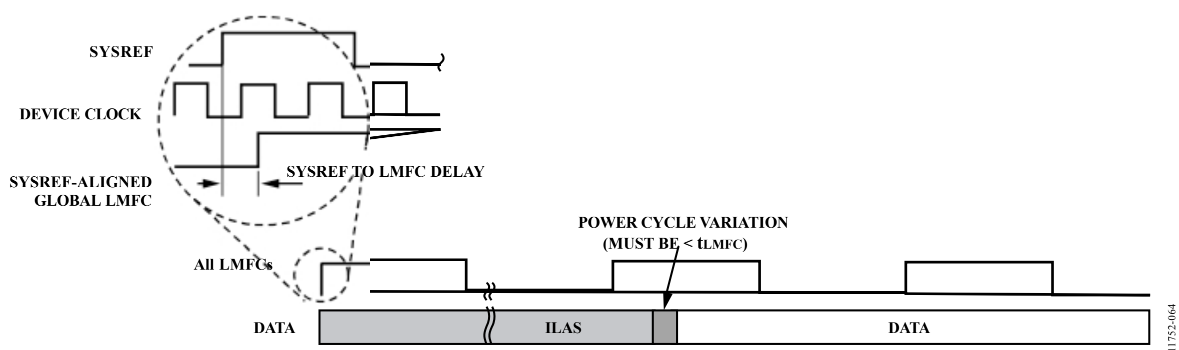


Figure 171. SYSREF± and LMFC

Figure 172 shows that, in the case where the link latency is near an LMFC boundary, the local LMFC of the CLM9680BCPZ can be delayed to in turn delay the data arrival time at the receiver. Figure 173 shows how the LMFC of the receiver is delayed to accommodate the receive buffer timing. Refer to the applicable JESD204B receiver user guide for details on making this adjustment. If the total latency in the system is not near an integer multiple of the LMFC period, or if the appropriate adjustments have been made to the LMFC phase at the clock source, it is still possible to have variable latency from one power cycle to the next. In this case, check for the possibility that the setup and hold time requirements for the SYSREF± signal are not being met. Perform this check by reading the SYSREF± setup and hold monitor register (Register 0x128).

This function is described in the SYSREF± Setup/Hold Window Monitor section.

If reading Register 0x128 indicates a timing problem, there are adjustments that can made in the CLM9680BCPZ. Changing the SYSREF± level used for alignment is possible using the SYSREF± transition select bit (Register 0x120, Bit 4). Also, changing which edge of the clock is used to capture SYSREF± can be performed using the clock edge select bit (Register 0x120, Bit 3). Both of these options are described in the SYSREF± Control Features section. If neither of these measures help achieve an acceptable setup and hold time, adjusting the phase of SYSREF± and/or the device clock (CLK±) may be required.

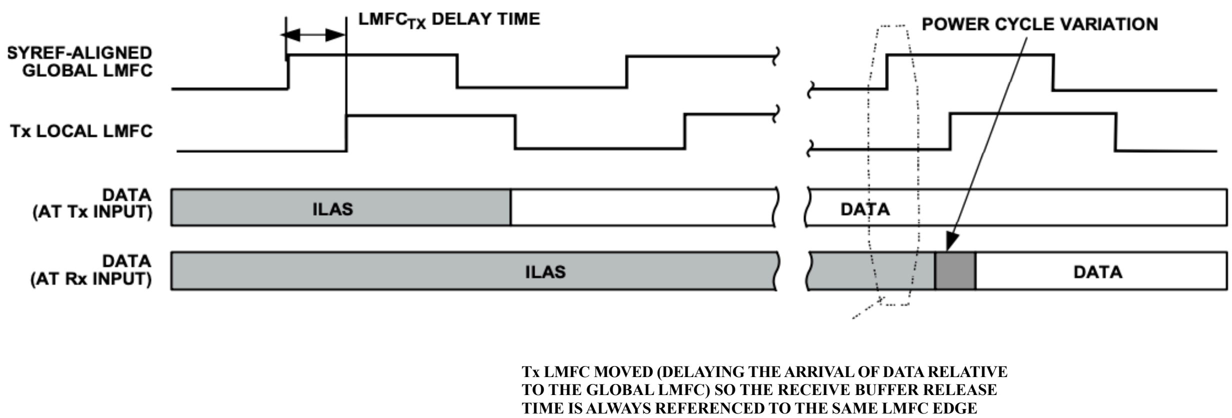


Figure 172. Adjusting the JESD204B Tx LMFC in the CLM9680BCPZ

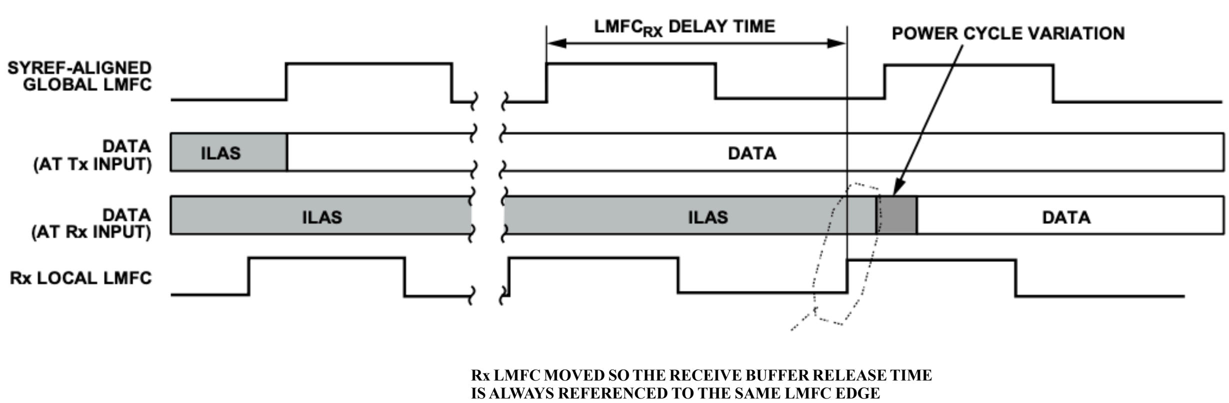


Figure 173. Adjusting the JESD204B Rx LMFC in the Logic Device

MULTICHIP SYNCHRONIZATION

The flowchart shown in Figure 175 describes the internal mechanism for multichip synchronization in the CLM9680BCPZ.

There are two methods by which multichip synchronization can take place, as determined by the chip synchronization mode bit (Register 0x1FF , Bit 0). Each method involves different applications of the SYSREF± signal.

NORMAL MODE

The default sate of the chip synchronization mode bit is 0, which configures the CLM9680BCPZ for normal chip synchronization. The JESD204B standard specifies the use of SYSREF± to provide deterministic latency within a single link. This same concept, when applied to a system with multiple converters and logic devices, can also provide multichip synchronization. In Figure 175, this is referred to as normal mode. Following the process outlined in the flowchart ensures that the CLM9680BCPZ is configured appropriately. Consult the logic devices user intellectual property (IP) guide to ensure that the JESD204B receivers are configured appropriately.

TIMESTAMP MODE

For all CLM9680BCPZ full bandwidth operating modes, the SYSREF input can also be used to timestamp samples. This is another method by which multiple channels and multiple devices can achieve synchronization. This is especially effective when synchronizing multiple devices to one or more logic devices. The logic devices simply buffer the data streams, identify the time stamped samples and align them. When the chip synchronization mode bit (0x1FF [0]) is set to 1, the timestamp method is used for synchronization of multiple channels and/or devices. In timestamp mode, the clocks are not reset but instead, the coinciding sample is time stamped using the JESD204B control bits of that sample. To operate in timestamp mode, these additional settings are necessary:

- Continuous or N-shot SYSREF enabled (0x120[2:1] = 1 or 2)
- At least one control bit must be enabled (CS > 0, Register 0x58F, Bits[7:6] = 1, 2, or 3)
- Set the function for one of the control bits to SYSREF
  - Register 0x559, Bits[2:0] = 5 if using Control Bit 0
  - Register 0x559, Bits[6:4] = 5 if using Control Bit 1
  - Register 0x55A, Bits[2:0] = 5 if using Control Bit 2

Control bits must be enabled MSB first. In other words, if only using one control bit (CS = 1), Control Bit 2 must be enabled. If two control bits are sued, then Control Bits[2:1] must be enabled. Figure 174 provides an illustration of how the input sample coincident with SYSREF is time stamped and ultimately output of the ADC. In this example, there are two control bits and Control Bit 1 is the bit indicating which sample was coincident with the SYSREF rising edge. Note that the pipeline latencies for each channel are identical. If so desired, the SYSREF timestamp delay register (0x123) can be used to adjust the timing of which sample is time stamped.

Note that time stamping is not supported by any CLM9680BCPZ operating modes that use decimation.

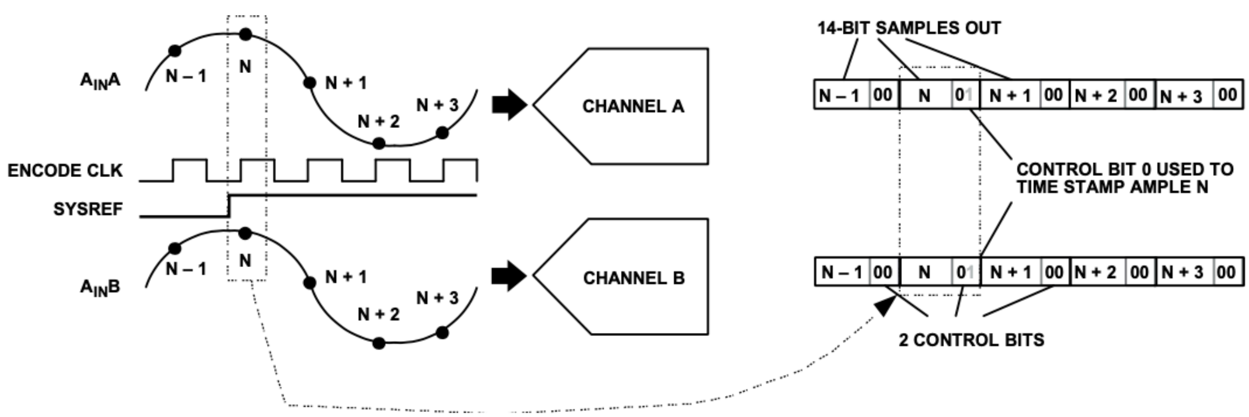


Figure 174. CLM9680BCPZ Timestamping—CS = 2 (Register 0x58F, Bits[7:6] = 2), Control Bit 1 is SYSREF± (Register 0x559, Bits[6:4] = 5)

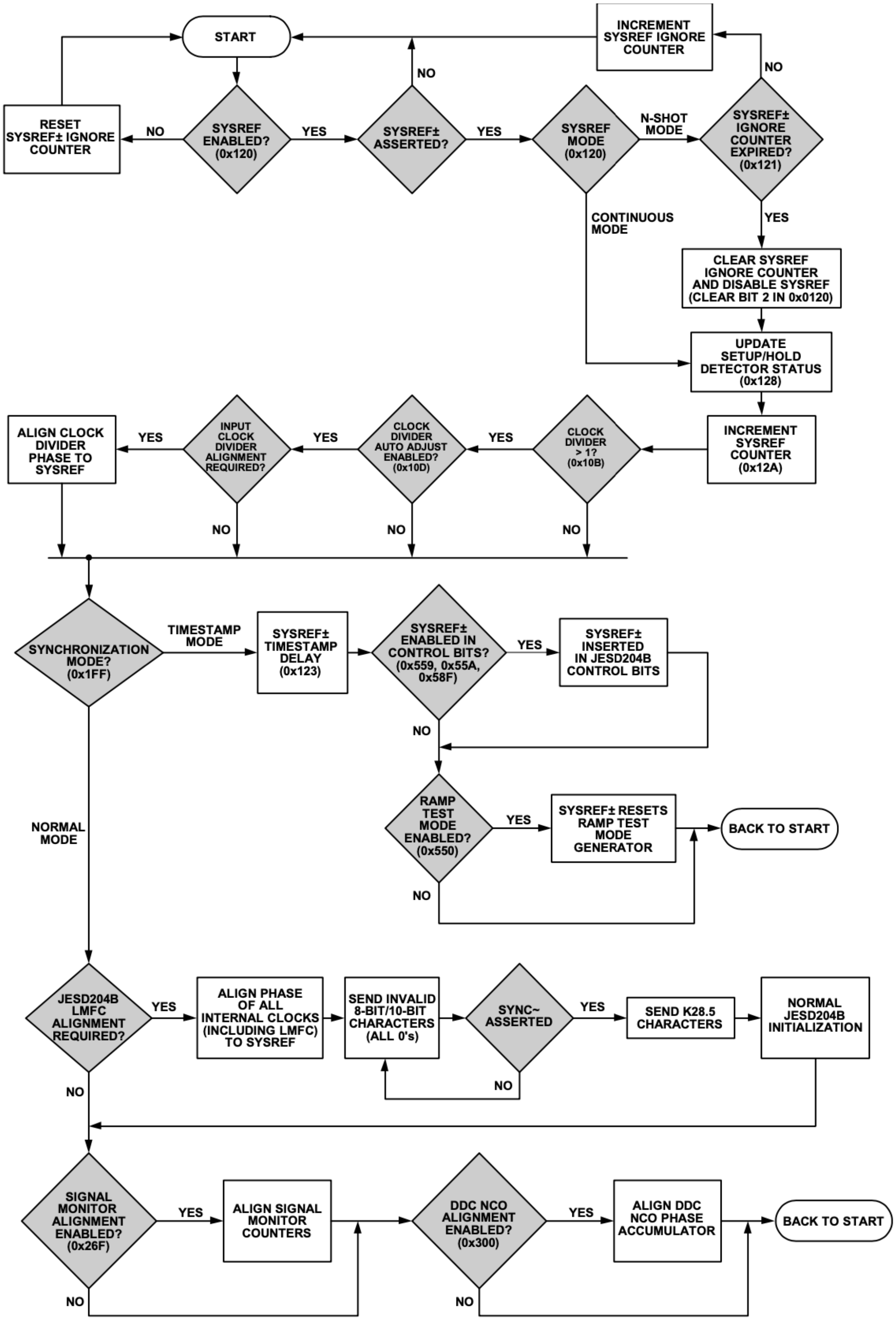


Figure 175. SYSREF± Capture Scenarios and Multichip Synchronization

SYSREF± INPUT

The SYSREF± input signal is used as a high accuracy system reference for deterministic latency and multichip synchronization. The CLM9680BCPZ accepts a single-shot or periodic input signal. The SYSREF± mode select bits (Register 0x120, Bits[2:1]) select the input signal type and also arm the SYSREF± state machine when set. If in single- (or N) shot mode (Register 0x120, Bits[2:1] = 2), the SYSREF± mode select bit self clears after the appropriate SYSREF± transition is detected. The pulse width must have a minimum width of two CLK± periods. If the clock divider (Register 0x10B, Bits[2:0]) is set to a value other than divide by 1, then multiply this minimum pulse width requirement by the divide ratio (for example, if set to divide by 8, the minimum pulse width is 16 CLK± cycles). When using a continuous SYSREF± signal (Register 0x120, Bits[2:1] = 1), the period of the SYSREF± signal must be an integer multiple of the LMFC. Derive the LMFC using the following formula:

$$LMFC = ADC\ Clock/S \times K$$

where:

S is the JESD204B parameter for number of samples per converter.

K is JESD204B parameter for number of frames per multiframe.

The input clock divider, DDCs, signal monitor block, and JESD204B link are all synchronized using the SYSREF± input when in normal synchronization mode (Register 0x1FF, Bits[1:0] = 0). The SYSREF± input can also be used to time stamp an ADC sample to provide a mechanism for synchronizing multiple CLM9680BCPZ devices in a system. For the highest level of timing accuracy, SYSREF± must meet the setup and hold requirements relative to the CLK± input. There are several features in the CLM9680BCPZ to ensure these requirements are met (see the SYSREF± Control Features section).

SYSREF± Control Features

SYSREF± is used, along with the input clock (CLK±), as part of a source synchronous timing interface and requires setup and hold timing requirements of 117 ps and −96 ps, relative to the input clock (see Figure 176). The CLM9680BCPZ has several features to meet these requirements. First, the SYSREF± sample event can be defined as either a synchronous low to high transition or synchronous high to low transition. Second, the CLM9680BCPZ allows the SYSREF± signal to be sampled using either the rising edge or falling edge of the input clock. Figure 176, Figure 177, Figure 178, and Figure 179 show all four possible combinations. The third SYSREF± related feature available is the ability to ignore a programmable number (up to 16) of SYSREF± events.

The SYSREF± ignore feature is enabled by setting the SYSREF± mode register (Register 0x0120, Bits[2:1]) to 2’b10, which is labeled as N-shot mode. The CLM9680BCPZ is able to ignore N SYSREF± events, which is useful to handle periodic SYSREF± signals that require time to settle after startup. Ignoring SYSREF± until the clocks in the system have settled avoids an inaccurate SYSREF± trigger. Figure 180 shows an example of the SYSREF± ignore feature when ignoring three SYSREF± events.

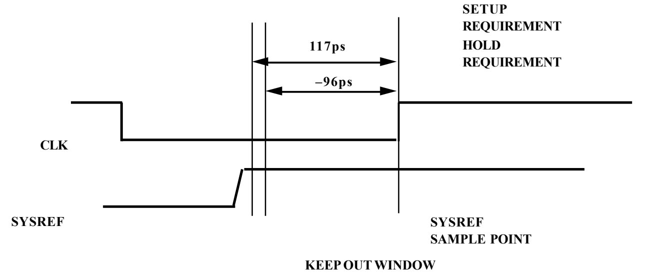


Figure 176. SYSREF± Setup and Hold Time Requirements; SYSREF± Low to High Transition Using the Rising Edge Clock (Default)

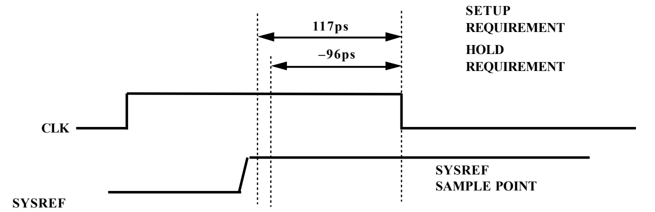


Figure 177. SYSREF± Low to High Transition Using Falling Edge Clock Capture (Register 0x0120, Bit 4 = 1’b0 and Register 0x0120, Bit 3 = 1’b1)

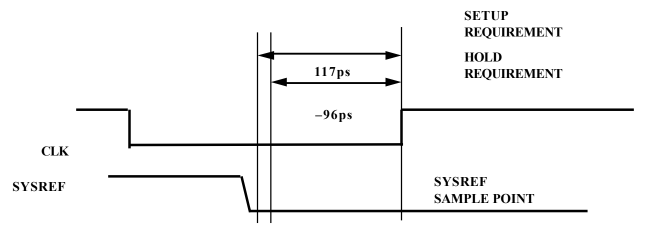


Figure 178. SYSREF± High to Low Transition Using Rising Edge Clock Capture (Register 0x0120, Bit 4 = 1’b1 and Register 0x0120, Bit 3 = 1’b0)

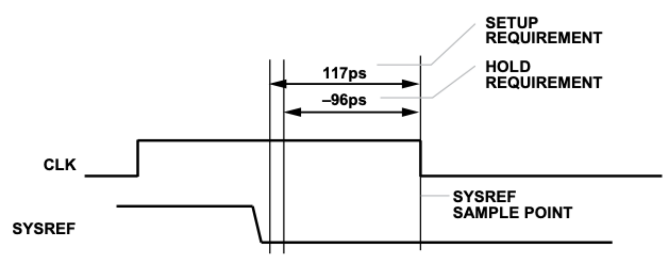


Figure 179. SYSREF± High to Low Transition Using Falling Edge Clock Capture (Register 0x0120, Bit 4= 1’b1 and Register 0x0120, Bit 3 = 1’b1)

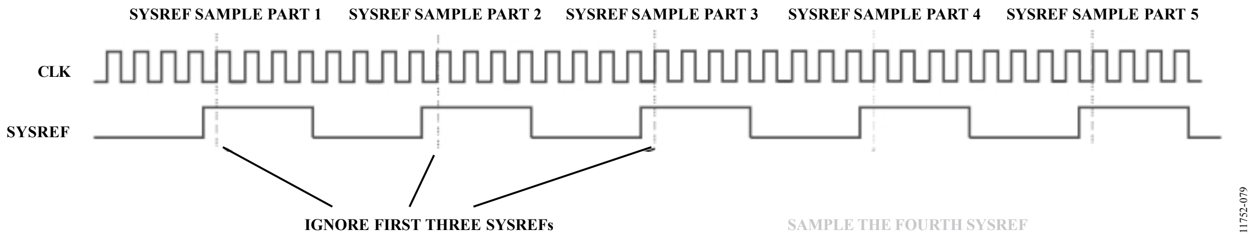


Figure 180. SYSREF± Ignore Example; SYSREF± Ignore Count Bits (Register 0x0121, Bits[3:0]) = 3

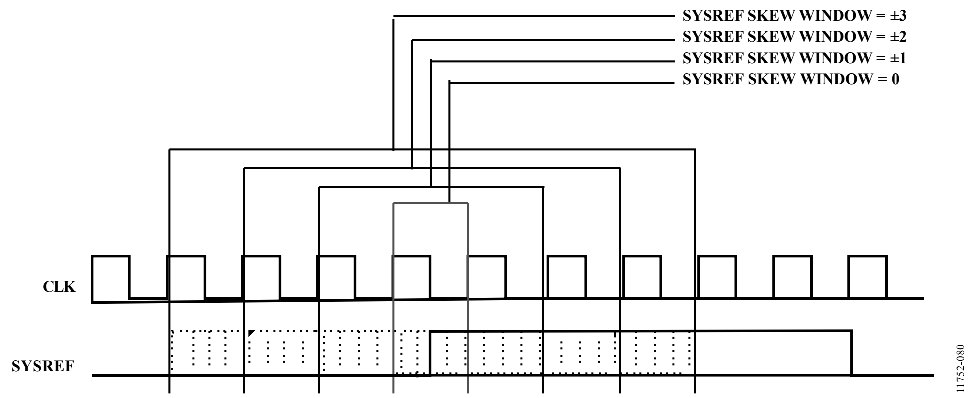


Figure 181. SYSREF± Skew Window

When in continuous SYSREF± mode (Register 0x120, Bits[2:1] = 1), the CLM9680BCPZ monitors the placement of the SYSREF± leading edge compared to the internal LMFC. If the SYSREF± edge is captured with a clock edge other than the one that is aligned with LMFC, the CLM9680BCPZ initiates a resynchronization of the link. Because the input clock rates for the CLM9680BCPZ can be up to 4 GHz, the CLM9680BCPZ provides another SYSREF± related feature that makes it possible to accommodate periodic SYSREF± signals where cycle accurate capture is not feasible or not required. For these scenarios, the CLM9680BCPZ has a programmable SYSREF± skew window that allows the internal dividers to remain undisturbed, unless SYSREF± occurs outside the skew window. The resolution of the SYSREF± skew window is set in sample clock cycles. If the SYSREF± negative skew window is 1 and the positive skew window is 1, then the total skew window is ±1 sample clock cycles, meaning that, as long as SYSREF± is captured within ±1 sample clock cycle of the clock that is aligned with LMFC, the link continues to operate normally. If the SYSREF± has jitter, which can cause a misalignment between SYSREF± and the LMFC, the system continues to run without a resynchro- nization, while still allowing the device to monitor for larger errors not caused by jitter. For the CLM9680BCPZ, the positive and negative skew window is controlled by the SYSREF± window negative bits (Register 0x0122, Bits[3:2]) and the SYSREF± window positive bits (Register 0x0122, Bits[1:0]). Figure 181 shows information on the location of the skew window settings relative to Phase 0 of the internal dividers. Negative skew is defined as occurring before the internal dividers reach Phase 0 and positive skew is defined after the internal dividers reach Phase 0.

SYSREF± SETUP/HOLD WINDOW MONITOR

To ensure a valid SYSREF± signal capture, the CLM9680BCPZ has a SYSREF± setup/hold window monitor. This feature allows the system designer to determine the location of the SYSREF± signals relative to the CLK± signals by reading back the amount of setup/hold margin on the interface through the memory map. Figure 182 and Figure 183 show the setup and hold status values for different phases of SYSREF±. The setup detector returns the status of the SYSREF± signal before the CLK± edge, and the hold detector returns the status of the SYSREF signal after the CLK± edge. Register 0x128 stores the status of SYSREF± and lets the user know if the SYSREF± signal is captured by the ADC.

Table 28 describes the contents of Register 0x128 and how to interpret them.

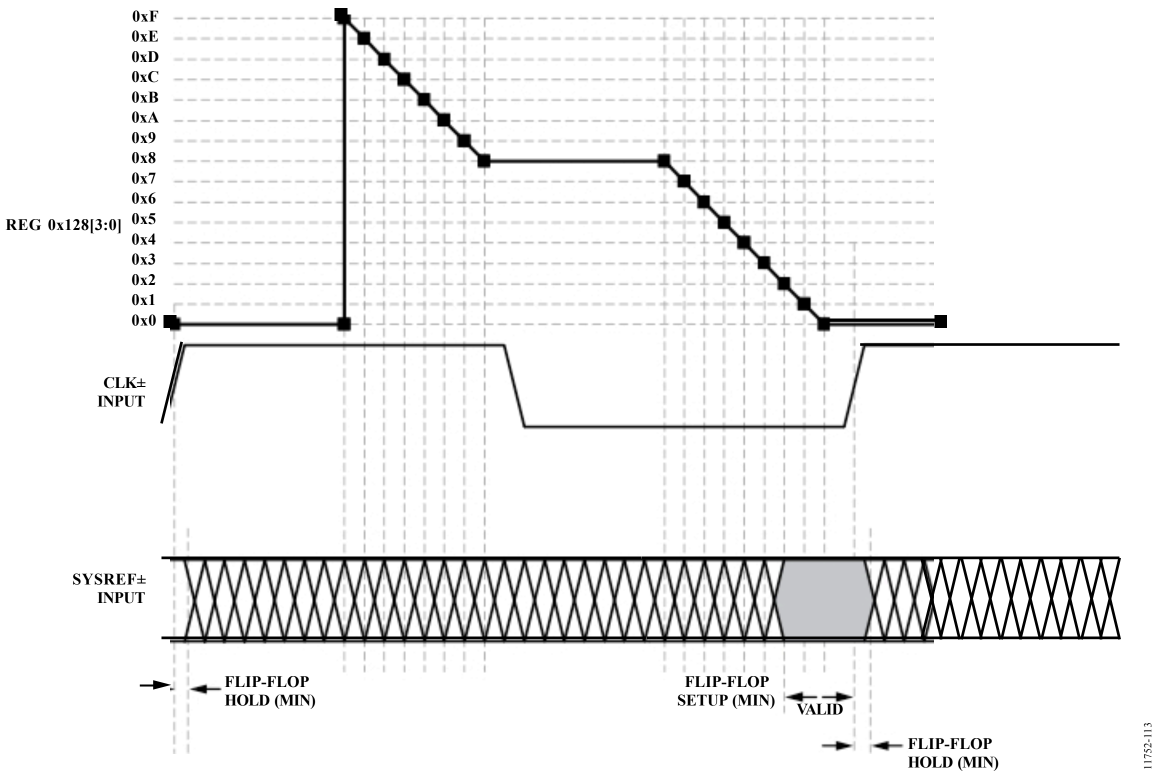


Figure 182. SYSREF± Setup Detector

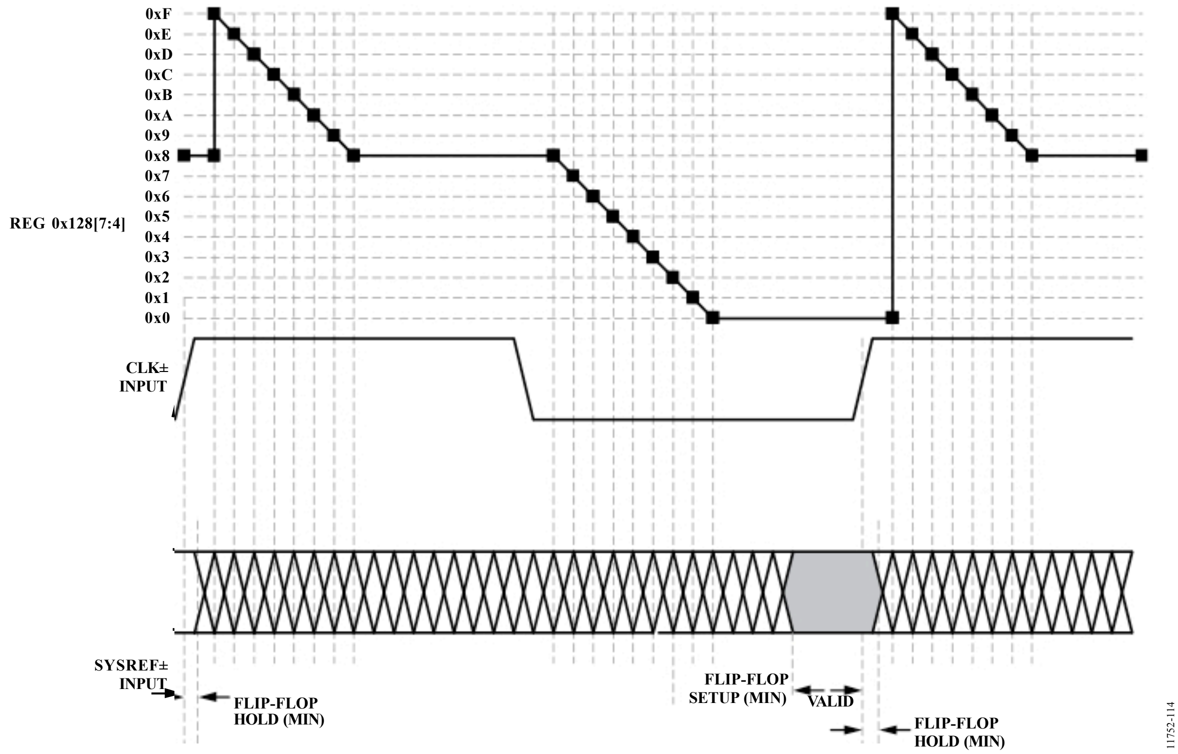


Figure 183. SYSREF± Hold Detector

Table 28. SYSREF± Setup/Hold Monitor, Register 0x128

Register 0x128[7:4] Hold Status	Register 0x128[3:0] Setup Status	Description
0x0	0x0 to 0x7	Possible setup error. The smaller this number, the smaller the setup margin.
0x0 to 0x8	0x8	No setup or hold error (best hold margin).
0x8	0x9 to 0xF	No setup or hold error (best setup and hold margin).
0x8	0x0	No setup or hold error (best setup margin).
0x9 to 0xF	0x0	Possible hold error. The larger this number, the smaller the hold margin.
0x0	0x0	Possible setup or hold error.

LATENCY

END TO END TOTAL LATENCY

Total latency in the CLM9680BCPZ is dependent on the various digital signal processing (DSP) and JESD204B configuration modes. Latency is fixed at 26 encode clocks through the ADC itself; however, the latency through the DSP and JESD204B blocks can vary greatly, depending on the configuration. Therefore, total latency must be calculated based on the DSP options selected and the JESD204B configuration.

Table 29 shows the combined latency through the ADC and DSP blocks (including data formatting) for the different application modes supported by the CLM9680BCPZ. Table 30 shows the latency through the JESD204B block for each JESD204B configuration and the various decimation modes supported for those modes. For both tables, latency is in units of the encode clock. Latency through the JESD204B clock can also be affected by the decimation ratio in some JESD204B configurations. Table 31 shows the latency for these modes for each of the possible decimation ratios.

Table 29. Latency Through the ADC and DSP Blocks

ADC Application Mode	Latency (No. of Encode Clocks), ADC+DSP Total
Full Bandwidth	29
DDC (HB1) (no mixer, complex outputs)	78
DDC (HB2 + HB1) (no mixer, complex outputs)	132
DDC (HB3 +HB2 + HB1) (no mixer, complex outputs)	232
DDC (HB4 + HB3 + HB2 + HB1) (no mixer, complex outputs)	432
DEC2 + NSR	57
NSR	35
VDR	33

EXAMPLE LATENCY CALCULATION

For a configuration where the ADC application mode is full bandwidth, the decimation ratio = 2, L = 4, M = 2, F = 1, and S = 1 (JESD204B mode),

Latency = 29 + 30 = 59 encode clocks

Table 30. Latency Through JESD204B Block—Full Bandwidth Modes

JESD204B Quick Configuration (Register 0x570)	Decimation Ratio	JESD204B Transport Layer Settings							Latency (Encode CLK)
		L	M	F	S	HD	N	N′	
0x01	1	1	1	2	1	0	8 to 16	16	13
0x40	1	2	1	1	1	1	8 to 16	16	28
0x41	1	2	1	2	2	0	8 to 16	16	28
0x80	1	4	1	1	2	1	8 to 16	16	53
0x81	1	4	1	2	4	0	8 to 16	16	53
0x0A	1	1	2	4	1	0	8 to 16	16	7
0x49	1	2	2	2	1	0	8 to 16	16	13
0x88	1	4	2	1	1	1	8 to 16	16	28
0x89	1	4	2	2	2	0	8 to 16	16	28

Table 31. Latency Through JESD204B Block—with Decimation

JESD204B Quick Configuration (Register 0x570)	Decimation Ratio	JESD204B Transport Layer Settings							Latency (Encode CLK)
		L	M	F	S	HD	N	N′	
0x88	2	4	2	1	1	1	8 to 16	16	30
0x89	2	4	2	2	2	0	8 to 16	16	30
0x13	2,4,8,16[1]	1	4	8	1	0	8 to 16	16	4
0x52	2,4,8,16[1]	2	4	4	1	0	8 to 16	16	7
0x91	2,4,8,16[1]	4	4	2	1	0	8 to 16	16	13
0x1C	4,8,16[1]	1	8	16	1	0	8 to 16	16	2
0x5B	4,8,16[1]	2	8	8	1	0	8 to 16	16	4
0x9A	4,8,16[1]	4	8	4	1	0	8 to 16	16	7

[1] For these modes, changing decimation does not affect latency.

TEST MODES

ADC TEST MODES

The CLM9680BCPZ has various test options that aid in the system level implementation. The CLM9680BCPZ has ADC test modes that are available in Register 0x0550. These test modes are described in Table 36. When an output test mode is enabled, the Chiplon section of the ADC is disconnected from the digital back end blocks, and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting, and some are not. The pseudorandom number (PN) generators from the PN sequence tests can be reset by setting Bit 4 or Bit 5 of Register 0x0550. These tests can be performed with or without an Chiplon signal (if present, the Chiplon signal is ignored); however, they do require an encode clock.

If the application mode is set to select a DDC mode of operation, the test modes must be enabled for each DDC enabled. The test patterns can be enabled via Bit 2 and Bit 0 of Register 0x0327, Register 0x0347, and Register 0x0367, depending on which DDC(s) are selected. The (I) data uses the test patterns selected for Channel A, and the (Q) data uses the test patterns selected for Channel B. For DDC3 only, the (I) data uses the test patterns from Channel A, and the (Q) data does not output test patterns. Bit 0 of Register 0x0387 selects the Channel A test patterns to be used for the (I) data. For more information, see the AN-877 Application Note, Interfacing to High Speed ADCs via SPI.

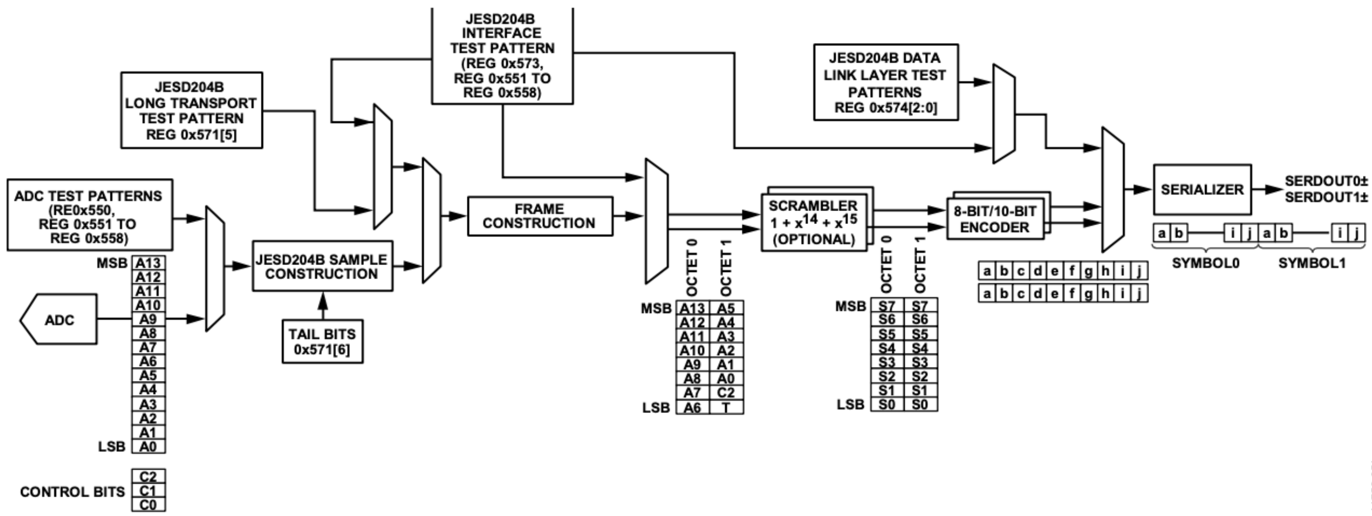


Figure 184. ADC Output Data Path Showing Data Framing

Table 36. ADC Test Modes[1]

Output Test Mode Bit Sequence	Pattern Name	Expression	Default/ Seed Value	Sample (N, N + 1, N + 2, …)
0000	Off (default)	N/A	N/A	N/A
0001	Midscale short	0000 0000 0000	N/A	N/A
0010	Positive full-scale short	01 1111 1111 1111	N/A	N/A
0011	Negative full-scale short	10 0000 0000 0000	N/A	N/A
0100	Checkerboard	10 1010 1010 1010	N/A	0x1555, 0x2AAA, 0x1555, 0x2AAA, 0x1555
0101	PN sequence long	$x^{23} + x^{18} + 1$	0x3AFF	0x3FD7, 0x0002, 0x26E0, 0x0A3D, 0x1CA6
0110	PN sequence short	$x^9 + x^5 + 1$	0x0092	0x125B, 0x3C9A, 0x2660, 0x0c65, 0x0697
0111	One-/zero-word toggle	11 1111 1111 1111	N/A	0x0000, 0x3FFF, 0x0000, 0x3FFF, 0x0000
1000	User input	Register 0x551 to Register 0x558	N/A	User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], User Pattern 1[15:2] … for repeat mode. User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], 0x0000 … for single mode.
1111	Ramp Output	$(x) \% 2^{14}$	N/A	$(x) \% 2^{14}$, $(x + 1) \% 2^{14}$, $(x + 2) \% 2^{14}$, $(x + 3) \% 2^{14}$

[1] N/A means not applicable.

JESD204B BLOCK TEST MODES

In addition to the ADC pipeline test modes, the CLM9680BCPZ also has flexible test modes in the JESD204B block. These test modes are listed in Register 0x0573 and Register 0x0574. These test patterns can be injected at various points along the output datapath. These test injection points are shown in Figure 184. Table 37 describes the various test modes available in the JESD204B block. For the CLM9680BCPZ, a transition from test modes (Register 0x0573 ≠ 0x00)

to normal mode (Register 0x0573 = 0x00) requires an SPI soft reset. This is done by writing 0x81 to Register 0x0000 (self cleared).

Transport Layer Sample Test Mode

The transport layer samples are implemented in the CLM9680BCPZ as defined by Section 5.1.6.3 in the JEDEC JESD204B specification.

These tests are shown in Register 0x0571, Bit 5. The test pattern is equivalent to the raw samples from the ADC.

Interface Test Modes

The interface test modes are described in Register 0x0573, Bits[3:0]. These test modes are also explained in Table 37. The interface tests can be injected at various points along the data. See Figure 87

for more information on the test injection points. Register 0x0573, Bits[5:4] show where these tests are injected.

Table 38, Table 39, and Table 40 show examples of some of the test modes when injected at the JESD sample input, PHY 10-bit input, and scrambler 8-bit input. UPx in the tables represent the user pattern control bits from the customer register map.

Table 37. JESD204B Interface Test Modes

Output Test Mode Bit Sequence	Pattern Name	Expression	Default
0000	Off (default)	Not applicable	Not applicable
0001	Alternating checker board	0x5555, 0xAAAA, 0x5555, …	Not applicable
0010	1/0 word toggle	0x0000, 0xFFFF, 0x0000, …	Not applicable
0011	31-bit PN sequence	$x^{31} + x^{28} + 1$	0x0003AFFF
0100	23-bit PN sequence	$x^{23} + x^{18} + 1$	0x003AFF
0101	15-bit PN sequence	$x^{15} + x^{14} + 1$	0x03AF
0110	9-bit PN sequence	$x^{9} + x^{5} + 1$	0x092
0111	7-bit PN sequence	$x^{7} + x^{6} + 1$	0x07
1000	Ramp output	$(x) \% 2^{16}$	Ramp size depends on test injection point
1110	Continuous/repeat user test	Register 0x551 to Register 0x558	User Pattern 1 to User Pattern 4, then repeat
1111	Single user test	Register 0x551 to Register 0x558	User Pattern 1 to User Pattern 4, then zeros

Table 38. JESD204B Sample Input for M = 2, S = 2, N' = 16 (Register 0x0573[5:4] = 'b00)

Frame Number	Converter Number	Sample Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0	0	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	0	1	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	1	0	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	1	1	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
1	0	0	0xAAAA	0xFFFF	$(x +1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	0	1	0xAAAA	0xFFFF	$(x +1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	1	0	0xAAAA	0xFFFF	$(x +1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	1	1	0xAAAA	0xFFFF	$(x +1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
2	0	0	0x5555	0x0000	$(x +2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	0	1	0x5555	0x0000	$(x +2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	1	0	0x5555	0x0000	$(x +2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	1	1	0x5555	0x0000	$(x +2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
3	0	0	0xAAAA	0xFFFF	$(x +3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	0	1	0xAAAA	0xFFFF	$(x +3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	1	0	0xAAAA	0xFFFF	$(x +3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	1	1	0xAAAA	0xFFFF	$(x +3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
4	0	0	0x5555	0x0000	$(x +4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	0	1	0x5555	0x0000	$(x +4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000

Frame Number	Converter Number	Sample Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
4	1	0	0x5555	0x0000	$(x+4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	1	1	0x5555	0x0000	$(x+4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000

Table 39. Physical Layer 10-Bit Input (Register 0x0573, Bits[5:4] = 'b01)

10-Bit Symbol Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0x155	0x000	$(x) \% 2^{10}$	0x125	0x3FD	UP1[15:6]	UP1[15:6]
1	0x2AA	0x3FF	$(x + 1) \% 2^{10}$	0x2FC	0x1C0	UP2[15:6]	UP2[15:6]
2	0x155	0x000	$(x + 2) \% 2^{10}$	0x26A	0x00A	UP3[15:6]	UP3[15:6]
3	0x2AA	0x3FF	$(x + 3) \% 2^{10}$	0x198	0x1B8	UP4[15:6]	UP4[15:6]
4	0x155	0x000	$(x + 4) \% 2^{10}$	0x031	0x028	UP1[15:6]	0x000
5	0x2AA	0x3FF	$(x + 5) \% 2^{10}$	0x251	0x3D7	UP2[15:6]	0x000
6	0x155	0x000	$(x + 6) \% 2^{10}$	0x297	0x0A6	UP3[15:6]	0x000
7	0x2AA	0x3FF	$(x + 7) \% 2^{10}$	0x3D1	0x326	UP4[15:6]	0x000
8	0x155	0x000	$(x + 8) \% 2^{10}$	0x18E	0x10F	UP1[15:6]	0x000
9	0x2AA	0x3FF	$(x + 9) \% 2^{10}$	0x2CB	0x3FD	UP2[15:6]	0x000
10	0x155	0x000	$(x + 10) \% 2^{10}$	0x0F1	0x31E	UP3[15:6]	0x000
11	0x2AA	0x3FF	$(x + 11) \% 2^{10}$	0x3DD	0x008	UP4[15:6]	0x000

Table 40. Scrambler 8-Bit Input (Register 0x0573, Bits[5:4] = 'b10)

8-Bit Octet Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0x55	0x00	$(x) \% 2^{8}$	0x49	0xFF	UP1[15:9]	UP1[15:9]
1	0xAA	0xFF	$(x + 1) \% 2^{8}$	0x6F	0x5C	UP2[15:9]	UP2[15:9]
2	0x55	0x00	$(x + 2) \% 2^{8}$	0xC9	0x00	UP3[15:9]	UP3[15:9]
3	0xAA	0xFF	$(x + 3) \% 2^{8}$	0xA9	0x29	UP4[15:9]	UP4[15:9]
4	0x55	0x00	$(x + 4) \% 2^{8}$	0x98	0xB8	UP1[15:9]	0x00
5	0xAA	0xFF	$(x + 5) \% 2^{8}$	0x0C	0x0A	UP2[15:9]	0x00
6	0x55	0x00	$(x + 6) \% 2^{8}$	0x65	0x3D	UP3[15:9]	0x00
7	0xAA	0xFF	$(x + 7) \% 2^{8}$	0x1A	0x72	UP4[15:9]	0x00
8	0x55	0x00	$(x + 8) \% 2^{8}$	0x5F	0x9B	UP1[15:9]	0x00
9	0xAA	0xFF	$(x + 9) \% 2^{8}$	0xD1	0x26	UP2[15:9]	0x00
10	0x55	0x00	$(x + 10) \% 2^{8}$	0x63	0x43	UP3[15:9]	0x00
11	0xAA	0xFF	$(x + 11) \% 2^{8}$	0xAC	0xFF	UP4[15:9]	0x00

Data Link Layer Test Modes

The data link layer test modes are implemented in the CLM9680BCPZ as defined by Section 5.3.3.8.2 in the JEDEC JESD204B specification. These tests are shown in Register 0x574 Bits[2:0].

Test patterns inserted at this point are useful for verifying the functionality of the data link layer. When the data link layer test modes are enabled, disable SYNCINB± by writing 0xC0 to Register 0x0572.

SERIAL PORT INTERFACE

The CLM9680BCPZ SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the Serial Control Interface Standard (Rev. 1.0).

CONFIGURATION USING THE SPI

Three pins define the SPI of the CLM9680BCPZ ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 37). The SCLK (serial clock) pin is used to synchronize the read and write data presented from/to the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 37. Serial Port Interface Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input that is used to synchronize serial interface, reads, and writes.
SDIO	Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active low control that gates the read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 4 and Table 5.

Other modes involving the CSB pin are available. The CSB pin can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB can stall high between bytes to allow additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued, which allows the SDIO pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the Serial Control Interface Standard (Rev. 1.0).

HARDWARE INTERFACE

The pins described in Table 37 comprise the physical interface between the user programming device and the serial port of the CLM9680BCPZ. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, Microcontroller-Based Serial Port Interface (SPI) Boot Circuit. Do not activate the SPI port during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the CLM9680BCPZ to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI ACCESSIBLE FEATURES

Table 38 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the Serial Control Interface Standard (Rev. 1.0). The CLM9680BCPZ device-specific features are described in the Memory Map section.

Table 38. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode.
Clock	Allows the user to access the clock divider via the SPI.
DDC	Allows the user to set up decimation filters for different applications.
Test Input/Output	Allows the user to set test modes to have known data on output bits.
Output Mode	Allows the user to set up outputs.
SERDES Output Setup	Allows the user to vary SERDES settings such as swing and emphasis.

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is divided into four sections: the Chiplon Devices SPI registers (Register 0x000 to Register 0x00D), the Chiplon input buffer control registers, the ADC function registers, the DDC function registers, and the digital outputs and test modes registers.

Table 39 (see the Memory Map Register Table section) documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x561, the output mode register, has a hexadecimal default value of 0x01, which means that Bit 0 = 1, and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on this function and others, see Table 39.

Open and Reserved Locations

All address and bit locations that are not included in Table 39 are not currently supported for this device. Write unused bits of a valid address location with 0s unless the default value is set otherwise. Writing to these locations is required only when part of an address location is unassigned (for example, Address 0x561). If the entire address location is open (for example, Address 0x13), do not write to this address location.

Default Values

After the CLM9680BCPZ is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table 39.

Logic Levels

An explanation of logic level terminology follows:

- “Bit is set” is synonymous with “bit is set to Logic 1” or “writing Logic 1 for the bit.”
- “Clear a bit” is synonymous with “bit is set to Logic 0” or “writing Logic 0 for the bit.”
- X denotes a don’t care bit.

Channel-Specific Registers

Some channel setup functions, such as the input termination (Register 0x016), can be programmed to a different value for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 39 as local. These local registers and bits can be accessed by setting the appropriate Channel A or Channel B bits in Register 0x008. If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, set only Channel A or Channel B to read one of the two registers. If both bits are set during an SPI read cycle, the device returns the value for Channel A. Registers and bits designated as global in Table 39 affect the entire device and the channel features for which independent settings are not allowed between channels. The settings in Register 0x005 do not affect the global registers and bits.

SPI Soft Reset

After issuing a soft reset by programming 0x81 to Register 0x000, the CLM9680BCPZ requires 5 ms to recover. When programming the CLM9680BCPZ for application setup, ensure that an adequate delay is programmed into the firmware after asserting the soft reset and before starting the device setup.

MEMORY MAP REGISTER TABLE

All address locations that are not included in Table 39 are not currently supported for this device and must not be written.

Table 39. Memory Map Registers

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
Chiplon Devices SPI Registers											
0x000	INTERFACE_ CONFIG_A	Soft reset (self clearing)	LSB first 0 = MSB 1 = LSB	Address ascension	0	0	Address ascension	LSB first 0 = MSB 1 = LSB	Soft reset (self clearing)	0x00	
0x001	INTERFACE_ CONFIG_B	Single instruction	0	0	0	0	0	Datapath soft reset (self clearing)	0	0x00	
0x002	DEVICE_ CONFIG (local)	0	0	0	0	0	0	00 = normal operation 10 = standby 11 = power-down		0x00	
0x003	CHIP_TYPE					011 = high speed ADC				0x03	Read only
0x004	CHIP_ID (low byte)	1	1	0	0	0	1	0	1	0xC5	Read only
0x005	CHIP_ID (high byte)	0	0	0	0	0	0	0	0	0x00	Read only
0x006	CHIP_ GRADE	1100 = 1250 MSPS 1010 = 1000 MSPS 1000 = 820 MSPS 0101 = 500 MSPS				X	X	X	X		Read only
0x008	Device index	0	0	0	0	0	0	Channel B	Channel A	0x0	
0x00A	Scratch pad	0	0	0	0	0	0	0	0	0x00	
0x00B	SPI revision	0	0	0	0	0	0	0	1	0x01	
0x00C	Vendor ID (low byte)	0	1	0	1	0	1	1	0	0x56	Read only
0x00D	Vendor ID (high byte)	0	0	0	0	0	1	0	0	0x04	Read only
Chiplon Input Buffer Control Registers											
0x015	Chiplon input (local)	0	0	0	0	0	0	0	Input disable 0 = normal operation 1 = input disabled	0x00	
0x016	Input termination (local)	Chiplon input differential termination 0000 = 400 Ω (default) 0001 = 200 Ω 0010 = 100 Ω 0110 = 50 Ω				1110 = CLM9680BCPZ-1250 and CLM9680BCPZ-1000 1100 = CLM9680BCPZ-820 and CLM9680BCPZ-500				0x0E for CLM9680 BCPZ-1250 and CLM9680 BCPZ-1000; 0x0C for CLM9680 BCPZ-820 and CLM968 0BCPZ-500	
0x934	Input capacitance (local)	0	0	0	0x1F = 3 pF to GND (default) 0x00 = 1.5 pF to GND					0x1F	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x018	Buffer Control 1 (local)	0000 = 1.0× buffer current 0001 = 1.5× buffer current 0010 = 2.0× buffer current (default for CLM9680BCPZ-500) 0011 = 2.5× buffer current 0100 = 3.0× buffer current (default for CLM9680BCPZ-1000 and CLM9680BCPZ-820) 0101 = 3.5× buffer current (default for CLM9680BCPZ-1250) … 1111 = 8.5× buffer current				0	0	0	0	0x50 for CLM9680BCPZ- 1250; 0x40 for CLM9680BCPZ- 1000 and CLM9680BCPZ- 820; 0x20 for CLM9680BCPZ- 500	
0x019	Buffer Control 2 (local)	0100 = Setting 1 (default for CLM9680BCPZ-820) 0101 = Setting 2 (default for CLM9680BCPZ-1250 and CLM9680BCPZ-1000) 0110 = Setting 3 (default for CLM9680BCPZ-500) 0111 = Setting 4				0	0	0	0	0x50 for CLM9680BCPZ-1250 and CLM9680BCPZ-1000; 0x40 for CLM9680BCPZ-820; 0x60 for CLM9680BCPZ- 500	
0x01A	Buffer Control 3 (local)	0	0	0	0	1000 = Setting 1 1001 = Setting 2 (default for CLM9680BCPZ-1250, CLM9680BCPZ-1000 and CLM9680BCPZ-820) 1010 = Setting 3 (default for CLM9680BCPZ-500)				0x09 for CLM9680BCPZ- 1250, CLM9680BCPZ- 1000 and CLM9680BCPZ- 820; 0x0A for CLM9680BCPZ- 500	
0x11A	Buffer Control 4 (local)	0	0	High frequency setting 0 = off (default) 1 = on	0	0	0	0	0		
0x935	Buffer Control 5 (local)	0	0	0	0	0	Low frequency operation 0 = off 1 = on (default)	0	0		
0x025	Input full-scale range (local)	0	0	0	0	Full-scale adjust 0000 = 1.94 V 1000 = 1.46 V 1001 = 1.58 V (default for CLM9680BCPZ-1250) 1010 = 1.70 V (default for CLM9680BCPZ-1000 and CLM9680BCPZ-820) 1011 = 1.82 V 1100 = 2.06 V (default for CLM9680BCPZ-500)				0x09 for CLM9680BCPZ- 1250; 0x0A for CLM9680BCPZ- 1000 and CLM9680BCPZ- 820; 0x0C for CLM9680BCPZ- 500	V p-p differ-ential; use in conjunc-tion with Reg. 0x030

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x030	Input full-scale control (local)	0	0	0	Full-scale control See Table 10 for recommended settings for different frequency bands; default values: CLM9680BCPZ-1250, CLM9680BCPZ-1000 = 110 CLM9680BCPZ-820 = 101 CLM9680BCPZ-500 = 001 CLM9680BCPZ-500 = 110 (for <1.82 V)			0	0		Used in conjunction with Reg. 0x025
ADC Function Registers											
0x024	V_1P0 control	0	0	0	0	0	0	0	1.0V reference select 0 = internal 1 = external	0x00	
0x028	Temperature diode	0	0	0	0	0	0	0	Diode selection 0 = no diode selected 1 = temperature diode selected	0x00	Used in conjunction with Reg. 0x040
0x03F	PDWN/ STBY pin control (local)	0 = PDWN/ STBY enabled 1 = disabled	0	0	0	0	0	0	0	0x00	Used in conjunction with Reg. 0x040
0x040	Chip pin control	PDWN/STBY function 00 = power down 01 = standby 10 = disabled		Fast Detect B (FD_B) 000 = Fast Detect B output 001 = JESD204B LMFC output 010 = JESD204B internal SYNC~ output 111 = disabled			Fast Detect A (FD_A) 000 = Fast Detect A output 001 = JESD204B LMFC output 010 = JESD204B internal SYNC~ output 011 = temperature diode 111 = disabled			0x3F	
0x10B	Clock divider	0	0	0	0	0	000 = divide by 1 001 = divide by 2 011 = divide by 4 111 = divide by 8			0x00	
0x10C	Clock divider phase (local)	0	0	0	0	Independently controls Channel A and Channel B clock divider phase offset 0000 = 0 input clock cycles delayed 0001 = ½ input clock cycles delayed 0010 = 1 input clock cycles delayed 0011 = 1½ input clock cycles delayed 0100 = 2 input clock cycles delayed 0101 = 2½ input clock cycles delayed … 1111 = 7½ input clock cycles delayed				0x00	
0x10D	Clock divider and SYSREF control	Clock divider auto phase adjust 0 = disabled 1 = enabled	0	0	0	Clock divider negative skew window 00 = no negative skew 01 = 1 device clock of negative skew 10 = 2 device clocks of negative skew 11 = 3 device clocks of negative skew		Clock divider positive skew window 00 = no positive skew 01 = 1 device clock of positive skew 10 = 2 device clocks of positive skew 11 = 3 device clocks of positive skew		0x00	Clock divider must be >1

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x117	Clock delay control	0	0	0	0	0	0	0	Clock fine delay adjust enable 0 = disabled 1 = enabled	0x00	Enabling the clock fine delay adjust causes a datapath reset
0x118	Clock fine delay (local)	Clock Fine Delay Adjust[7:0], twos complement coded control to adjust the fine sample clock skew in ~1.7 ps steps ≤ −88 = −151.7 ps skew −87 = −150 ps skew … 0 = 0 ps skew … ≥ +87 = +150 ps skew								0x00	Used in con-junction with Reg. 0x0117
0x11C	Clock status	0	0	0	0	0	0	0	0 = no input clock detected 1 = input clock detected	Read only	
0x120	SYSREF± Control 1	0	SYSREF± flag reset 0 = normal opera-tion 1 = flags held in reset	0	SYSREF± transition select 0 = low to high 1 = high to low	CLK± edge select 0 = rising 1 = falling	SYSREF± mode select 00 = disabled 01 = continuous 10 = N shot		0	0x00	
0x121	SYSREF± Control 2	0	0	0	0	SYSREF N-shot ignore counter select 0000 = next SYSREF± only 0001 = ignore the first SYSREF± transition 0010 = ignore the first two SYSREF± transitions … 1111 = ignore the first 16 SYSREF± transitions				0x00	Mode select (Reg 0x120, Bits [2:1]) must be N-shot
0x123	SYSREF± timestamp delay control		SYSREF± timestamp delay, Bits[6:0] 0x00 = no delay 0x01 = 1 clock delay … 0x7F = 127 clocks delay							0x00	Ignored when Reg. 0x01FF = 0x00
0x128	SYSREF± Status 1	SYSREF± hold status, Register 0x128[7:4] (see the SYSREF± Setup/Hold Window Monitor section)				SYSREF± setup status, Register 0x128[3:0] (see the SYSREF± Setup/Hold Window Monitor section)				Read only	
0x129	SYSREF±and clock divider status	0	0	0	0	Clock divider phase when SYSREF± was captured 0000 = in-phase 0001 = SYSREF± is ½ cycle delayed from clock 0010 = SYSREF± is 1 cycle delayed from clock 0011 = 1½ input clock cycles delayed 0100 = 2 input clock cycles delayed 0101 = 2½ input clock cycles delayed … 1111 = 7½ input clock cycles delayed				Read only	
0x12A	SYSREF± counter	SYSREF counter, Bits[7:0] increments when a SYSREF± is captured								Read only	
0x1FF	Chip sync mode							Synchronization mode 00 = normal 01 = timestamp		0x00	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x200	Chip application mode	0	0	Chip Q ignore 0 = normal (I/Q) 1 = ignore (I only)	0	0	0	Chip operating mode 00 = full bandwidth mode 01 = DDC 0 on 10 = DDC 0 and DDC 1 on 11 = DDC 0, DDC 1, DDC 2, and DDC 3 on		0x00	
0x201	Chip decimation ratio	0	0	0	0	0	Chip decimation ratio select 000 = full sample rate (decimate = 1) 001 = decimate by 2 010 = decimate by 4 011 = decimate by 8 100 = decimate by 16			0x00	
0x228	Customer offset	Offset adjust in LSBs from +127 to −128 (twos complement format)								0x00	
0x245	Fast detect (FD) control (local)	0	0	0	0	Force FD_A/ FD_B pins; 0 = normal function; 1 = force to value	Force value of FD_A/FD_B pins if force pins is true, this value is output on FD pins	0	Enable fast detect output	0x00	
0x247	FD upper threshold LSB (local)	Fast detect upper threshold, Bits[7:0]								0x00	
0x248	FD upper threshold MSB (local)	0	0	0	Fast detect upper threshold, Bits[12:8]					0x00	
0x249	FD lower threshold LSB (local)	Fast detect lower threshold, Bits[7:0]								0x00	
0x24A	FD lower threshold MSB (local)	0	0	0	Fast detect lower threshold, Bits[12:8]					0x00	
0x24B	FD dwell time LSB (local)	Fast detect dwell time, Bits[7:0]								0x00	
0x24C	FD dwell time MSB (local)	Fast detect dwell time, Bits[15:8]								0x00	
0x26F	Signal monitor synchronization control	0	0	0	0	0	0	Synchronization mode 00 = disabled 01 = continuous 11 = one shot		0x00	Refer to the Signal Monitor section
0x270	Signal monitor control (local)	0	0	0	0	0	0	Peak detector 0 = disabled 1 = enabled	0	0x00	
0x271	Signal Monitor Period Register 0 (local)	Signal monitor period, Bits[7:0]								0x80	Indecimated output clock cycles
0x272	Signal Monitor Period Register 1 (local)	Signal monitor period, Bits[15:8]								0x00	Indecimated output clock cycles

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x273	Signal Monitor Period Register2 (local)	Signal monitor period, Bits[23:16]								0x00	Indeci- mated output clock cycles
0x274	Signal monitor result control (local)	0	0	0	Result update 1 = update results (self clear)	0	0	0	Result selection 0 = reserved 1 = peak detector	0x01	
0x275	Signal Monitor Result Register 0 (local)	Signal monitor result, Bits[7:0] When Register 0x0274[0] = 1, Result Bits[19:7] = Peak Detector Absolute Value[12:0]; Result Bits[6:0] = 0								Read only	Updated based on Reg. 0x274[4]
0x276	Signal Monitor Result Register 1 (local)	Signal monitor result, Bits[15:8]								Read only	Updated based on Reg. 0x274[4]
0x277	Signal Monitor Result Register 1 (local)	0	0	0	0	Signal monitor result, Bits[19:16]				Read only	Updated based on Reg. 0x274[4]
0x278	Signal monitor period counter result (local)	Period count result, Bits[7:0]								Read only	Updated based on Reg. 0x274[4]
0x279	Signal monitor SPORT over JESD204B control (local)	0	0	0	0	0	0	00 = disabled 11 = enable		0x00	
0x27A	SPORT over JESD204B input selection (local)	0	0	0	0	0	0	Peak detector 0 = disabled 1 = enabled	0	0x00	
DDC Function Registers (See the Digital Downconverter (DDC) Section)											
0x300	DDC synchro- n	0	0	0	DDC NCO soft reset 0 = normal operation 1 = reset	0	0	Synchronization mode (triggered by SYSREF±) 00 = disabled 01 = continuous 11 = one shot			
0x310	DDC0 control	Mixer select 0 = real mixer 1 = complex	Gain select 0 = 0 dB gain 1 = 6 dB ga	IF (intermediate frequency) mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = f_S/4 Hz IF mode (f_S/4 downmixing mode) 11 = test mode (mixer inputs forced to +f_S, NCO enabled)		Complex to 0 = disabled 1 = enabled	0	Decimation rate select (complex to real disabled) 11 = decimate by 2 00 = decimate by 4 01 = decimate by 8 10 = decimate by 16 (complex to real enabled) 11 = decimate by 1 00 = decimate by 2 01 = decimate by 4 10 = decimate by 8		0x00	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x311	DDC 0 input selection	0	0	0	0	0	Q input select 0 = Ch A 1 = Ch B	0	I input select 0 = Ch A 1 = Ch B	0x00	Refer to the DDC section
0x314	DDC 0 frequency LSB	DDC 0 NCO frequency value, Bits[7:0] twos complement								0x00	
0x315	DDC 0 frequency MSB	X	X	X	X	DDC 0 NCO frequency value, Bits[11:8] twos complement				0x00	
0x320	DDC 0 phase LSB	DDC 0 NCO phase value, Bits[7:0] twos complement								0x00	
0x321	DDC 0 phase MSB	X	X	X	X	DDC 0 NCO phase value, Bits[11:8] twos complement				0x00	
0x327	DDC 0 output test mode selection	0	0	0	0	0	Q output test mode enable 0 = disabled 1 = enabled from Channel B	0	I output test mode enable 0 = disabled 1 = enabled from Channel A	0x00	Refer to the DDC section
0x330	DDC 1 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF (intermediate frequency) mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = $f_{ADC}/4$ Hz IF mode ($f_{ADC}/4$ downmixing mode) 11 = test mode (mixer inputs forced to $+f_S$, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation rate select (complex to real disabled) 11 = decimate by 2 00 = decimate by 4 01 = decimate by 8 10 = decimate by 16 (complex to real enabled) 11 = decimate by 1 00 = decimate by 2 01 = decimate by 4 10 = decimate by 8		0x00	
0x331	DDC 1 input selection	0	0	0	0	0	Q input select 0 = Ch A 1 = Ch B	0	I input select 0 = Ch A 1 = Ch B	0x05	Refer to the DDC section
0x334	DDC 1 frequency LSB	DDC 1 NCO frequency value, Bits[7:0] twos complement								0x00	
0x335	DDC 1 frequency MSB	X	X	X	X	DDC 1 NCO frequency value, Bits[11:8] twos complement				0x00	
0x340	DDC 1 phase LSB	DDC 1 NCO phase value, Bits[7:0] twos complement								0x00	
0x341	DDC 1 phase MSB	X	X	X	X	DDC 1 NCO phase value, Bits[11:8] twos complement				0x00	
0x347	DDC 1 output test mode selection	0	0	0	0	0	Q output test mode enable 0 = disabled 1 = enabled from Ch B	0	I output test mode enable 0 = disabled 1 = enabled from Ch A	0x00	Refer to the DDC section

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x350	DDC2 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = $f_{ADC}/4$ Hz IF mode ($f_{ADC}/4$ downmixing mode) 11 = test mode (mixer inputs forced to $+f_S$, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation rate select (complex to real disabled) 11 = decimate by 2 00 = decimate by 4 01 = decimate by 8 10 = decimate by 16 (complex to real enabled) 11 = decimate by 1 00 = decimate by 2 01 = decimate by 4 10 = decimate by 8		0x00	
0x351	DDC 2 input selection	0	0	0	0	0	Q input select 0 = Ch A 1 = Ch B	0	I input select 0 = Ch A 1 = Ch B	0x00	Refer to the DDC section
0x354	DDC2 frequency LSB	DDC 2 NCO frequency value, Bits[7:0] twos complement								0x00	
0x355	DDC2 frequency MSB	X	X	X	X	DDC 2 NCO frequency value, Bits[11:8] twos complement				0x00	
0x360	DDC 2 phase LSB	DDC 2 NCO phase value, Bits[7:0] twos complement								0x00	
0x361	DDC 2 phase MSB	X	X	X	X	DDC 2 NCO phase value, Bits[11:8] twos complement				0x00	
0x367	DDC2 output test mode selection	0	0	0	0	0	Q output test mode enable 0 = disabled 1 = enabled from Ch B	0	I output test mode enable 0 = disabled 1 = enabled from Ch A	0x00	Refer to the DDC section
0x370	DDC3 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 db gain 1 = 6 db gain	IF mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode(mixer bypassed, NCO disabled) 10 = $f_{ADC}/4$ Hz IF mode ($f_{ADC}/4$ downmixing mode) 11 = test mode (mixer inputs forced to $+f_S$, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation rate select (complex to real disabled) 11 = decimate by 2 00 = decimate by 4 01 = decimate by 8 10 = decimate by 16 (complex to real enabled) 11 = decimate by 1 00 = decimate by 2 01 = decimate by 4 10 = decimate by 8		0x00	
0x371	DDC 3 input selection	0	0	0	0	0	Q input select 0 = Ch A 1 = Ch B	0	I input select 0 = Ch A 1 = Ch B	0x05	Refer to the DDC section
0x374	DDC3 frequency LSB	DDC 3 NCO frequency value, Bits[7:0] twos complement								0x00	
0x375	DDC3 frequency MSB	X	X	X	X	DDC 3 NCO frequency value, Bits[11:8] twos complement				0x00	
0x380	DDC3 phase LSB	DDC 3 NCO phase value, Bits[7:0] twos complement								0x00	
0x381	DDC 3 phase MSB	X	X	X	X	DDC 3 NCO phase value, Bits[11:8] twos complement				0x00	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x387	DDC 3 output test mode selection	0	0	0	0	0	0	0	I output test mode enable 0 = disabled 1 = enabled from Ch A	0x00	Refer to the DDC section
Digital Outputs and Test Modes											
0x550	ADC test modes (local)	User pattern selection 0 = conti-nuous repeat 1 = single pattern	0	Reset PN long gen 0 = long PN enable 1 = long PN reset	Reset PN short gen 0 = short PN enable 1 = short PN reset	Test mode selection 0000 = off, normal operation 0001 = midscale short 0010 = positive full scale 0011 = negative full scale 0100 = alternating checker board 0101 = PN sequence, long 0110 = PN sequence, short 0111 = 1/0 word toggle 1000 = the user pattern test mode (used with Register 0x0550, Bit 7 and User Pattern 1 to User Pattern 4 registers) 1111 = ramp output				0x00	
0x551	User Pattern 1 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x552	User Pattern 1 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x553	User Pattern 2 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x554	User Pattern 2 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x555	User Pattern 3 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x556	User Pattern 3 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x557	User Pattern 4 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x558	User Pattern 4 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x559	Output Mode Control 1	0	Converter Control Bit 1 selection 000 = tie low (1'b0) 001 = overrange bit 011 = fast detect (FD) bit 101 = SYSREF± Only used when CS (Register 0x58F) = 2 or 3			0	Converter Control Bit 0 selection 000 = tie low (1'b0) 001 = overrange bit 011 = fast detect (FD) bit 101 = SYSREF± Only used when CS (Register 0x58F) = 3			0x00	
0x55A	Output Mode Control 2	0	0	0	0	0	Converter Control Bit 2 selection 000 = tie low (1'b0) 001 = overrange bit 011 = fast detect (FD) bit 101 = SYSREF Used when CS (Register 0x58F) = 1, 2, or 3			0x01	
0x561	Output mode	0	0	0	0	0	Sample invert 0 = normal 1 = sample invert	Data format select 00 = offset binary 01 = twos complement		0x01	
0x562	Output overrange (OR) clear	Virtual Converter 7 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 6 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 5 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 4 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 3 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 2 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 1 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 0 OR 0 = OR bit enabled 1 = OR bit cleared	0x00	
0x563	Output OR status	Virtual Converter 7 OR 0 = no OR 1 = OR occurred	Virtual Converter 6 OR 0 = no OR 1 = OR occurred	Virtual Converter 5 OR 0 = no OR 1 = OR occurred	Virtual Converter 4 OR 0 = no OR 1 = OR occurred	Virtual Converter 3 OR 0 = no OR 1 = OR occurred	Virtual Converter 2 OR 0 = no OR 1 = OR occurred	Virtual Converter 1 OR 0 = no OR 1 = OR occurred	Virtual Converter 0 OR 0 = no OR 1 = OR occurred	0x00	Read only
0x564	Output channel select	0	0	0	0	0	0	0	Converter channel swap 0 = normal channel ordering 1 = channel swap enabled	0x00	
0x56E	JESD204B lane rate control	0	0	0	0 = serial lane rate ≥6.25 Gbps and ≤12.5 Gbps 1 = serial lane rate must be ≥ 3.125 Gbps and ≤6.25 Gbps	0	0	0	0	0x00 for CLM9680 BCPZ-1250, CLM9680 BCPZ-1000 and CLM9680 BCPZ-820; 0x10 for CLM968 0BCPZ-500	
0x56F	JESD204B PLL lock status	PLL lock 0 = not locked 1 = locked	0	0	0	0	0	0	0	0x00	Read only

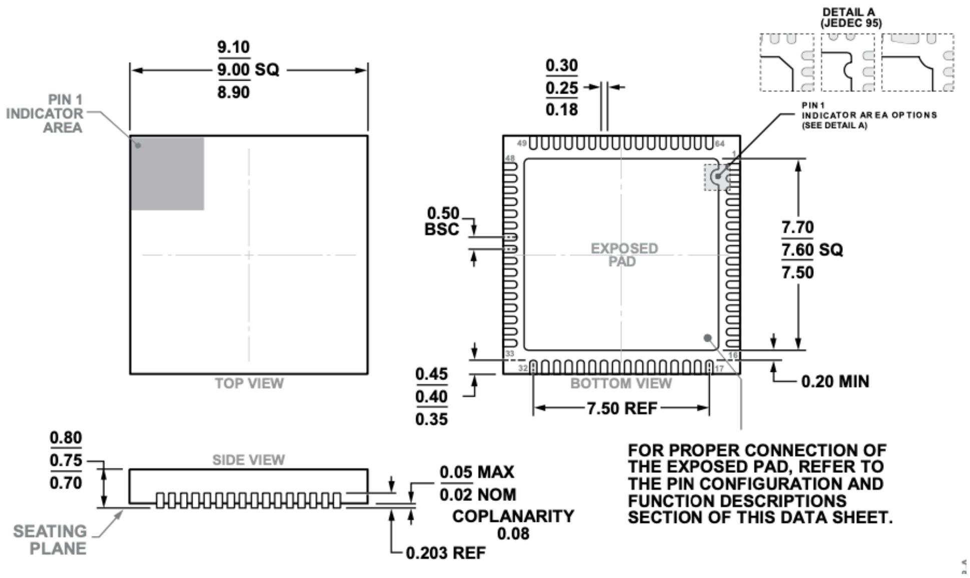
Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x570	JESD204B quick config-uration	JESD204B quick configuration L = number of lanes = $2_{\text{Register 0x570, Bits[7:6]}}$ M = number of converters = $2_{\text{Register 0x570, Bits[5:3]}}$ F = number of octets/frame = $2_{\text{Register 0x570, Bits[2:0]}}$								0x88 for CLM9680 BCPZ-1250, CLM9680 BCPZ-1000 and CLM9680 BCPZ-820; 0x49 for CLM9680BCPZ-500	Refer to Table 26 and Table 27
0x571	JESD204B Link Mode Control 1	Standby mode 0 = all converter outputs 0 1 = CGS (/K28.5/)	Tail bit (t) PN 0 = disable 1 = enable T = N´ − N − CS	Long transport layer test 0 = disable 1 = enable	Lane synch-ronization 0 = disable FACI uses / K28.7/ 1 = enable FACI uses / K28.3/ and /K28.7/	ILAS sequence mode 00 = ILAS disabled 01 = ILAS enabled 11 = ILAS always on test mode		FACI 0 = enabled 1 = disabled	Link control 0 = active 1 = power down	0x14	
0x572	JESD204B Link Mode Control 2	SYNCINB± pin control 00 = normal 10 = ignore SYNCINB± (force CGS) 11 = ignore SYNCINB± (force ILAS/user data)		SYNCINB± pin invert 0 = active low 1 = active high	SYNCINB± pin type 0 = differential 1 = CMOS	0	8-bit/10-bit bypass 0 = normal 1 = bypass	8-/10-bit bit invert 0 = normal 1 = invert the abcd efghij symbols	0	0x00	
0x573	JESD204B Link Mode Control 3	CHKSUM mode 00 = sum of all 8-bit link config registers 01 = sum of individual link config fields 10 = checksum set to zero		Test injection point 00 = N´ sample input 01 = 10-bit data at 8-bit/10-bit output (for PHY testing) 10 = 8-bit data at scrambler input		JESD204B test mode patterns 0000 = normal operation (test mode disabled) 0001 = alternating checker board 0010 = 1/0 word toggle 0011 = 31-bit PN sequence—$X_{31} + X_{28} + 1$ 0100 = 23-bit PN sequence—$X_{23} + X_{18} + 1$ 0101 = 15-bit PN sequence—$X_{15} + X_{14} + 1$ 0110 = 9-bit PN sequence—$X_9 + X_5 + 1$ 0111 = 7-bit PN sequence—$X_7 + X_6 + 1$ 1000 = ramp output 1110 = continuous/repeat user test 1111 = single user test				0x00	
0x574	JESD204B Link Mode Control 4	ILAS delay 0000 = transmit ILAS on first LMFC after SYNCINB± deasserted 0001 = transmit ILAS on second LMFC after SYNCINB± deasserted … 1111 = transmit ILAS on 16th LMFC after SYNCINB± deasserted				0	Link layer test mode 000 = normal operation (link layer test mode disabled) 001 = continuous sequence of /D21.5/ characters 100 = modified RPAT test sequence 101 = JSPAT test sequence 110 = JTSPAT test sequence			0x00	
0x578	JESD204B LMFC offset	0	0	0	LMFC phase offset value[4:0]					0x00	
0x580	JESD204B DID config	JESD204B Tx DID value[7:0]								0x00	
0x581	JESD204B BID config	0	0	0	0	JESD204B Tx BID value, Bits[3:0]				0x00	
0x583	JESD204B LID Config 1	0	0	0	Lane 0 LID value, Bits[4:0]					0x00	
0x584	JESD204B LID Config 2	0	0	0	Lane 1 LID value, Bits[4:0]					0x01	
0x585	JESD204B LID Config 3	0	0	0	Lane 2 LID value, Bits[4:0]					0x01	
0x586	JESD204B LID Config 4	0	0	0	Lane 3 LID value, Bits[4:0]					0x03	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x58B	JESD204B parameters SCR/L	JESD204B scrambling (SCR) 0 = disabled 1 = enabled	0	0	0	0	0	JESD204B lanes (L) 00 = 1 lane 01 = 2 lanes 11 = 4 lanes Read only, see Register 0x570		0x8X	
0x58C	JESD204BF config	Number of octets per frame, F = Register 0x58C[7:0] + 1								0x88	Read only, see Reg. 0x570
0x58D	JESD204BK config	0	0	0	Number of frames per multiframe, K = Register 0x58D[4:0] + 1 Only values where (F × K) mod 4 = 0 are supported					0x1F	See Reg. 0x570
0x58E	JESD204BM config	Number of Converters per Link[7:0] 0x00 = link connected to one virtual converter (M = 1) 0x01 = link connected to two virtual converters (M = 2) 0x03 = link connected to four virtual converters (M = 4) 0x07 = link connected to eight virtual converters (M = 8)									Read only
0x58F	JESD204B CS/N config	Number of control bits (CS) per sample 00 = no control bits (CS = 0) 01 = 1 control bit (CS = 1); Control Bit 2 only 10 = 2 control bits (CS = 2); Control Bit 2 and 1 only 11 = 3 control bits (CS = 3); all control bits (2, 1, 0)		0	ADC converter resolution (N) 0x06 = 7-bit resolution 0x07 = 8-bit resolution 0x08 = 9-bit resolution 0x09 = 10-bit resolution 0x0A = 11-bit resolution 0x0B = 12-bit resolution 0x0C = 13-bit resolution 0x0D = 14-bit resolution 0x0E = 15-bit resolution 0x0F = 16-bit resolution					0x0F	
0x590	JESD204BN' config	0	0	Subclass support (Subclass V) 0 = Subclass 0 (no deter-ministic latency) 1 = Subclass 1	ADC number of bits per sample (N') 0x7 = 8 bits 0xF = 16 bits					0x2F	
0x591	JESD204BS config	0	0	1	Samples per converter frame cycle (S) S value = Register 0x591[4:0] + 1					0x20	Read only
0x592	JESD204BHD and CF config	HD value 0 = disabled 1 = enabled	0	0	Control words per frame clock cycle per link (CF) CF value = Register 0x592, Bits[4:0]					0x80	Read only
0x5A0	JESD204B CHKSUM0	CHKSUM value for SERDOUT0±, Bits[7:0]								0x81	Read only
0x5A1	JESD204B CHKSUM1	CHKSUM value for SERDOUT1±, Bits[7:0]								0x82	Read only
0x5A2	JESD204B CHKSUM2	CHKSUM value for SERDOUT2±, Bits[7:0]								0x82	Read only
0x5A3	JESD204B CHKSUM3	CHKSUM value for SERDOUT3±, Bits[7:0]								0x84	Read only
0x5B0	JESD204B lane power-down	1	SERD-OUT3± 0 = on 1 = off	1	SERD-OUT2± 0 = on 1 = off	1	SERD-OUT1± 0 = on 1 = off	1	SERD-OUT0± 0 = on 1 = off	0xAA	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x5B2	JESD204B lane SERDOUT0± assign	X	X	X	X	0	SERDOUT0± lane assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3			0x00	
0x5B3	JESD204B lane SERDOUT1± assign	X	X	X	X	0	SERDOUT1± lane assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3			0x11	
0x5B5	JESD204B lane SERDOUT2± assign	X	X	X	X	0	SERDOUT2± lane assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3			0x22	
0x5B6	JESD204B lane SERDOUT3± assign	X	X	X	X	0	SERDOUT3± lane assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3			0x33	
0x5BF	JESD serializer drive adjust	0	0	0	0	Swing voltage 0000 = 237.5 mV 0001 = 250 mV 0010 = 262.5 mV 0011 = 275 mV 0100 = 287.5 mV 0101 = 300 mV (default) 0110 = 312.5 mV 0111 = 325 mV 1000 = 337.5 mV 1001 = 350 mV 1010 = 362.5 mV 1011 = 375 mV 1100 = 387.5 mV 1101 = 400 mV 1110 = 412.5 mV 1111 = 425 mV				0x05	
0x5C1	De-emphasis select	0	SERD-OUT3± 0 = disable 1 = enable	0	SERD-OUT2± 0 = disable 1 = enable	0	SERDOUT1± 0 = disable 1 = enable	0	SERD-OUT0± 0 = disable 1 = enable	0x00	
0x5C2	De-emphasis setting for SERDOUT0±	0	0	0	0	SERDOUT0± de-emphasis settings 0000 = 0 dB 0001 = 0.3 dB 0010 = 0.8 dB 0011 = 1.4 dB 0100 = 2.2 dB 0101 = 3.0 dB 0110 = 4.0 dB 0111 = 5.0 dB				0x00	
0x5C3	De-emphasis setting for SERDOUT1±	0	0	0	0	SERDOUT1± de-emphasis settings 0000 = 0 dB 0001 = 0.3 dB 0010 = 0.8 dB 0011 = 1.4 dB 0100 = 2.2 dB 0101 = 3.0 dB 0110 = 4.0 dB 0111 = 5.0 dB				0x00	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x5C4	De-emphasis setting for SERDOUT2±	0	0	0	0	SERDOUT2± de-emphasis settings 0000 = 0 dB 0001 = 0.3 dB 0010 = 0.8 dB 0011 = 1.4 dB 0100 = 2.2 dB 0101 = 3.0 dB 0110 = 4.0 dB 0111 = 5.0 dB				0x00	
0x5C5	De-emphasis setting for SERDOUT3±	0	0	0	0	SERDOUT3± de-emphasis settings 0000 = 0 dB 0001 = 0.3 dB 0010 = 0.8 dB 0011 = 1.4 dB 0100 = 2.2 dB 0101 = 3.0 dB 0110 = 4.0 dB 0111 = 5.0 dB				0x00	

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WMMD

Figure 187. 64-Lead Lead Frame Chip Scale Package [LFCSP]
9 mm × 9 mm Body and 0.75 mm Package Height
(CP-64-15)
Dimensions shown in millimeters

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