Quad 3-STATE NOR R/S Latches

Description

The CD4043 is quad cross-couple 3-STATE CMOS NOR latches, has a separate Q output and individual SET and RESET inputs. There is a common 3-STATE ENABLE input for all four latches. A logic " 1" on the ENABLE input connects the latch states to the Q outputs. A logic " 0" on the ENABLE input discon-nects the latch states from the Q outputs resulting in an open circuit condition on the Q output. The 3-STATE fea-ture allows common bussing of the outputs.

Features

Wide supply voltage range: 3V to 15V

Low power: 100 nW (typ.)

High noise immunity: 0.45 V_{DD} (typ.)

Separate SET and RESET inputs for each latch

NOR and NAND configuration

3-STATE output with common output enable

Application

- Multiple bus storage
- Strobed register
- Four bits of independent storage with output enable
- General digital logic

Absolute Maximum Ratings

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

function diagram

Top View
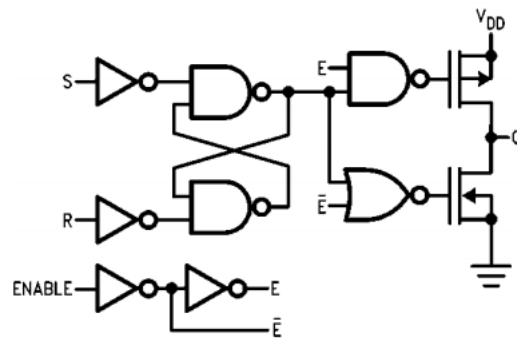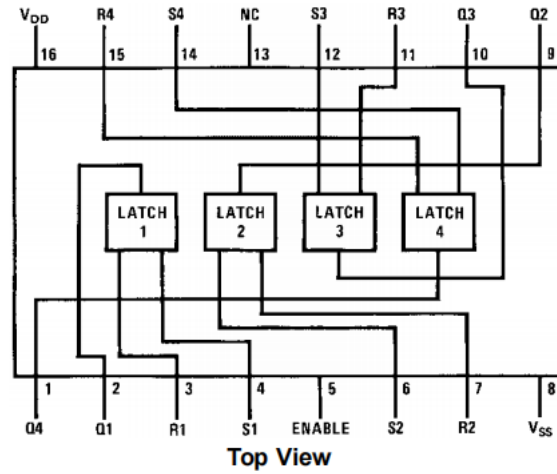
Truth Tables

| S	R	E	Q
X	X	0	OC
0	0	1	NC
1	0	1	1
0	1	1	0
1	1	1	Δ

OC = 3-STATE
NC = No change
X = Don't care
Δ = Dominated by S = 1 input
ΔΔ = Dominated by R = 0 input

DC Electrical Characteristics

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$, $V_{IN}=V_{DD}$ or V_{SS}		20		0.01	20		150	µA
		$V_{DD}=10V$, $V_{IN}=V_{DD}$ or V_{SS}		40		0.01	40		300	µA
		$V_{DD}=15V$, $V_{IN}=V_{DD}$ or V_{SS}		80		0.02	80		600	µA
V_{OL}	LOW Level Output Voltage	$|I_O| \leq 1$ µA, $V_{IL}=0V$, $V_{IH}=V_{DD}$								
		$V_{DD}=5.0V$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$		0.05		0	0.05		0.05	V
V_{OH}	HIGH Level Output Voltage	$|I_O| \leq 1$ µA, $V_{IL}=0V$, $V_{IH}=V_{DD}$								
		$V_{DD}=5.0V$	4.95		4.95	5.0		4.95		V
		$V_{DD}=10V$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$	14.95		14.95	15		14.95		V
V_{IL}	LOW Level Input Voltage	$|I_O| \leq 1$ µA								
		$V_{DD}=5.0V$, $V_O=0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD}=10V$, $V_O=1.0V$ or $9.0V$		3.0		4.5	3.0		3.0	V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	HIGH Level Input Voltage	$|I_O| \leq 1$ µA								
		$V_{DD}=5.0V$, $V_O=0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD}=5.0V$, $V_O=1.0V$ or $9.0V$	7.0		7.0			7.0		V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$	11		11			11		V
I_{OL}	LOW Level Output Current (Note 3)	$V_{IL}=0V$, $V_{IH}=V_{DD}$								
		$V_{DD}=5.0V$, $V_O=0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.3		1.1	2.2		0.9		mA
		$V_{DD}=15V$, $V_O=1.5V$	3.6		3.0	6.0		2.4		mA
I_{OH}	HIGH Level Output Current (Note 3)	$V_{IL}=0V$, $V_{IH}=V_{DD}$								
		$V_{DD}=5.0V$, $V_O=4.6V$	−0.52		−0.44	−0.32		−0.36		mA
		$V_{DD}=10V$, $V_O=9.5V$	−1.3		−1.1	−0.8		−0.9		mA
		$V_{DD}=15V$, $V_O=13.5V$	−3.6		−3.0	−2.4		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$	−0.3			−0.3			−1.0	µA
		$V_{DD}=15V$, $V_{IN}=15V$	0.3			0.3			1.0	µA

Timing Waveforms

Enable Timing

CD4043
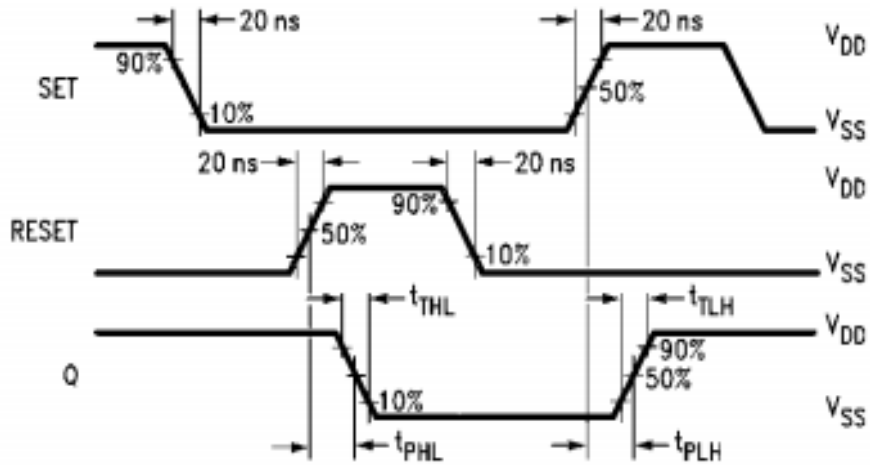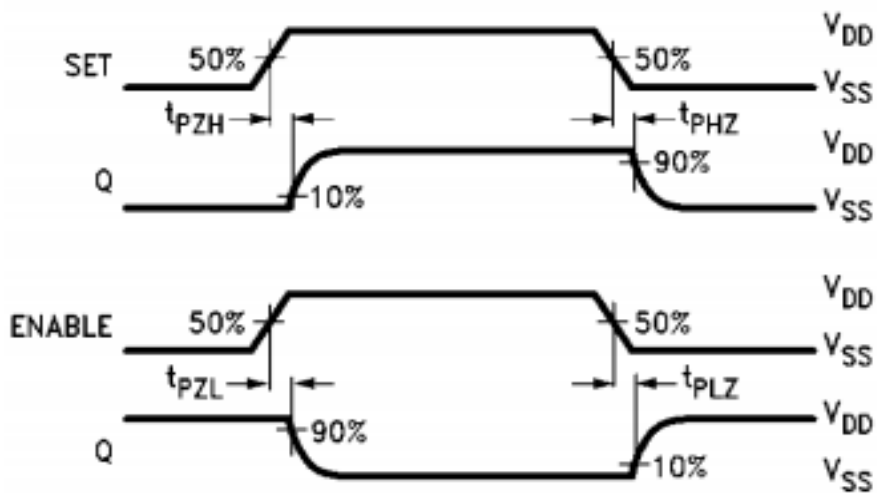
Pin Assignment

DIP16
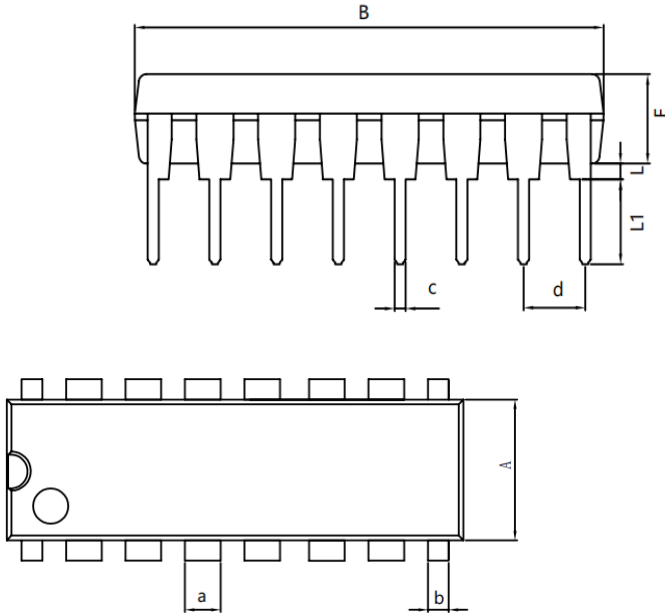
Dimensions In Millimeters					
Symbol :	Min :	Max :	Symbol :	Min :	Max :
A	6.100	6.680	L	0.500	0.800
B	18.940	19.560	a	1.524 TYP	
D	8.200	9.200	b	0.889 TYP	
D1	7.42	7.820	c	0.457 TYP	
E	3.100	3.550	d	2.540 TYP	
L	0.500	0.800			

SOP16
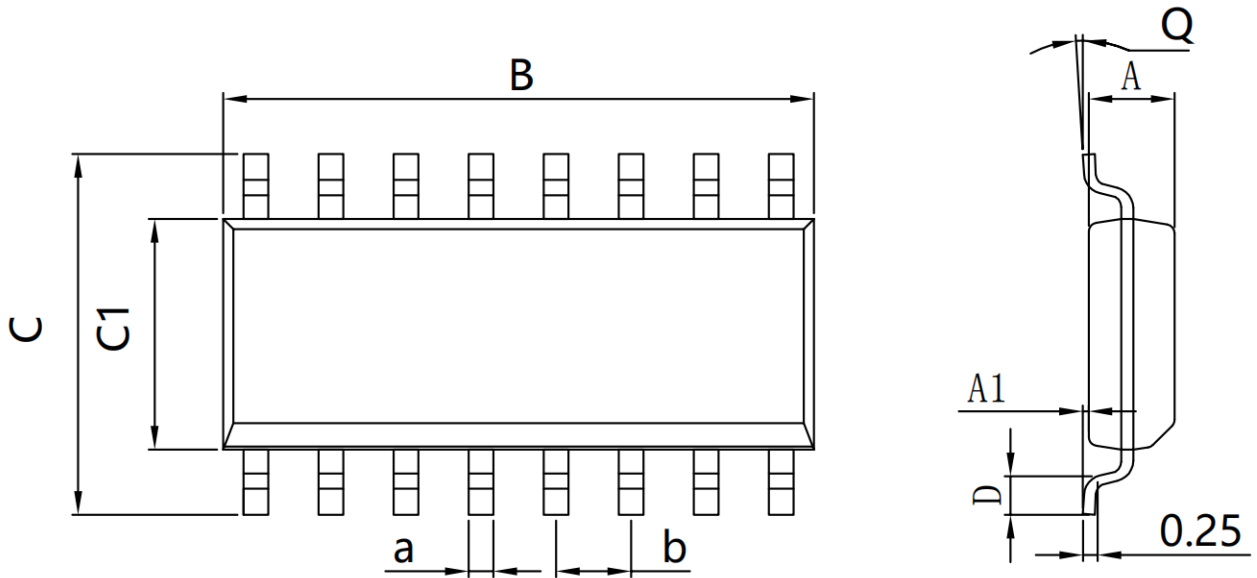
Dimensions In Millimeters					
Symbol :	Min :	Max :	Symbol :	Min :	Max :
A	1.225	1.570	D	0.400	0.950
A1	0.100	0.250	Q	0°	8°
B	9.800	10.00	a	0.420 TYP	
C	5.800	6.250	b	1.270 TYP	
C1	3.800	4.000			