Description

AT8236 is a DC brushed motor driver, which can bidirectional control motor through peak current up to 6A.Using the current decay mode, the motor speed can be controlled by pulse width modulation (PWM) on the input signal, and it has a low-power sleep mode.

AT8236 integrates synchronous rectification function, which can significantly reduce the power consumption requirements of the system.

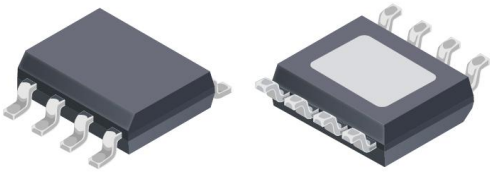
Internal protection function includes over current protection, short circuit protection, undervoltage lockout protection and overtemperature protection. AT8236N provides a fault detection output pin.

AT8236 provides an ESOP8 package with exposed pad, which can effectively improve the heat dissipation performance, and is a lead-free product that meets environmental protection requirements.

Features

- Single Channel H-bridge Motor Driver
- Wide Voltage Supply，5.5V-36V
- Low $R_{DS(ON)}$ resistance，200mΩ（HS+LS）
- 6A peak drive output，4A continuous drive output
- PWM control interface
- Support low power sleep mode

Package



ESOP8

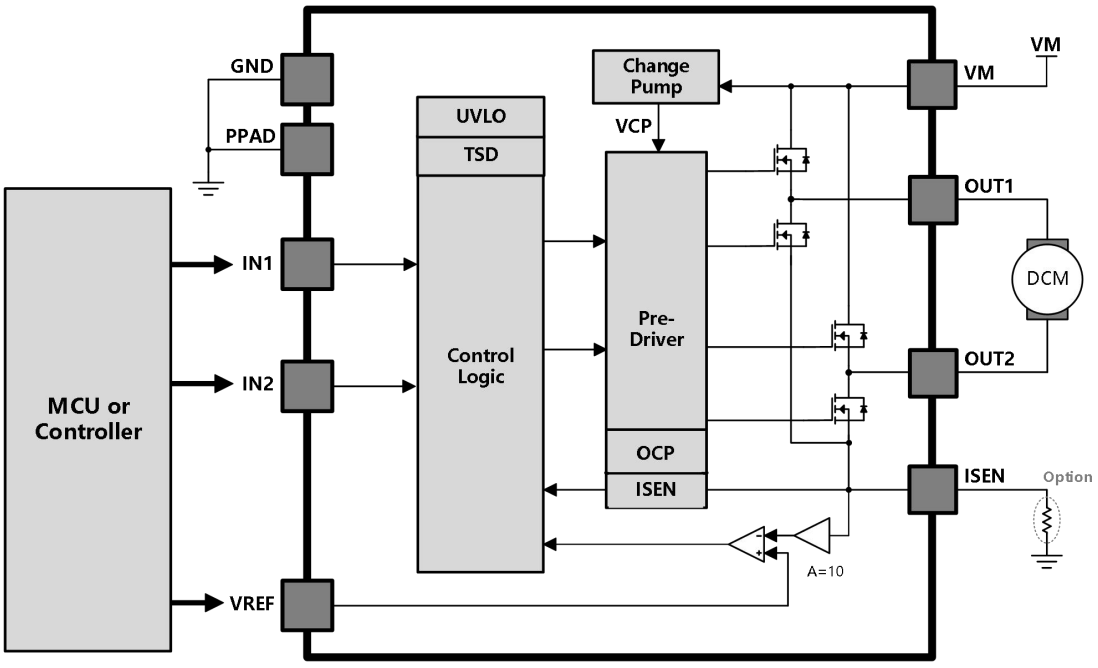
Application

- Printer and office automation equipment
- Electrical appliances
- Smart home
- Industrial control

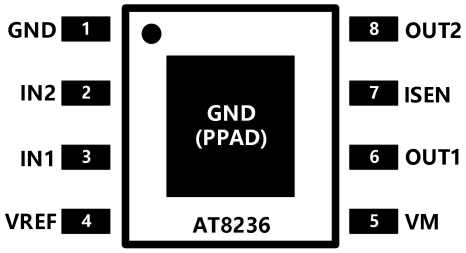
Selection Guide

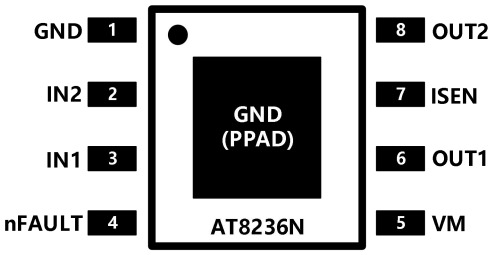
Model	Package	Packaging Information
AT8236	ESOP8	Taping，4000 pcs/reel
AT8236N	ESOP8	Taping，4000 pcs/reel

Typical Application Diagram



Pin Configuration





Pin List

Pin Name	Pin number	Pin Definition	Description
Power and Ground			
GND	1	Chip Ground	All GND pins and exposed pads of the chip must be connected to the power ground.
PPAD	-		
VM	5	Chip Power	Chip power supply and motor power supply must be filtered
Control Logic			
IN1	3	Logic Input	Control H-bridge output state, built-in pull-down resistor
IN2	2		
VREF	4	Reference Voltage Input (8236)	Reference voltage input to set driving peak current.
nFAULT		Fault detection output (8236N)	Open drain output, use external pull-up resistor. When over current, over temperature, under voltage, nFAULT will be pulled low.
ISEN	7	H-bridge current-sense input / ground	H bridge current-sense terminal，connect the current-sense resistor to the ground，if current limiting is not required, ground it directly
Output			
OUT1	6	H-bridge output 1	H-bridge output， Define the forward current as OUT1 → OUT2
OUT2	8	H-bridge output 2	

Limit Parameters at T_A = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Power Supply	VM		-0.3 – 40	V
Peak Output Current	I_{PEAK}		±6	A
Logic Input Voltage	V_{IN}		-0.7 to 7	V
Sense Voltage	V_{SENSE}		-0.3 to 0.5	V
Working Temperature	T_A	Range S	-40 to 85	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		-55 to 150	°C

Thermal Resistance Characteristics at T_A = 25°C

Thermal Metering	ESOP 8PINS	Unit
θ_{JA} - Thermal resistance coefficient from silicon core to environment (*)	35	°C/W

(*)The thermal resistance coefficient of the silicon core to the environment under natural convection conditions is obtained by actual testing on the JEDEC standard high-K circuit board specified in JESD51-7. The environmental conditions are as described in JESD51-2a.

Recommended working conditions at T_A= 25°C

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	VM	5.5	-	36	V
Continuous Output Current	I_{OUT}	0	-	3	A
Peak Output Current	I_{PEAK}	0	-	4.5	A
Logic Input Voltage	V_{IN}	0	-	5.25	V
Logic Input Frequency	f_{PWM}	0	-	100	kHZ
Reference Voltage	V_{REF}	0.5	-	4	V

(*)When the chip works with large current, heat dissipation of the chip should be done well.

Electrical Characteristics at T_A= 25°C, V_M= 24 V

Parameter		Conditions	Min	Typ	Max	Unit
Power Supply						
I_{VM}	VM static working current	f_{PWM} < 50 kHz	-	4.5	6	mA
I_{VMQ}	VM sleep current	IN1 = IN2 = 0 V	-	20	30	uA
V_{UVLO}	VM undervoltage lockout value	VM rise	-	4.7	5.0	V
V_{HYS}	VM undervoltage hysteresis		-	300	-	mV
Logic Input						
V_{IL}	Logic input low voltage		-	0.5	0.7	V
V_{IH}	Logic input high voltage		1.5	-	5.25	V
V_{HYS}	Logic input hysteresis		-	0.2	-	V
I_{IL}	Logic input current_low level	V_{IN} = 0 V	-0.2	-	0.2	uA
I_{IH}	Logic input current_high level	V_{IN} = 3.3 V	-	33	100	uA
R_{pd}	Input internal pull-down resistor	Other	-	100	-	kΩ
t_{SLEEP}	Sleep delay		-	0.7	1.0	ms
H-bridge FETS						
$R_{DS(ON)}$	High side+low side FET resistance	I_O = 1A，T_J = 25°C	-	200	-	mΩ
I_{OFF}	Output shutdown leakage current		-1	-	1	uA
Drive circuit timing and current configuration						
t_{OFF}	Current decay time	Internal PWM fixed turn-off time	-	23	-	us
t_R	Rise time	V_M =24V, 24Ω to GND, 20% to	-	150	-	ns
t_F	Fall time	V_M =24V, 24Ω to GND, 20% to	-	150	-	ns
t_{DEAD}	Dead time		-	250	-	ns
A_{ISEN}	ISEN current gain		-	10	-	V/V
t_{BLANK}	Blanking time		-	2.2	-	us
Protection Circuit						
I_{OCP}	Overcurrent threshold		6	7	10	A
T_{OCP}	Overcurrent restart time		-	3	-	ms
T_{SD}	Over temperature threshold	Junction temperature	140	150	160	℃
T_{HYS}	Over temperature hysteresis		-	30	-	℃

Functional Description

H-Bridge Control

Input pins IN1 and IN2 control the output state of H-bridge. The following table shows the logical relationship between input and output:

IN1	IN2	OUT1	OUT2	Function
0	0	Z	Z	Sliding/Sleep
1	0	H	L	Reverse
0	1	L	H	Forward
1	1	L	L	Brake

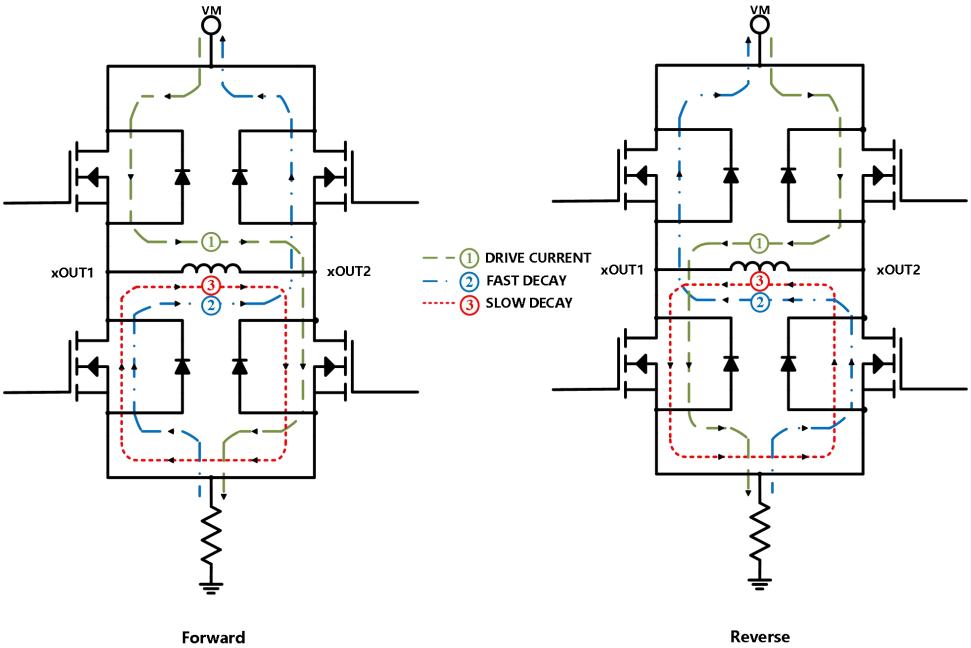
H-bridge Control Logic Table

When using PWM control to realize the speed control function, the H-bridge can operate in two different states, fast decay or slow decay. In the fast decay mode, the H-bridge is forbidden, and the freewheeling current flows through the body diode; in the slow decay mode, the two lower tubes of the output H-bridge are both open.

IN1	IN2	Function
PWM	0	Forward PWM, Fast Decay
1	PWM	Forward PWM, Slow Decay
0	PWM	Reverse PWM, Fast Decay
PWM	1	Reverse PWM, Slow Decay

Function Logic Table

The figure below shows the current path in different drive and decay modes.



Drive and Decay Mode

Current Control

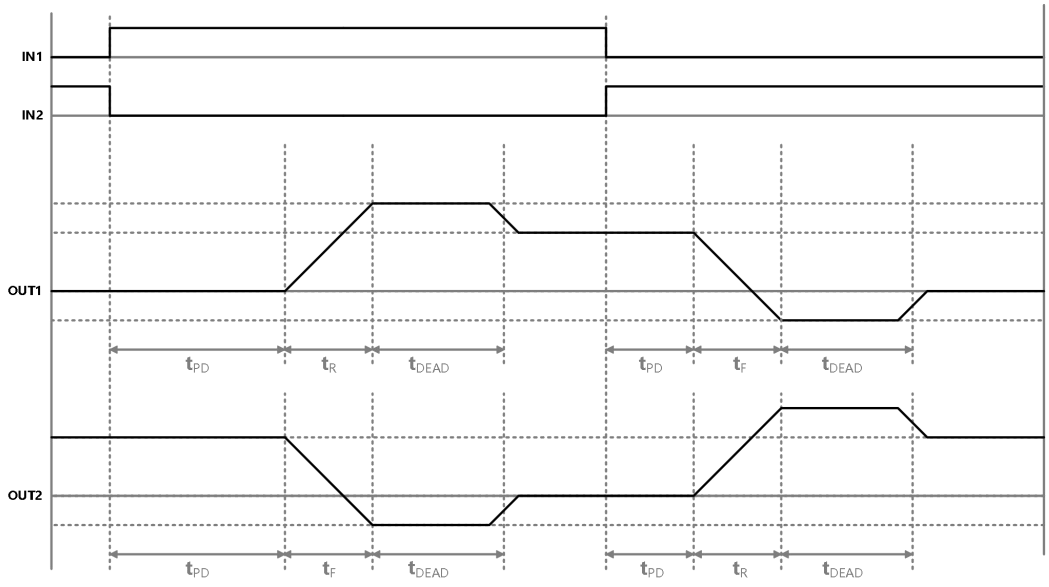
When an H-bridge is enabled, the current flowing through the corresponding bridge arm rises. When the current reaches the set threshold, the driver will turn off the current until the next PWM cycle begins. Note that at the moment the current is enabled, the voltage on the xISEN pin is ignored and after a fixed time the current detection circuit is enabled. This blanking time is generally fixed at 2.2us. This blanking time also determines the minimum PWM time when the operating current decays.

The PWM target current is set by a comparator, and the voltage on the current-sense resistor connected to the xISEN pin is multiplied by a factor of 10 and compared with a reference voltage. The reference voltage of AT8236 is input through the VREF pin, and the internal fixed VREF voltage of AT8236N is 3.3V.The following is the calculation formula of 100% target current:

$$I_{TRIP}(A) = \frac{V_{REF}(V)}{A_V \times R_{ISEN}(\Omega)} = \frac{V_{REF}(V)}{10 \times R_{ISEN}(\Omega)}$$

Dead Time

When the output changes from high level to low level or from low level to high level, there is a dead time to prevent the upper and lower tubes from conducting at the same time.In the dead time, the output is a high resistance state. When the dead time needs to be measured on the output, it needs to be measured according to the current direction of the corresponding pin at that time.If the current flows out of this pin, at this time, the voltage is one diode voltage drop below ground level; If the current flows into this pin, at this time, the voltage is one diode voltage drop above supply voltage VM.



Time Parameter

Sleep Mode

When IN1 and IN2 are both low for more than 1ms, the device will enter the sleep mode, thus greatly reducing the idle power consumption of the device. After entering the sleep mode, the H-bridge of the device is disabled and the charge pump circuit stops working. When IN1 or IN2 turns to high level and maintains at least 5us, after about 1ms delay, the chip will return to normal operation state.

Overcurrent Protection (OCP)

When the current flowing through the output tube exceeds the over-current threshold, the chip

output is turned off. After 3 ms, the chip will try to restart and return to normal.

Over Temperature Protection (TSD)

If the junction temperature exceeds the safety threshold, all FET of H-bridge are turned off. Once the junction temperature drops to a safe level, all functions of the chip will return to normal automatically.

Undervoltage Lockout Protection (UVLO)

If the voltage on the VM pin drops below the undervoltage lockout threshold, output is prohibited and the internal logic is reset. When the VM voltage rises above the UVLO voltage, all circuit return to normal.

Notice

The PCB board should be covered with a large cooling fin, and the ground wire should be connected with a wide covered ground wire. In order to optimize the electrical and thermal performance of the circuit, the chip should be directly attached to the cooling fin.

For the electrode power supply VM, an electrolytic capacitor of no less than 47uF should be connected to the ground coupling, and the capacitor should be placed as close to the device as possible.

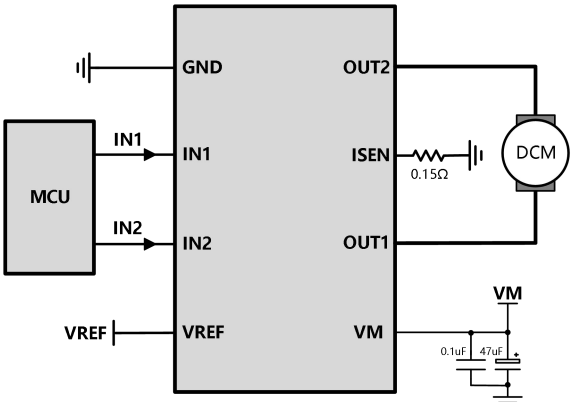
In order to avoid the capacitance coupling problem caused by high speed dv/dt conversion, the cover wire of drive circuit output end should be far away from that of logic control input end.

The lead wire of logic control terminal should adopt low impedance traces to reduce noise caused by thermal resistance.

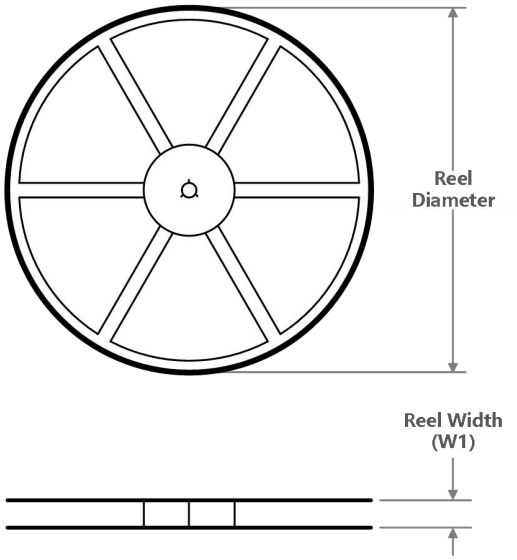
Typical Application Examples

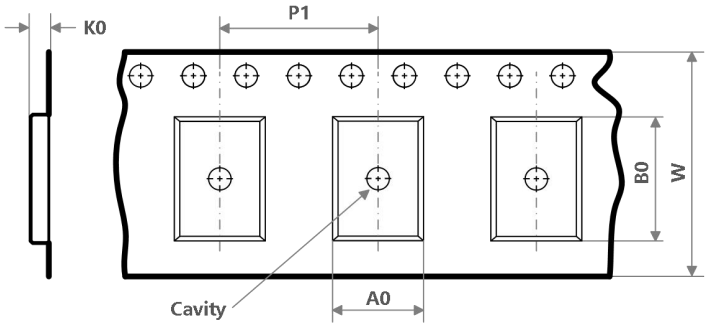
The following is an example of application schematic diagram under specific working conditions:

V_{IN}	24V
I_{OUT}	2A
V_{REF}	3.0V



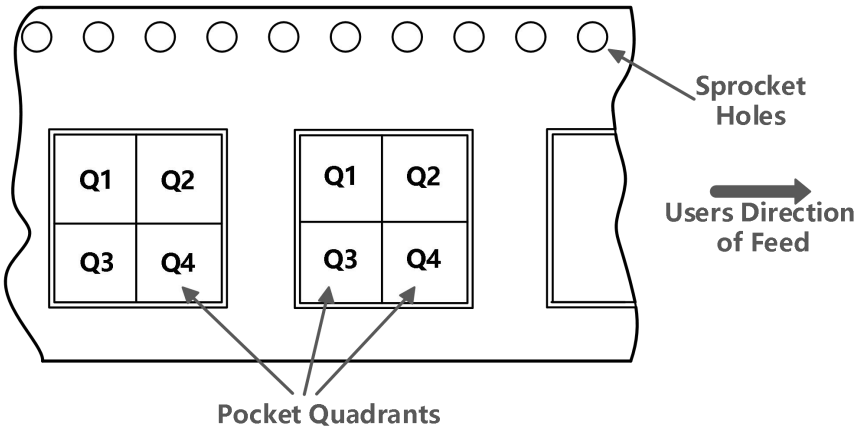
TAPE AND REEL INFORMATION





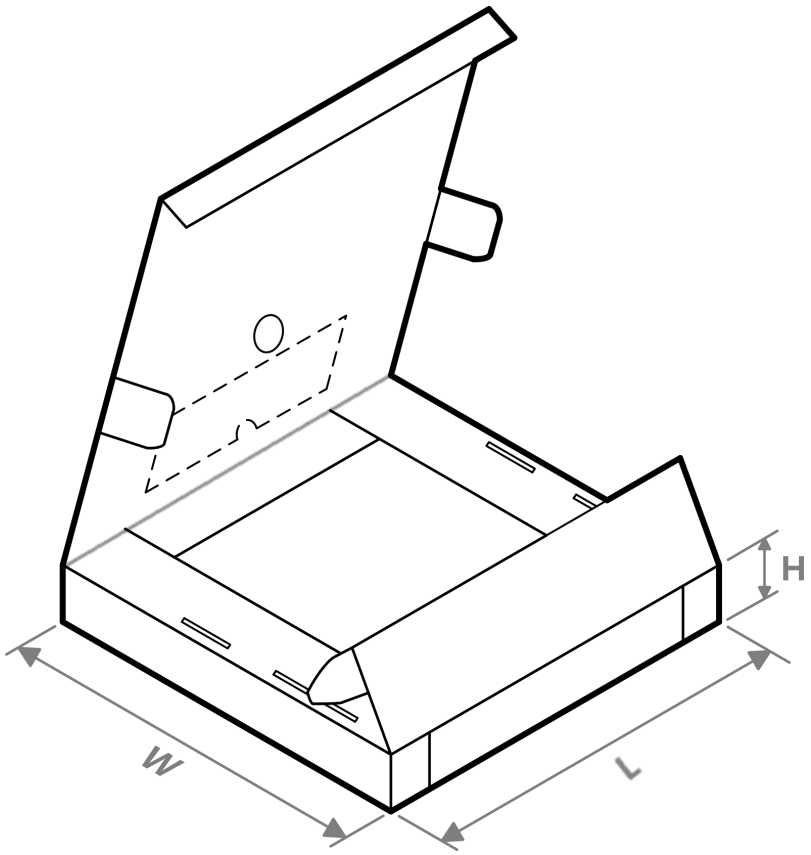
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AT8236	ESOP	-	8	4000	330	12	6.55	5.2	2	8	12	Q1
AT8236N	ESOP	-	8	4000	330	12	6.55	5.2	2	8	12	Q1

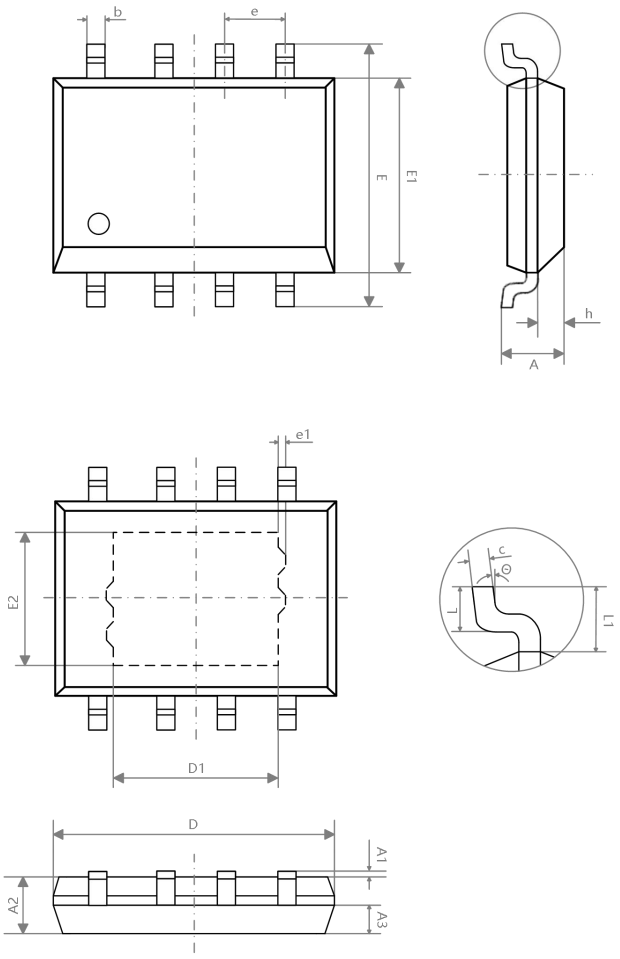
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length(mm)	Width(mm)	Height(mm)
AT8236	ESOP	-	8	4000	400	343	60
AT8236N	ESOP	-	8	4000	400	343	60

Package

ESOP8



Symbol	Millimeter (mm)		
	MIN	TYP	MAX
A	——	——	1.65
A1	0.05	——	0.15
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	——	0.47
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27(BSC)		
h	0.25	——	0.50
L	0.50	0.60	0.80
L1	1.05(REF)		
θ	0	——	8°
e1	0.10(REF)		
D1	3.10(REF)		
E2	2.21(REF)		