



16-bit Digital Signal Controllers (up to 256 KB Fl 30 KB SRAM) with Motor Control and Advanced

Operating Conditions

- 3.0V to 3.6V, -40°C to +150°C, DC to 20 MIPS
- 3.0V to 3.6V, -40°C to +125°C, DC to 40 MIPS

Core: 16-bit dsPIC33F CPU

- Code-efficient (C and Assembly) architecture
- Two 40-bit wide accumulators
- · Single-cycle (MAC/MPY) with dual data fetch
- Single-cycle mixed-sign MUL plus hardware divide

Clock Management

- ±2% internal oscillator
- · Programmable PLLs and oscillator clock sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timer (WDT)
- Fast wake-up and start-up

Power Management

- Low-power management modes (Sleep, Idle, Doze)
- · Integrated Power-on Reset and Brown-out Reset
- 1.35 mA/MHz dynamic current (typical)
- 55 µA IPD current (typical)

Motor Control PWM

- Up to four PWM generators with eight outputs
- Dead Time for rising and falling edges
- 12.5 ns PWM resolution
- PWM support for Motor Control: BLDC, PMSM, ACIM, and SRM
- Programmable Fault inputs
- Flexible trigger for ADC conversions and configurations

Advanced Analog Features

- Two ADC modules:
 - Configurable as 10-bit, 1.1 Msps with four S&H or 12-bit, 500 ksps with one S&H
 - 18 analog inputs on 64-pin devices and up to 32 analog inputs on 100-pin devices
- · Flexible and independent ADC trigger sources

Timers/Output Compare/Input Capture

- Up to nine 16-bit timers/counters. Can pair up to make four 32-bit timers.
- Eight Output Compare modules configurable as timers/counters
- Eight Input Capture modules

Communication Interfaces

- Two UART modules (10 Mbps)
 - With support for LIN 2.0 protocols and $\ensuremath{\text{IrDA}}^{\ensuremath{\mathbb{R}}}$
- Two 4-wire SPI modules (15 Mbps)
- Up to two I²C[™] modules (up to 1 Mbaud) with SMBus support
- Up to two Enhanced CAN (ECAN) modules (1 Mbaud) with 2.0B support
- Quadrature Encoder Interface (QEI) module
- Data Converter Interface (DCI) module with I²S codec support

Input/Output

- Sink/Source up to 10 mA (pin specific) for standard VOH/VOL, up to 16 mA (pin specific) for nonstandard VOH1
- 5V-tolerant pins
- · Selectable open drain, pull-ups, and pull-downs
- Up to 5 mA overvoltage clamp current
- · External interrupts on all I/O pins

Qualification and Class B Support

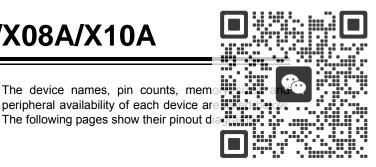
- AEC-Q100 REVG (Grade 1 -40°C to +125°C)
- AEC-Q100 REVG (Grade 0 -40°C to +150°C)
- Class B Safety Library, IEC 60730

Debugger Development Support

- · In-circuit and in-application programming
- · Two program and two complex data breakpoints
- IEEE 1149.2-compatible (JTAG) boundary scan
- Trace and run-time watch

Туре	QFN	TQFP	TQFP	TQFP
Pin Count	64	64	80	100
Contact Lead/Pitch	0.50	0.50	0.50	0.40
I/O Pins	53	53	69	85
Dimensions	9x9x0.9	10x10x1	12x12x1	14x14x1

Note: All dimensions are in millimeters (mm) unless specified.



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dsPIC33F PRODUCT FAMILIES

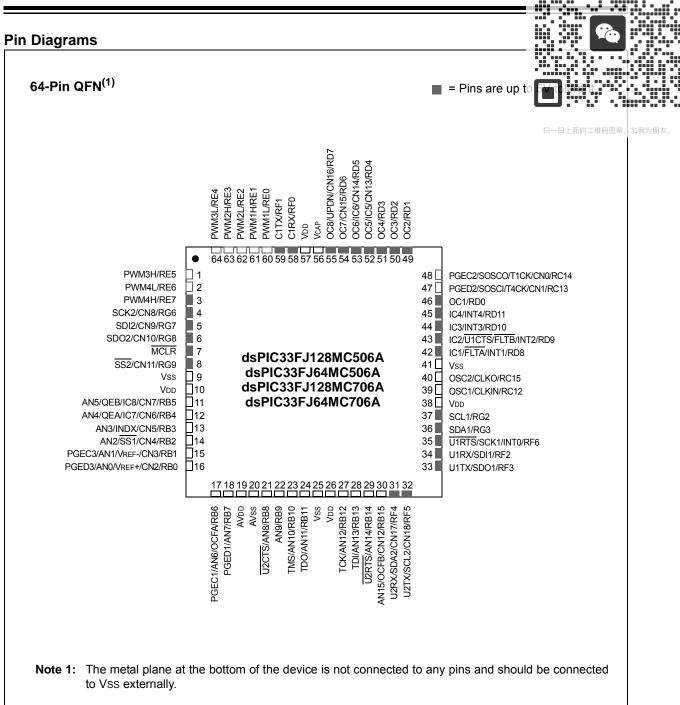
The dsPIC33FJXXXMCX06A/X08A/X10A family of devices supports a variety of motor control applications, such as brushless DC motors, single and 3-phase induction motors and switched reluctance motors. The dsPIC33F Motor Control products are also well-suited for Uninterrupted Power Supply (UPS), inverters, Switched mode power supplies, power factor correction and also for controlling the power management module in servers, telecommunication equipment and other industrial equipment.

dsPIC33FJXXXMCX06A/X08A/X10A Controller Families

Device	Pins	Program Flash Memory (Kbyte)	RAM (Kbyte) ⁽¹⁾	Timer 16-bit	Input Capture	Output Compare Std. PWM	Motor Control PWM	Quadrature Encoder Interface	Codec Interface	ADC	UART	SPI	I²C™	Enhanced CAN	I/O Pins (Max) ⁽²⁾	Packages
dsPIC33FJ64MC506A	64	64	8	9	8	8	8 ch	1	0	1 ADC, 16 ch	2	2	2	1	53	PT, MR
dsPIC33FJ64MC508A	80	64	8	9	8	8	8 ch	1	0	1 ADC, 18 ch	2	2	2	1	69	PT
dsPIC33FJ64MC510A	100	64	8	9	8	8	8 ch	1	0	1 ADC, 24 ch	2	2	2	1	85	PF, PT
dsPIC33FJ64MC706A	64	64	16	9	8	8	8 ch	1	0	2 ADC, 16 ch	2	2	2	1	53	PT, MR
dsPIC33FJ64MC710A	100	64	16	9	8	8	8 ch	1	0	2 ADC, 24 ch	2	2	2	2	85	PF, PT
dsPIC33FJ128MC506A	64	128	8	9	8	8	8 ch	1	0	1 ADC, 16 ch	2	2	2	1	53	PT, MR
dsPIC33FJ128MC510A	100	128	8	9	8	8	8 ch	1	0	1 ADC, 24 ch	2	2	2	1	85	PF, PT
dsPIC33FJ128MC706A	64	128	16	9	8	8	8 ch	1	0	2 ADC, 16 ch	2	2	2	1	53	PT, MR
dsPIC33FJ128MC708A	80	128	16	9	8	8	8 ch	1	0	2 ADC, 18 ch	2	2	2	2	69	PT
dsPIC33FJ128MC710A	100	128	16	9	8	8	8 ch	1	0	2 ADC, 24 ch	2	2	2	2	85	PF, PT
dsPIC33FJ256MC510A	100	256	16	9	8	8	8 ch	1	0	1 ADC, 24 ch	2	2	2	1	85	PF, PT
dsPIC33FJ256MC710A	100	256	30	9	8	8	8 ch	1	0	2 ADC, 24 ch	2	2	2	2	85	PF, PT

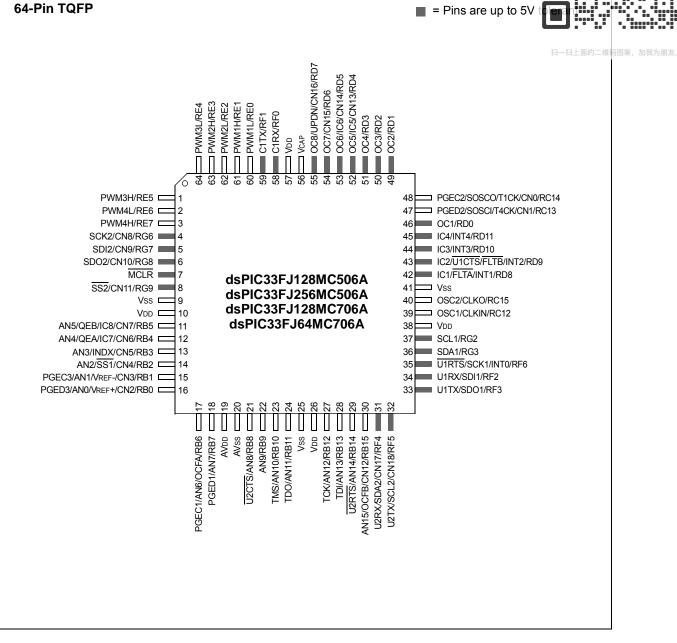
Note 1: RAM size is inclusive of 2 Kbytes DMA RAM.

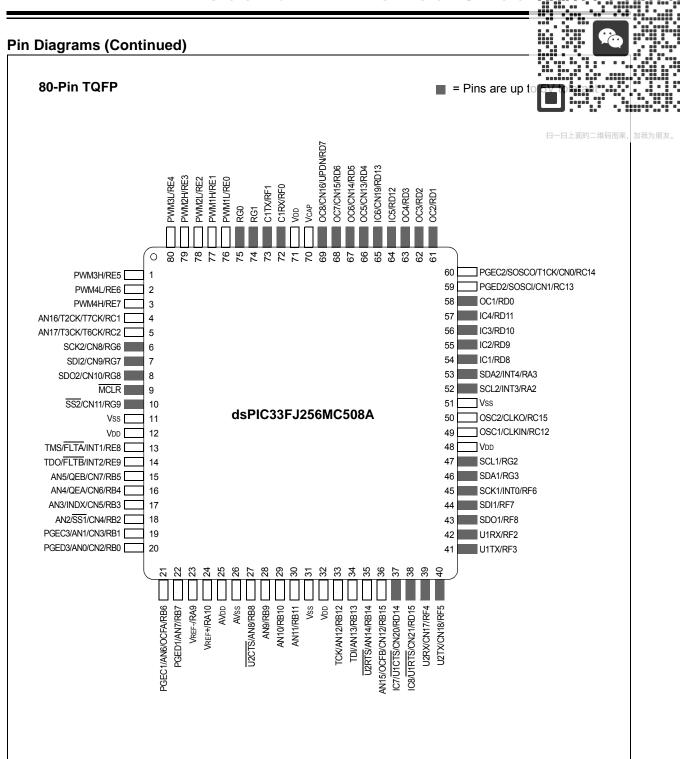
2: Maximum I/O pin count includes pins shared by the peripheral functions.





Pin Diagrams (Continued)





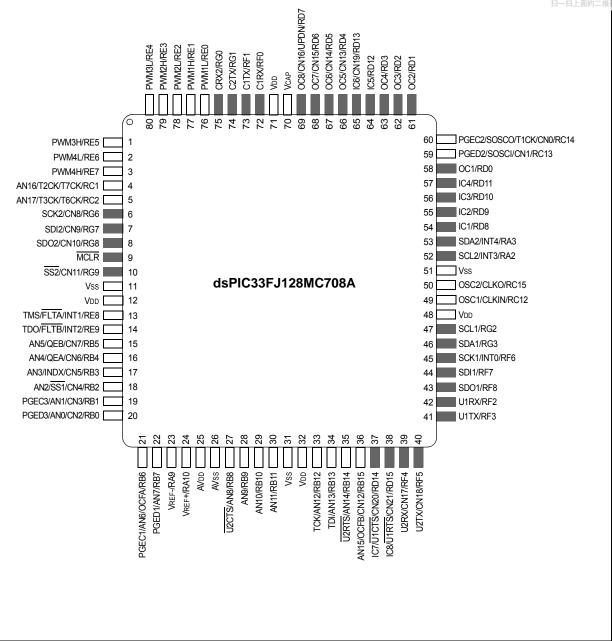
Pin Diagrams (Continued)

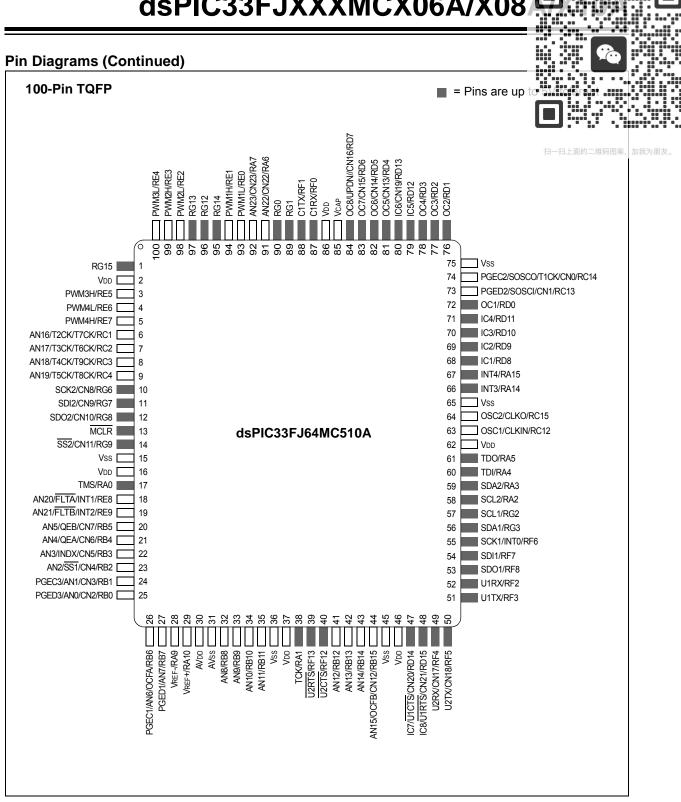
80-Pin TQFP

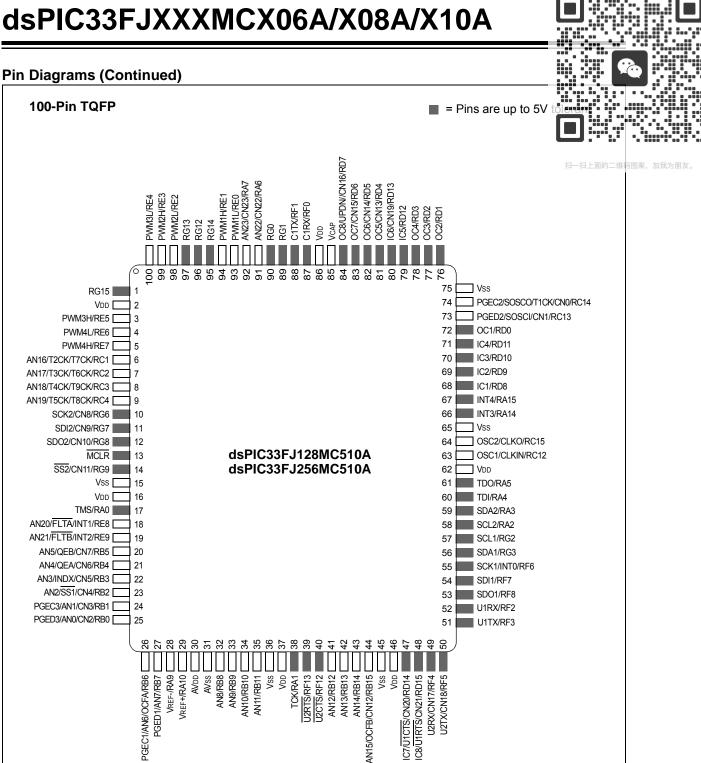


= Pins are up to 5V

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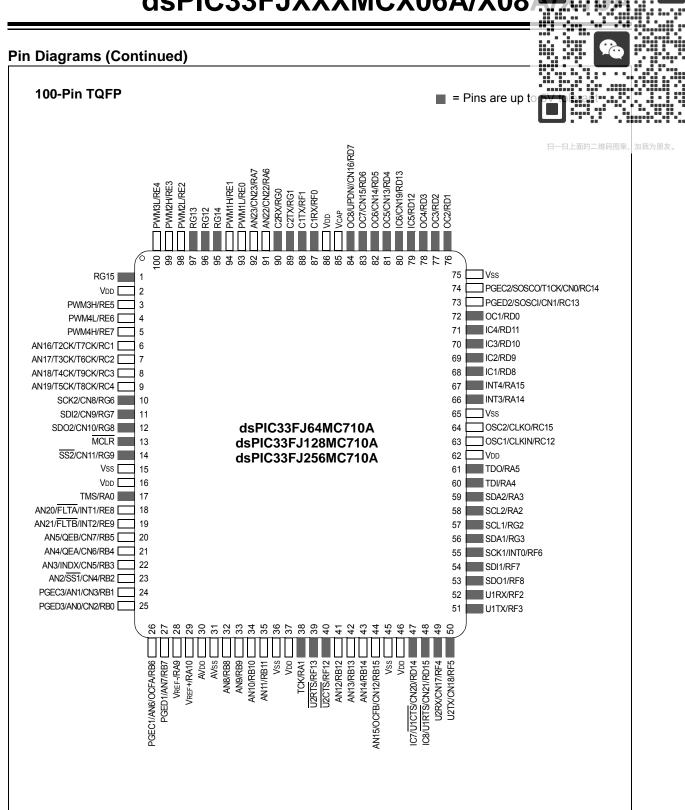


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Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

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- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

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Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33F/PIC24H Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the documents listed below, browse to the documentation section of the dsPIC33FJ256MC710A product page on the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

In addition to parameters, features, and other documentation, the resulting page provides links to the related family reference manual sections.

- Section 1. "Introduction" (DS70197)
- Section 2. "CPU" (DS70204)
- Section 3. "Data Memory" (DS70202)
- Section 4. "Program Memory" (DS70203)
- Section 5. "Flash Programming" (DS70191)
- Section 6. "Interrupts" (DS70184)
- Section 7. "Oscillator" (DS70186)
- Section 8. "Reset" (DS70192)
- Section 9. "Watchdog Timer and Power-Saving Modes" (DS70196)
- Section 10. "I/O Ports" (DS70193)
- Section 11. "Timers" (DS70205)
- Section 12. "Input Capture" (DS70198)
- Section 13. "Output Compare" (DS70209)
- Section 14. "Motor Control PWM" (DS70187)
- Section 15. "Quadrature Encoder Interface (QEI)" (DS70208)
- Section 16. "Analog-to-Digital Converter (ADC)" (DS70183)
- Section 17. "UART" (DS70188)
- Section 18. "Serial Peripheral Interface (SPI)" (DS70206)
- Section 19. "Inter-Integrated Circuit[™] (I2C[™])" (DS70195)
- Section 20. "Data Converter Interface (DCI)" (DS70288)
- Section 21. "Enhanced Controller Area Network (ECAN™)" (DS70185)
- Section 22. "Direct Memory Access (DMA)" (DS70182)
- Section 23. "CodeGuard™ Security" (DS70199)
- Section 24. "Programming and Diagnostics" (DS70207)
- Section 25. "Device Configuration" (DS70194)



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1.0 DEVICE OVERVIEW

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/X08A/ X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F/PIC24H Family Reference Manual"*. Please see the Microchip web site (www.microchip.com) for the latest dsPIC33F/PIC24H Family Reference Manual sections.
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

This document contains device-specific information for the following devices:

- dsPIC33FJ64MC506A
- dsPIC33FJ64MC508A
- dsPIC33FJ64MC510A
- dsPIC33FJ64MC706A
- dsPIC33FJ64MC710A
- dsPIC33FJ128MC506A
- dsPIC33FJ128MC510A
- dsPIC33FJ128MC706A
- dsPIC33FJ128MC708A
- dsPIC33FJ128MC710A
- dsPIC33FJ256MC510A
- dsPIC33FJ256MC710A

The dsPIC33FJXXXMCX06A/X08A/X10A includes devices with a wide range of pin counts (64, 80 and 100), different program memory sizes (64 Kbytes, 128 Kbytes and 256 Kbytes) and different RAM sizes (8 Kbytes, 16 Kbytes and 30 Kbytes).

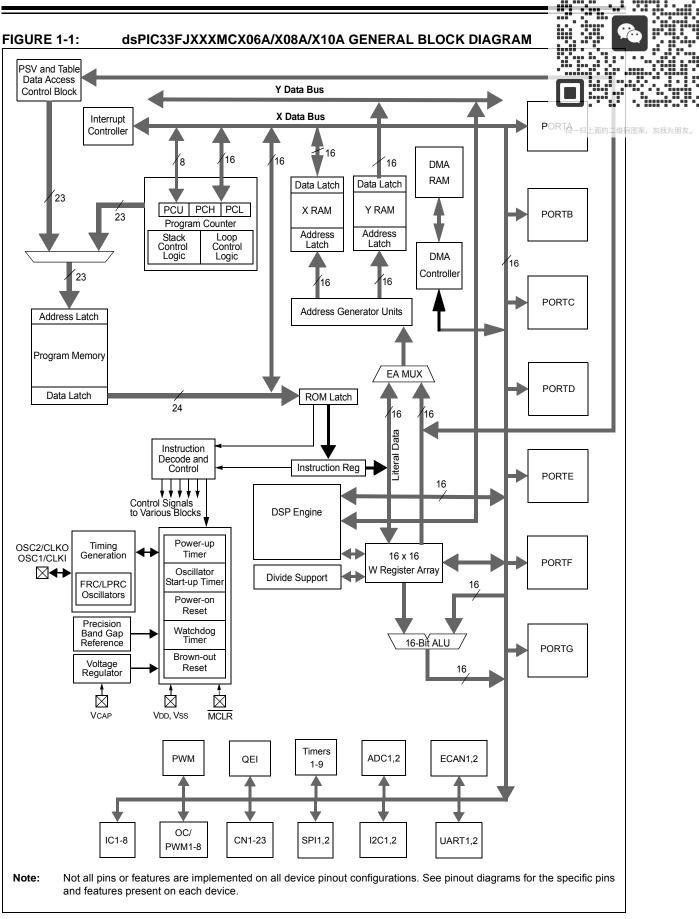
These features make this family survively of high-performance, digital signature tions. The devices are pin compatible family of devices, and also share a v compatibility with the dsPIC30F families as



necessitated by the specific functionality computational maxmax, resource and system cost requirements of the application.

The dsPIC33FJXXXMCX06A/X08A/X10A family of devices employs a powerful 16-bit architecture that seamlessly integrates the control features of a Microcontroller (MCU) with the computational capabilities of a Digital Signal Processor (DSP). The resulting functionality is ideal for applications that rely on high-speed, repetitive computations, as well as control.

The DSP engine, dual 40-bit accumulators, hardware support for division operations, barrel shifter, 17 x 17 multiplier, a large array of 16-bit working registers and a wide variety of data addressing modes, together, the dsPIC33FJXXXMCX06A/X08A/X10A provide Central Processing Unit (CPU) with extensive mathematical processing capability. Flexible and deterministic interrupt handling, coupled with a powerful array of peripherals, renders the dsPIC33FJXXXMCX06A/X08A/X10A devices suitable for control applications. Further, Direct Memory Access (DMA) enables overhead-free transfer of data between several peripherals and a dedicated DMA RAM. Reliable, field programmable Flash program memory ensures scalability of applications that use dsPIC33FJXXXMCX06A/X08A/X10A devices.



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nected at all times.	
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TABLE 1-1: PINOUT I/O DESCRIPTIONS

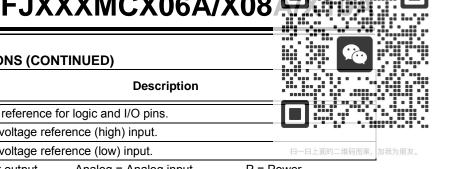
AN0-AN31 AVdd AVss	I	· · ·	
AVss		Analog	Analog input channels.
	Р	Р	Positive supply for analog modules. This pin must be connected at all times.
	Р	Р	Ground reference for analog modules. 扫一扫上面的二维码图案
CLKI CLKO	I O	ST/CMOS	External clock source input. Always associated with OSC1 pin function. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
CN0-CN23	Ι	ST	Input change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
C1RX	I	ST	ECAN1 bus receive pin.
C1TX	0	—	ECAN1 bus transmit pin.
C2RX	I	ST	ECAN2 bus receive pin.
C2TX	0	—	ECAN2 bus transmit pin.
PGED1	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 1.
PGEC1	I	ST	Clock input pin for Programming/Debugging Communication Channel 1.
PGED2	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 2.
PGEC2	Ī	ST	Clock input pin for Programming/Debugging Communication Channel 2.
PGED3	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 3.
PGEC3		ST	Clock input pin for Programming/Debugging Communication Channel 3.
IC1-IC8	1	ST	Capture Inputs 1 through 8.
INDX	J	ST	Quadrature Encoder Index Pulse input.
QEA	I I	ST	Quadrature Encoder Phase A input in QEI mode. Auxiliary timer external clock
	I		gate input in Timer mode.
QEB	I.	ST	Quadrature Encoder Phase A input in QEI mode. Auxiliary timer external clock
	I	51	gate input in Timer mode.
UPDN	0	CMOS	Position up/down counter direction state.
INT0		ST	
INT0 INT1	1	ST	External Interrupt 0.
	1		External Interrupt 1.
INT2	1	ST ST	External Interrupt 2.
INT3 INT4	1	ST	External Interrupt 3. External Interrupt 4.
FLTA	I	ST	PWM Fault A input.
FLTB		ST	PWM Fault B input.
PWM1L	0	—	PWM1 low output.
PWM1H	0	-	PWM1 high output.
PWM2L	0	—	PWM2 low output.
PWM2H	0	-	PWM2 high output.
PWM3L	0	-	PWM3 low output.
PWM3H	0	_	PWM3 high output.
PWM4L	0	—	PWM4 low output.
PWM4H	0	—	PWM4 high output.
MCLR	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
OCFA	I	ST	Compare Fault A input (for Compare Channels 1, 2, 3 and 4).
OCFB	I	ST	Compare Fault B input (for Compare Channels 5, 6, 7 and 8).
OC1-OC8	0	—	Compare outputs 1 through 8.
OSC1	Ι	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	_	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.

TABLE 1-1:	PINOU	T I/O DES	CRIPTIONS (CONTINUED)		
Pin Name	Pin Type	Buffer Type	Description		
RA0-RA7	I/O	ST	PORTA is a bidirectional I/O port.		
RA9-RA10	I/O	ST			*
RA12-RA15	I/O	ST		——扫—扫上面的二维	-
RB0-RB15	I/O	ST	PORTB is a bidirectional I/O port.		
RC1-RC4	I/O	ST	PORTC is a bidirectional I/O port.		
RC12-RC15	I/O	ST			
RD0-RD15	I/O	ST	PORTD is a bidirectional I/O port.		
RE0-RE9	I/O	ST	PORTE is a bidirectional I/O port.		
RF0-RF8 RF12-RF13	I/O	ST	PORTF is a bidirectional I/O port.		
RG0-RG3	I/O	ST	PORTG is a bidirectional I/O port.		
RG6-RG9	I/O	ST			
RG12-RG15	I/O	ST			
SCK1	I/O	ST	Synchronous serial clock input/output for SPI1.		
SDI1 SDO1		ST	SPI1 data in. SPI1 data out.		
<u>SS1</u>	1/0	ST	SPI1 slave synchronization or frame pulse I/O.		
SCK2	I/O	ST	Synchronous serial clock input/output for SPI2.		
SDI2	I	ST	SPI2 data in.		
SDO2	0	—	SPI2 data out.		
SS2	I/O	ST	SPI2 slave synchronization or frame pulse I/O.		
SCL1	I/O	ST	Synchronous serial clock input/output for I2C1.		
SDA1	I/O	ST	Synchronous serial data input/output for I2C1.		
SCL2 SDA2	I/O I/O	ST ST	Synchronous serial clock input/output for I2C2. Synchronous serial data input/output for I2C2.		
SOSCI					
SOSCO			32.768 kHz low-power oscillator crystal input; CMOS otherwise. 32.768 kHz low-power oscillator crystal output.		
TMS	I	ST	JTAG Test mode select pin.		
TCK	I	ST	JTAG test clock input pin.		
TDI	I	ST	JTAG test data input pin.		
TDO	0	—	JTAG test data output pin.		
T1CK	I	ST	Timer1 external clock input.		
T2CK T3CK		ST ST	Timer2 external clock input.		
T4CK		ST	Timer3 external clock input. Timer4 external clock input.		
T5CK	i	ST	Timer5 external clock input.		
T6CK	I	ST	Timer6 external clock input.		
T7CK	I	ST	Timer7 external clock input.		
T8CK	I	ST	Timer8 external clock input.		
T9CK	I	ST	Timer9 external clock input.		
U1CTS	I	ST	UART1 clear to send.		
U1RTS	0	-	UART1 ready to send.		
U1RX		ST	UART1 receive.		
U1TX U2CTS	0	ST	UART1 transmit. UART2 clear to send.		
U2RTS	0		UART2 ready to send.		
U2RX	I	ST	UART2 receive.		
U2TX	Ó	—	UART2 transmit.		
Vdd	Р	_	Positive supply for peripheral logic and I/O pins.		1
VCAP	P		CPU logic filter capacitor connection.		

TAB

Legend: CMOS compatible input or output Analog = Analog input CIV ST = Schmitt Trigger input with CMOS levels O = Output

I = Input



PINOUT I/O DESCRIPTIONS (CONTINUED) TABLE 1-1:

Pin Name	Pin Type	Buffer Type	Description	
Vss	Р	—	Ground reference for logic and I/O pins.	
VREF+	I	Analog	Analog voltage reference (high) input.	
VREF-	I	Analog	Analog voltage reference (low) input.	扫一扫上面的二维码图案,加我为朋
Legend: CMC)S = CMO	S compatible	e input or output Analog = Analog input	P = Power

ST = Schmitt Trigger input with CMOS levels O = Output

I = Input

NOTES:



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2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/X08A/ X10A family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "dsPIC33F/ PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33FJXXXMCX06A/X08A/X10A family of 16-bit Digital Signal Controllers (DSC) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and Vss pins (see Section 2.2 "Decoupling Capacitors")
- All AVDD and AVss pins (regardless if ADC module is not used)
- (see Section 2.2 "Decoupling Capacitors")
 VCAP
- (see Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)")
- MCLR pin (see Section 2.4 "Master Clear (MCLR) Pin")
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see Section 2.5 "ICSP Pins")
- OSC1 and OSC2 pins when external oscillator source is used
 Oscillator Discussion of the second operation operatio

(see Section 2.6 "External Oscillator Pins")

Additionally, the following pins may be required:

• VREF+/VREF- pins used when external voltage reference for ADC module is implemented

Note: The AVDD and AVSS pins must be connected independent of the ADC voltage reference source.

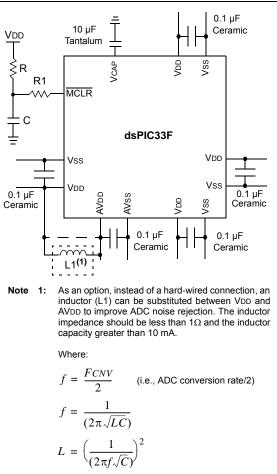
2.2 Decoupling Capacito

The use of decoupling capacitors power supply pins, such as VDD AVss is required.



- Value and type of capacitor: Recommendation of 0.1 μ F (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.
- Placement on the printed circuit board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- Handling high-frequency noise: If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μ F to 0.001 μ F. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 μ F in parallel with 0.001 μ F.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.





2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μ F to 47 μ F.

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (< 5 Ohms) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD and must have a capacitor between 4.7 μ F and 10 μ F, 16V connected to ground. The type can be ceramic or tantalum. Refer to Section 26.0 "Electrical Characteristics" for additional information.

The placement of this capacitor should be VCAP. It is recommended that the trace exceed one-quarter inch (6 mm). Refer to "On-Chip Voltage Regulator" for details



2.4 Master Clear (MCLR) Pin

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- Device Reset
- Device Programming and Debugging

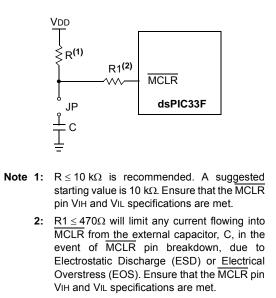
During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the \overline{MCLR} pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor, C, be isolated from the MCLR pin during programming and debugging operations.

Place the components shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2:	

EXAMPLE OF MCLR PIN CONNECTIONS





2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial ProgrammingTM (ICSPTM) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the "dsPIC33F/PIC24H Flash Programming Specification" (DS70152) for information on capacitive loading limits, and pin input voltage high (VIH) and input low (VIL) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to the MPLAB[®] ICD 3 or REAL ICE™ in-circuit emulator.

For more information on the ICD 3 and REAL ICE in-circuit emulator connection requirements, refer to the following documents that are available on the Microchip web site.

- "Using MPLAB[®] ICD 3" (poster) (DS51765)
- *"MPLAB[®] ICD 3 Design Advisory"* (DS51764)
- "MPLAB[®] REAL ICE™ In-Circuit Emulator User's Guide" (DS51616)
- "Using MPLAB[®] REAL ICE™ In-Circuit Emulator" (poster) (DS51749)

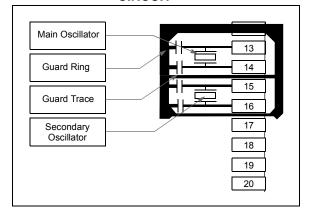
2.6 External Oscillator P

Many DSCs have options for at least high-frequency primary oscillator and secondary oscillator (refer to **Sectio Configuration**" for details).

The oscillator circuit should be placed on the same methanics, side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

FIGURE 2-3:

SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT





2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to \leq 8 MHz for start-up with PLL enabled to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start-up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLDBF to a suitable value, and then perform a clock switch to the oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration Word.

2.8 Configuration of Analog and Digital Pins During ICSP Operations

If the MPLAB ICD 3 or REAL ICE in-circuit emulator is selected as a debugger, it automatically initializes all of the A/D input pins (ANx) as "digital" pins by setting all bits in the AD1PCFGL register.

The bits in this register that correspond to that are initialized by the MPLAB ICD 3 in-circuit emulator, must not be cleared application firmware; otherwise, commun will result between the debugger and the

If your application needs to use certain A/D pins as analog input pins during the debug session, 他他的感觉问题, 加我为朋友, application must clear the corresponding bits in the AD1PCFGL register during initialization of the ADC module.

When the MPLAB ICD 3 or REAL ICE in-circuit emulator is used as a programmer, the user application firmware must correctly configure the AD1PCFGL register. Automatic initialization of this register is only done during debugger operation. Failure to correctly configure the register(s) will result in all A/D pins being recognized as analog input pins, resulting in the port value being read as a logic '0', which may affect user application functionality.

2.9 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.

Alternatively, connect a 1k to 10k resistor between Vss and the unused pins.

3.0 CPU

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section
 2. "CPU" (DS70204) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33FJXXXMCX06A/X08A/X10A CPU module has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for DSP. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space. The actual amount of program memory implemented varies by device. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double word move (MOV.D) instruction and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

The dsPIC33FJXXXMCX06A/X08A/X10A devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can serve as a data, address or address offset register. The 16th working register (W15) operates as a software Stack Pointer (SP) for interrupts and calls.

The dsPIC33FJXXXMCX06A/X08A/X10A instruction set has two classes of instructions: MCU and DSP. These two instruction classes are seamlessly integrated into a single CPU. The instruction set includes many addressing modes and is designed for optimum 'C' compiler efficiency. For most instructions, the dsPIC33FJXXXMCX06A/X08A/X10A devices are capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing A + B = C operations to be executed in a single cycle.

A block diagram of the CPU is shown in Figure 3-1 and the programmer's model for the dsPIC33FJXXXMCX06A/X08A/X10A is shown in Figure 3-2.

3.1 Data Addressing Ove



X memory AGU, which accesses the entire memory map as one linear data space. Certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y data space boundary is device-specific.

Overhead-free circular buffers (Modulo Addressing mode) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. Furthermore, the X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms.

The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary defined by the 8-bit Program Space Visibility Page register (PSVPAG). The program to data space mapping feature lets any instruction access program space as if it were data space.

The data space also includes 2 Kbytes of DMA RAM, which is primarily used for DMA data transfers but may be used as general purpose RAM.

3.2 DSP Engine Overview

The DSP engine features a high-speed, 17-bit by 17-bit multiplier, a 40-bit ALU, two 40-bit saturating accumulators and a 40-bit bidirectional barrel shifter. The barrel shifter is capable of shifting a 40-bit value up to 16 bits right or left in a single cycle. The DSP instructions operate seamlessly with all other instructions and have been designed for optimal real-time performance. The MAC instruction and other associated instructions can concurrently fetch two data operands from memory while multiplying two W registers, and accumulating and optionally saturating the result in the same cycle. This instruction functionality requires that the RAM memory data space be split for these instructions and linear for all others. Data space partitioning is achieved in a transparent and flexible manner through dedicating certain working registers to each address space.

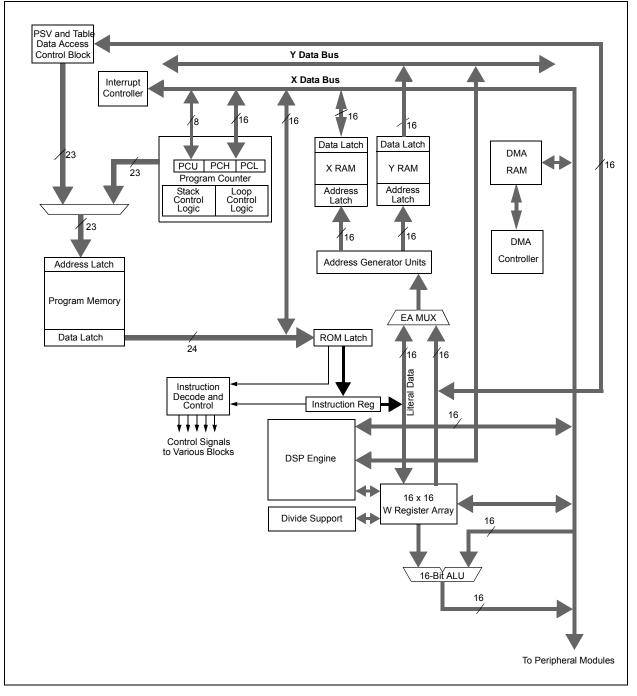
3.3 Special MCU Features

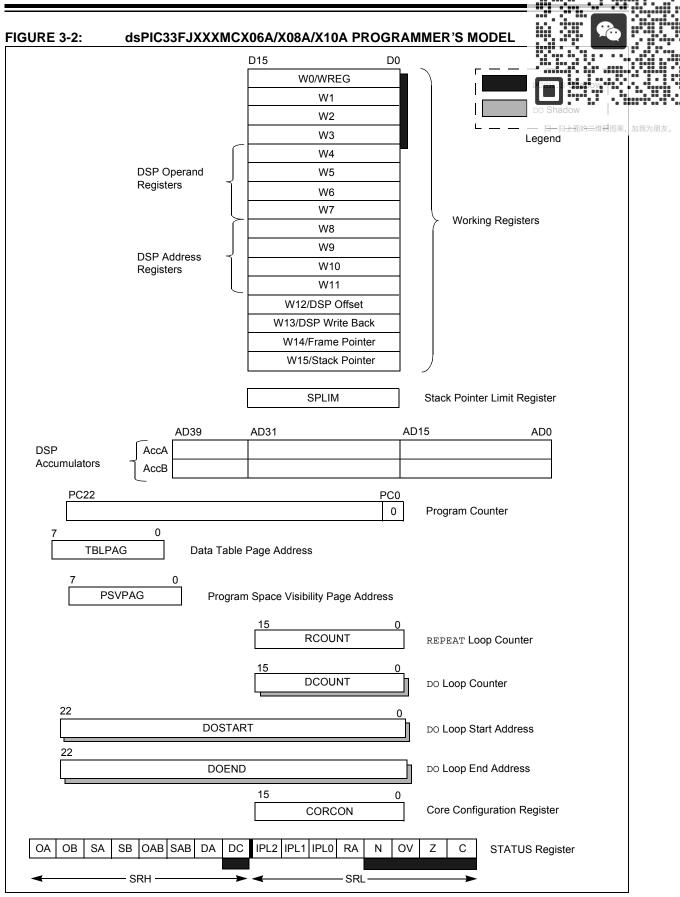
The dsPIC33FJXXXMCX06A/X08A/X10A devices feature a 17-bit by 17-bit, single-cycle multiplier that is shared by both the MCU ALU and DSP engine. The multiplier can perform signed, unsigned and mixed sign multiplication. Using a 17-bit by 17-bit multiplier for 16-bit by 16-bit multiplication not only allows you to perform mixed sign multiplication, it also achieves accurate results for special operations, such as (-1.0) x (-1.0).

The dsPIC33FJXXXMCX06A/X08A/X1 support 16/16 and 32/16 divide operations and integer. All divide instructions operations. They must be executed with loop, resulting in a total execution time of cycles. The divide operation can be interrupted during the divide operation operat

A 40-bit barrel shifter is used to perform up to a 16-bit left or right shift in a single cycle. The barrel shifter can be used by both MCU and DSP instructions.

FIGURE 3-1: dsPIC33FJXXXMCX06A/X08A/X10A CPU CORE BLOCK DIAGRAM





3.4 CPU Control Registers

REGISTER 3-1: SR: CPU STATUS REGISTER

EGISTER 3-	1: SR: CI	SR: CPU STATUS REGISTER									
R-0	R-0	R/C-0	R/C-0	R-0	R/C-0	R -0					
OA	OB	SA ⁽¹⁾	SB ⁽¹⁾	OAB	SAB ⁽⁴⁾	DA	DC				
pit 15							扫一扫上面的14日日				
R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R-0	R/W-0	R/W-0	R/W-0	R/W-0				
	IPL<2:0> ⁽²⁾		RA	N	OV	Z	С				
pit 7				•		·	bit 0				
egend:											
C = Clearable b	bit	R = Readable	bit	U = Unimplen	nented bit, read	l as '0'					
S = Settable bit	t	W = Writable	bit	-n = Value at	POR						
1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown						
	01										
bit 15		ator A Overflow									
		itor A has not o									
pit 14	OB: Accumulator B Overflow Status bit										
	1 = Accumulator B overflowed										
	0 = Accumula	itor B has not o	verflowed								
bit 13	SA: Accumulator A Saturation 'Sticky' Status bit ⁽¹⁾										
		itor A is saturat itor A is not sat		en saturated at	some time						
bit 12	SB: Accumulator B Saturation 'Sticky' Status bit ⁽¹⁾										
		itor B is saturat itor B is not sat		en saturated at	some time						
bit 11	OAB: OA O	B Combined A	ccumulator (Overflow Status	bit						
		itors A or B hav									
pit 10	SAB: SA SI	3 Combined Ac	cumulator 'S	Sticky' Status bit	(4)						
		itors A or B are ccumulator A o		have been saturated	rated at some	time in the pas	t				
oit 9	DA: DO Loop	Active bit									
	1 = DO loop in 0 = DO loop n	1 0									
oit 8	DC: MCU ALU Half Carry/Borrow bit										
	1 = A carry-o	-		(for byte-sized d	lata) or 8th low⊣	order bit (for wo	ord-sized data)				
			th low-order	bit (for byte-size	ed data) or 8th	low-order bit (for word-sized				

- 2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU interrupt priority level. The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
- 3: The IPL<2:0> Status bits are read only when NSTDIS = 1 (INTCON1<15>).
- 4: This bit may be read or cleared (not set). Clearing this bit will clear SA and SB.



REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)

bit 7-5	IPL<2:0>: CPU Interrupt Priority Level Status bits ⁽²⁾	
	111 = CPU interrupt priority level is 7 (15), user interrupts disabled	
	110 = CPU interrupt priority level is 6 (14)	
	101 = CPU interrupt priority level is 5 (13)	
	100 = CPU interrupt priority level is 4 (12)	扫一扫上面的二维码图案,加到
	011 = CPU interrupt priority level is 3 (11)	
	010 = CPU interrupt priority level is 2 (10) 001 = CPU interrupt priority level is 1 (9)	
	000 = CPU interrupt priority level is 0 (8)	
bit 4	RA: REPEAT Loop Active bit	
	1 = REPEAT loop in progress	
	0 = REPEAT loop not in progress	
bit 3	N: MCU ALU Negative bit	
	1 = Result was negative	
	0 = Result was non-negative (zero or positive)	
bit 2	OV: MCU ALU Overflow bit	
	This bit is used for signed arithmetic (2's complement). It indicates an overflow causes the sign bit to change state.	w of the magnitude that
	1 = Overflow occurred for signed arithmetic (in this arithmetic operation)	
	0 = No overflow occurred	
bit 1	Z: MCU ALU Zero bit	
	1 = An operation which affects the Z bit has set it at some time in the past	
	0 = The most recent operation which affects the Z bit has cleared it (i.e., a not	n-zero result)
bit 0	C: MCU ALU Carry/Borrow bit	
	1 = A carry-out from the Most Significant bit of the result occurred	
	0 = No carry-out from the Most Significant bit of the result occurred	

- Note 1: This bit may be read or cleared (not set).
 - 2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU interrupt priority level. The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
 - **3:** The IPL<2:0> Status bits are read only when NSTDIS = 1 (INTCON1<15>).
 - 4: This bit may be read or cleared (not set). Clearing this bit will clear SA and SB.



U-0	U-0	REGISTER 3-2: CORCON: CORE CONTROL REGISTER										
	0-0	U-0	R/W-0	R/W-0	R-0	R-0						
	_	_	US	EDT ⁽¹⁾		DL<2:0>						
it 15												
R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R/W-0	R/W-0	扫 尺为以 面的二维码	8图案,加我》				
SATA	SATB	SATDW	ACCSAT	IPL3 ⁽²⁾	PSV	RND	IF					
oit 7							bit 0					
egend:		C = Clearable	e bit									
R = Readable	bit	W = Writable	bit	-n = Value at	POR	'1' = Bit is set	:					
' = Bit is clear	red	'x = Bit is unk	nown	U = Unimpler	mented bit, rea	id as '0'						
oit 15-13	Unimpleme	nted: Read as '	0'									
oit 12	US: DSP Mu	ultiply Unsigned	Signed Contr	ol bit								
		gine multiplies a	•									
		gine multiplies a										
oit 11	EDT: Early D	00 Loop Termina	ation Control b	_{oit} (1)								
	1 = Terminat 0 = No effec	te executing D0 t	loop at end o	f current loop it	eration							
oit 10-8	DL<2:0>: DC	Loop Nesting	Level Status b	oits								
	111 = 7 do 	oops active										
	•											
	001 = 1 DO 000 = 0 DO											
it 7		Saturation Ena	hle hit									
		lator A saturatio										
		lator A saturatio										
oit 6	SATB: AccB	Saturation Ena	ble bit									
	1 = Accumu	lator B saturatio	n enabled									
	0 = Accumu	lator B saturatio	n disabled									
oit 5	SATDW: Da	ta Space Write	from DSP Eng	gine Saturation	Enable bit							
		ace write satura ace write satura										
oit 4	ACCSAT: A	ccumulator Satu	ration Mode S	Select bit								
		uration (super s										
	0 = 1.31 sat	uration (normal	saturation)									
oit 3	IPL3: CPU I	nterrupt Priority	Level Status	bit 3 ⁽²⁾								
		errupt priority le errupt priority le										
it 2		im Space Visibil										
		, space visible ii										
		space not visit		ce								
oit 1	RND: Round	ding Mode Sele	ct bit									
		conventional) ro		ed								
	0 = Unbiase	d (convergent)	ounding enab	oled								
oit O	•	r Fractional Mul										
		node enabled fo al mode enable										

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU interrupt priority level.

3.5 Arithmetic Logic Unit (ALU)

The dsPIC33FJXXXMCX06A/X08A/X10A ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are 2's complement in nature. Depending on the operation, the ALU may affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the "16-bit MCU and DSC Programmer's *Reference Manual*" (DS70157) for information on the SR bits affected by each instruction.

The dsPIC33FJXXXMCX06A/X08A/X10A CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit-divisor division.

3.5.1 MULTIPLIER

Using the high-speed, 17-bit x 17-bit multiplier of the DSP engine, the ALU supports unsigned, signed or mixed sign operation in several MCU multiplication modes:

- 1. 16-bit x 16-bit signed
- 2. 16-bit x 16-bit unsigned
- 3. 16-bit signed x 5-bit (literal) unsigned
- 4. 16-bit unsigned x 16-bit unsigned
- 5. 16-bit unsigned x 5-bit (literal) unsigned
- 6. 16-bit unsigned x 16-bit signed
- 7. 8-bit unsigned x 8-bit unsigned

3.5.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 1. 32-bit signed/16-bit signed divide
- 2. 32-bit unsigned/16-bit unsigned divide
- 3. 16-bit signed/16-bit signed divide
- 4. 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. 16-bit signed and unsigned DIV instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/ 16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.6 DSP Engine

The DSP engine consists of a high 17-bit multiplier, a barrel shifter an subtracter (with two target accumu saturation logic).



The dsPIC33FJXXXMCX06A/X08A/X10A devices are maxbex, a single-cycle, instruction flow architecture; therefore, concurrent operation of the DSP engine with MCU instruction flow is not possible. However, some MCU ALU and DSP engine resources may be used concurrently by the same instruction (e.g., ED, EDAC).

The DSP engine also has the capability to perform inherent accumulator-to-accumulator operations which require no additional data. These instructions are ADD, SUB and NEG.

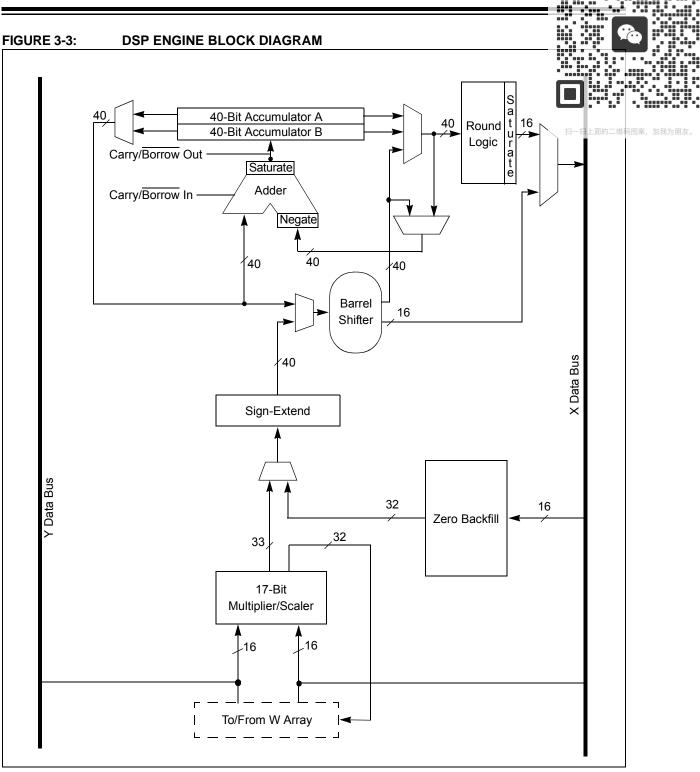
The DSP engine has various options selected through various bits in the CPU Core Control register (CORCON), as listed below:

- 1. Fractional or integer DSP multiply (IF)
- 2. Signed or unsigned DSP multiply (US)
- 3. Conventional or convergent rounding (RND)
- 4. Automatic saturation on/off for AccA (SATA)
- 5. Automatic saturation on/off for AccB (SATB)
- 6. Automatic saturation on/off for writes to data memory (SATDW)
- 7. Accumulator Saturation mode selection (ACCSAT)

Table 2-1 provides a summary of DSP instructions. A block diagram of the DSP engine is shown in Figure 3-3.

SUMMARY				
Instruction	Algebraic Operation	ACC Write Back		
CLR	A = 0	Yes		
ED	$A = (x - y)^2$	No		
EDAC	$A = A + (x - y)^2$	No		
MAC	$A = A + (x \bullet y)$	Yes		
MAC	$A = A + x^2$	No		
MOVSAC	No change in A	Yes		
MPY	$A = x \bullet y$	No		
MPY	$A = x^2$	No		
MPY.N	$A = -x \bullet y$	No		
MSC	$A = A - x \bullet y$	Yes		

TABLE 3-1: DSP INSTRUCTIONS SUMMARY



3.6.1 MULTIPLIER

The 17-bit x 17-bit multiplier is capable of signed or unsigned operation and can multiplex its output using a scaler to support either 1.31 fractional (Q31) or 32-bit integer results. Unsigned operands are zero-extended into the 17th bit of the multiplier input value. Signed operands are sign-extended into the 17th bit of the multiplier input value. The output of the 17-bit x 17-bit multiplier/scaler is a 33-bit value which is sign-extended to 40 bits. Integer data is inherently represented as a signed two's complement value, where the MSb is defined as a sign bit. Generally speaking, the range of an N-bit two's complement integer is -2^{N-1} to $2^{N-1} - 1$. For a 16-bit integer, the data range is -32768 (0x8000) to 32767 (0x7FFF) including 0. For a 32-bit integer, the data range is -2,147,483,648 (0x8000 0000) to 2,147,483,647 (0x7FFF FFFF).

When the multiplier is configured for fractional multiplication, the data is represented as a two's complement fraction, where the MSb is defined as a sign bit and the radix point is implied to lie just after the sign bit (QX format). The range of an N-bit two's complement fraction with this implied radix point is -1.0 to $(1 - 2^{1-N})$. For a 16-bit fraction, the Q15 data range is -1.0 (0x8000) to 0.999969482 (0x7FFF) including 0 and has a precision of 3.01518 x 10⁻⁵. In Fractional mode, the 16 x 16 multiply operation generates a 1.31 product which has a precision of 4.65661 x 10⁻¹⁰.

The same multiplier is used to support the MCU multiply instructions which include integer 16-bit signed, unsigned and mixed sign multiplies.

The MUL instruction may be directed to use byte or word-sized operands. Byte operands will direct a 16-bit result, and word operands will direct a 32-bit result to the specified register(s) in the W array.

3.6.2 DATA ACCUMULATORS AND ADDER/SUBTRACTER

The data accumulator consists of a 40-bit adder/ subtracter with automatic sign extension logic. It can select one of two accumulators (A or B) as its pre-accumulation source and post-accumulation destination. For the ADD and LAC instructions, the data to be accumulated or loaded can be optionally scaled via the barrel shifter prior to accumulation.

3.6.2.1 Adder/Subtracter, Ov Saturation



The adder/subtracter is a 40-bit adder zero input into one side, and either trudata into the other input. In the case

Carry/Borrow input is active-high and the other input is true data (not complemented); where do in the case of the subtraction, the Carry/Borrow input is active-low and the other input is complemented. The adder/subtracter generates Overflow Status bits, SA/SB and OA/OB, which are latched and reflected in the STATUS register:

- Overflow from bit 39: this is a catastrophic overflow in which the sign of the accumulator is destroyed.
- Overflow into guard bits 32 through 39: this is a recoverable overflow. This bit is set whenever all the guard bits are not identical to each other.

The adder has an additional saturation block which controls accumulator data saturation, if selected. It uses the result of the adder, the Overflow Status bits described above and the SAT<A:B> (CORCON<7:6>) and ACCSAT (CORCON<4>) mode control bits to determine when and to what value to saturate.

Six STATUS register bits have been provided to support saturation and overflow; they are:

- 1. OA: AccA overflowed into guard bits
- OB: AccB overflowed into guard bits
- 3. SA:

AccA saturated (bit 31 overflow and saturation) or

AccA overflowed into guard bits and saturated (bit 39 overflow and saturation)

4. SB:

AccB saturated (bit 31 overflow and saturation) or

AccB overflowed into guard bits and saturated (bit 39 overflow and saturation)

5. OAB:

Logical OR of OA and OB

6. SAB:

Logical OR of SA and SB

The OA and OB bits are modified each time data passes through the adder/subtracter. When set, they indicate that the most recent operation has overflowed into the accumulator guard bits (bits 32 through 39). The OA and OB bits can also optionally generate an arithmetic warning trap when they and the corresponding Overflow Trap Flag Enable bits (OVATE, OVBTE) in the INTCON1 register (refer to **Section 7.0 "Interrupt Controller"**) are set. This allows the user to take immediate action, for example, to correct system gain.

The SA and SB bits are modified each time data passes through the adder/subtracter, but can only be cleared by the user. When set, they indicate that the accumulator has overflowed its maximum range (bit 31 for 32-bit saturation or bit 39 for 40-bit saturation) and will be saturated (if saturation is enabled). When saturation is not enabled, SA and SB default to bit 39 overflow, and thus, indicate that a catastrophic overflow has occurred. If the COVTE bit in the INTCON1 register is set, SA and SB bits will generate an arithmetic warning trap when saturation is disabled.

The Overflow and Saturation Status bits can optionally be viewed in the STATUS Register (SR) as the logical OR of OA and OB (in bit OAB), and the logical OR of SA and SB (in bit SAB). This allows programmers to check one bit in the STATUS register to determine if either accumulator has overflowed or one bit to determine if either accumulator has saturated. This would be useful for complex number arithmetic, which typically uses both the accumulators.

The device supports three Saturation and Overflow modes:

1. Bit 39 Overflow and Saturation:

When bit 39 overflow and saturation occurs, the saturation logic loads the maximally positive 9.31 (0x7FFFFFFFF) or maximally negative 9.31 value (0x800000000) into the target accumulator. The SA or SB bit is set and remains set until cleared by the user. This is referred to as 'super saturation' and provides protection against erroneous data or unexpected algorithm problems (e.g., gain calculations).

- 2. Bit 31 Overflow and Saturation: When bit 31 overflow and saturation occurs, the saturation logic then loads the maximally positive 1.31 value (0x007FFFFFF) or maximally negative 1.31 value (0x0080000000) into the target accumulator. The SA or SB bit is set and remains set until cleared by the user. When this Saturation mode is in effect, the guard bits are not used (so the OA, OB or OAB bits are never set).
- 3. Bit 39 Catastrophic Overflow:

The bit 39 Overflow Status bit from the adder is used to set the SA or SB bit, which remains set until cleared by the user. No saturation operation is performed and the accumulator is allowed to overflow (destroying its sign). If the COVTE bit in the INTCON1 register is set, a catastrophic overflow can initiate a trap exception.

3.6.2.2 Accumulator 'Write Back

The MAC class of instructions (with the MPY, MPY.N, ED and EDAC) can option of the high word (bits 3 of the accumulator that is not targeted by the accumulator target by target by the accumulator target by the accumulator target by the accumulator target by targ



the X bus into combined X and Y address 弱起色的情绪的图案, 加我为朋友, following addressing modes are supported:

- 1. W13, Register Direct: The rounded contents of the non-target accumulator are written into W13 as a 1.15 fraction.
- [W13]+ = 2, Register Indirect with Post-Increment: The rounded contents of the non-target accumulator are written into the address pointed to by W13 as a 1.15 fraction. W13 is then incremented by 2 (for a word write).

3.6.2.3 Round Logic

The round logic is a combinational block which performs a conventional (biased) or convergent (unbiased) round function during an accumulator write (store). The Round mode is determined by the state of the RND bit in the CORCON register. It generates a 16-bit, 1.15 data value which is passed to the data space write saturation logic. If rounding is not indicated by the instruction, a truncated 1.15 data value is stored and the least significant word is simply discarded.

Conventional rounding zero-extends bit 15 of the accumulator and adds it to the ACCxH word (bits 16 through 31 of the accumulator). If the ACCxL word (bits 0 through 15 of the accumulator) is between 0x8000 and 0xFFFF (0x8000 included), ACCxH is incremented. If ACCxL is between 0x0000 and 0x7FFF, ACCxH is left unchanged. A consequence of this algorithm is that over a succession of random rounding operations, the value tends to be biased slightly positive.

Convergent (or unbiased) rounding operates in the same manner as conventional rounding, except when ACCxL equals 0x8000. In this case, the Least Significant bit (bit 16 of the accumulator) of ACCxH is examined. If it is '1', ACCxH is incremented. If it is '0', ACCxH is not modified. Assuming that bit 16 is effectively random in nature, this scheme removes any rounding bias that may accumulate.

The SAC and SAC.R instructions store either a truncated (SAC) or rounded (SAC.R) version of the contents of the target accumulator to data memory via the X bus, subject to data saturation (see **Section 3.6.2.4 "Data Space Write Saturation**"). For the MAC class of instructions, the accumulator write-back operation will function in the same manner, addressing combined MCU (X and Y) data space though the X bus. For this class of instructions, the data is always subject to rounding.

3.6.2.4 Data Space Write Saturation

In addition to adder/subtracter saturation, writes to data space can also be saturated – but without affecting the contents of the source accumulator. The data space write saturation logic block accepts a 16-bit, 1.15 fractional value from the round logic block as its input, together with overflow status from the original source (accumulator) and the 16-bit round adder. These inputs are combined and used to select the appropriate 1.15 fractional value as output to write to data space memory.

If the SATDW bit in the CORCON register is set, data (after rounding or truncation) is tested for overflow and adjusted accordingly. For input data greater than 0x007FFF, data written to memory is forced to the maximum positive 1.15 value, 0x7FFF. For input data less than 0xFF8000, data written to memory is forced to the maximum negative 1.15 value, 0x8000. The Most Significant bit of the source (bit 39) is used to determine the sign of the operand being tested.

If the SATDW bit in the CORCON register is not set, the input data is always passed through unmodified under all conditions.

3.6.3 BARREL SHIFTER

The barrel shifter is capable of performant arithmetic or logic right shifts, or up in a single cycle. The source can be DSP accumulators or the X bus (to shifts of register or memory data).



The shifter requires a signed binary value to determine both the magnitude (number of bits) and direction of the shift operation. A positive value shifts the operand right. A negative value shifts the operand left. A value of '0' does not modify the operand.

The barrel shifter is 40 bits wide, thereby obtaining a 40-bit result for DSP shift operations and a 16-bit result for MCU shift operations. Data from the X bus is presented to the barrel shifter between bit positions 16 to 31 for right shifts and between bit positions 0 to 16 for left shifts.

NOTES:



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4.0 MEMORY ORGANIZATION

Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/ X08A/X10A family of devices. However, it is not intended to be a comprereference source. hensive То complement the information in this data sheet, refer to Section 3. "Data Memory" (DS70202) and Section 4. "Program Memory" (DS70203) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

The dsPIC33FJXXXMCX06A/X08A/X10A architecture features separate program and data memory spaces, and buses. This architecture also allows the direct access of program memory from the data space during code execution.

4.1 Program Address Sp

The program address memory dsPIC33FJXXXMCX06A/X08A/X10A instructions. The space is address value derived from either the 23-bit (PC) during program execution, or from



(PC) during program execution, or from table operation or data space remapping as described可能的意志。 "Interfacing Program and Data Memory Spaces".

User access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of TBLRD/TBLWT operations, which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space. Memory usage for the dsPIC33FJXXXMCX06A/X08A/X10A family of devices is shown in Figure 4-1.

	dsPIC33FJ64MCXXXA	dsPIC33FJ128MCXXXA	dsPIC33FJ256MCXXXA	
A	GOTO Instruction	GOTO Instruction	GOTO Instruction	0x000000 - 0x000002
User Memory Space	Reset Address	Reset Address	Reset Address	- 0x000002
	Interrupt Vector Table	Interrupt Vector Table	Interrupt Vector Table	0x0000FE
	Reserved	Reserved	Reserved	0x000100 0x000104
	Alternate Vector Table	Alternate Vector Table	Alternate Vector Table	0x0001FE
	User Program Flash Memory (22K instructions)	User Program Flash Memory (44K instructions)	User Program Flash Memory (88K instructions)	0x000200 0x00ABFE 0x00AC00
len				0x0157FE
User M				0x015800
	Unimplemented (Read '0's)	Unimplemented (Read '0's)	Unimplemented (Read '0's)	0x02ABFE 0x02AC00 0x7FFFFE
Configuration Memory Space	Reserved	Reserved	Reserved	0x800000
	Device Configuration	Device Configuration	Device Configuration	0xF7FFFE 0xF80000
	Registers	Registers	Registers	0xF80017
	Reserved	Reserved	Reserved	0xF80010
S	DEVID (2)	DEVID (2)	DEVID (2)	0xFEFFFE 0xFF0000
				0xFFFFFE

FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33FJXXXMCX06A/X08A/X10A DEVICES



4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-2).

Program memory addresses are always word-aligned on the lower word, and addresses are incremented or decremented by two during code execution. This arrangement also provides compatibility with data memory space addressing and makes it possible to access data in the program memory space.

4.1.2 INTERRUPT AND TRAP

All dsPIC33FJXXXMCX06A/X08A/X10 reserve the addresses between 0x000200 for hard-coded program execution A hardware Reset vector is provided to execution from the default value of the PC on device

Reset to the actual start of code. A GOTO instruction 890%, m33, m

dsPIC33FJXXXMCX06A/X08A/X10A devices also have two interrupt vector tables located from 0x000004 to 0x0000FF and 0x000100 to 0x0001FF. These vector tables allow each of the many device interrupt sources to be handled by separate Interrupt Service Routines (ISRs). A more detailed discussion of the interrupt vector tables is provided in Section 7.1 "Interrupt Vector Table".

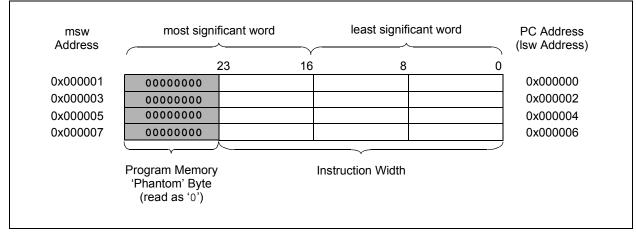


FIGURE 4-2: PROGRAM MEMORY ORGANIZATION

4.2 Data Address Space

The dsPIC33FJXXXMCX06A/X08A/X10A CPU has a separate 16-bit wide data memory space. The data space is accessed using separate Address Generation Units (AGUs) for read and write operations. Data memory maps of devices with different RAM sizes are shown in Figure 4-3 through Figure 4-5.

All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the data space. This arrangement gives a data space address range of 64 Kbytes or 32K words. The lower half of the data memory space (that is, when EA<15> = 0) is used for implemented memory addresses, while the upper half (EA<15> = 1) is reserved for the Program Space Visibility area (see Section 4.6.3 "Reading Data from Program Memory Using Program Space Visibility").

dsPIC33FJXXXMCX06A/X08A/X10A devices implement a total of up to 30 Kbytes of data memory. Should an EA point to a location outside of this area, an all-zero word or byte will be returned.

4.2.1 DATA SPACE WIDTH

The data memory space is organized in byte addressable, 16-bit wide blocks. Data is aligned in data memory and registers as 16-bit words, but all data space EAs resolve to bytes. The Least Significant Bytes of each word have even addresses, while the Most Significant Bytes have odd addresses.

4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC[®] microcontrollers and improve data space memory usage efficiency, the dsPIC33FJXXXMCX06A/X08A/X10A instruction set supports both word and byte operations. As a consequence of byte accessibility, all Effective Address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] will result in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

Data byte reads will read the complete word that contains the byte, using the LSb of any EA to determine which byte to select. The selected byte is placed onto the LSb of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode but separate write lines. Data byte writes only write to the corresponding side of the array or register which matches the byte address. All word accesses must be aligned to Misaligned word data fetches are care must be taken when mixing operations or translating from 8-bit misaligned read or write is attempted trap is generated. If the error occurred on a



instruction underway is completed; if the open red part in the instruction will be executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the Least Significant Byte. The Most Significant Byte is not modified.

A sign-extend instruction (SE) is provided to allow users to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, users can clear the MSb of any W register by executing a zero-extend (ZE) instruction on the appropriate address.

4.2.3 SFR SPACE

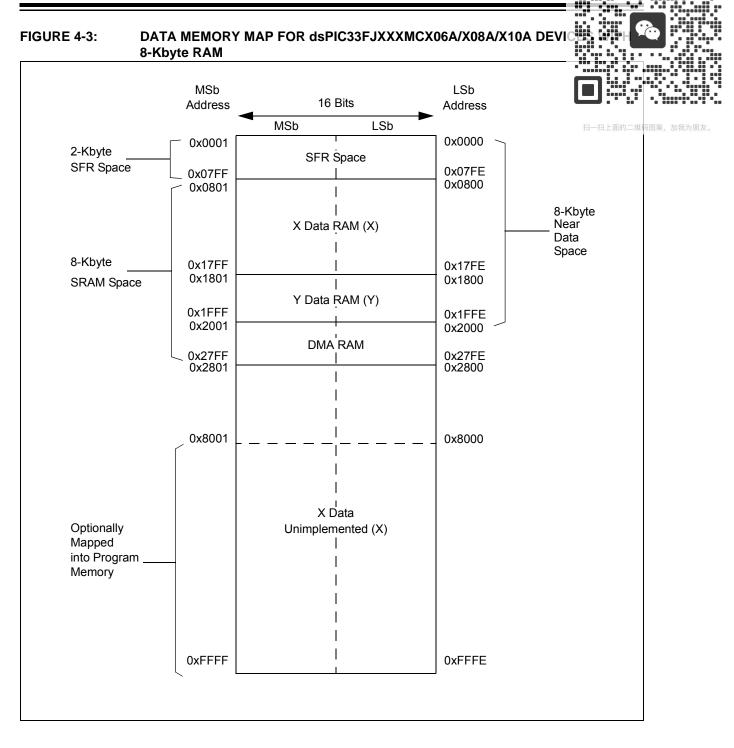
The first 2 Kbytes of the Near Data Space, from 0x0000 to 0x07FF, is primarily occupied by Special Function Registers (SFRs). These are used by the dsPIC33FJXXXMCX06A/X08A/X10A core and peripheral modules for controlling the operation of the device.

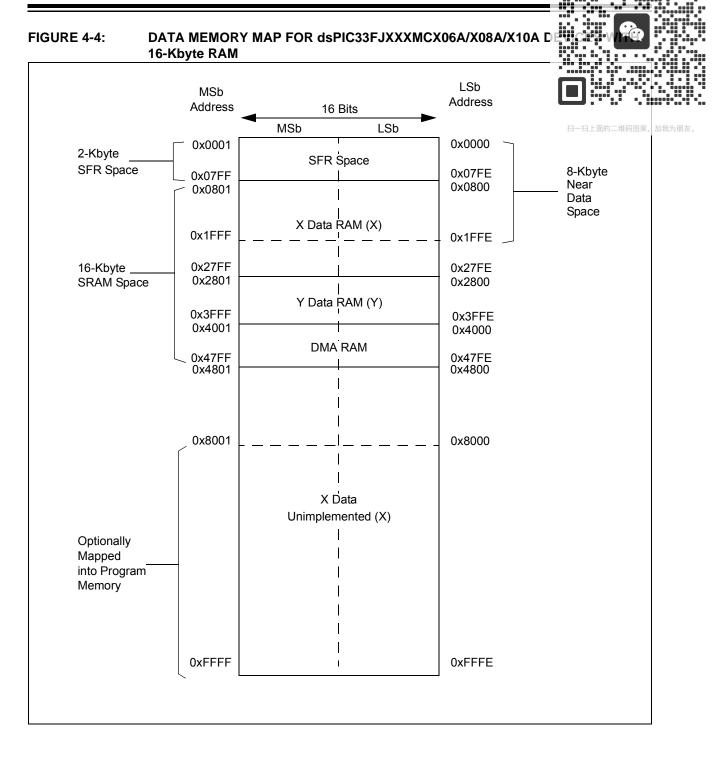
SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'.

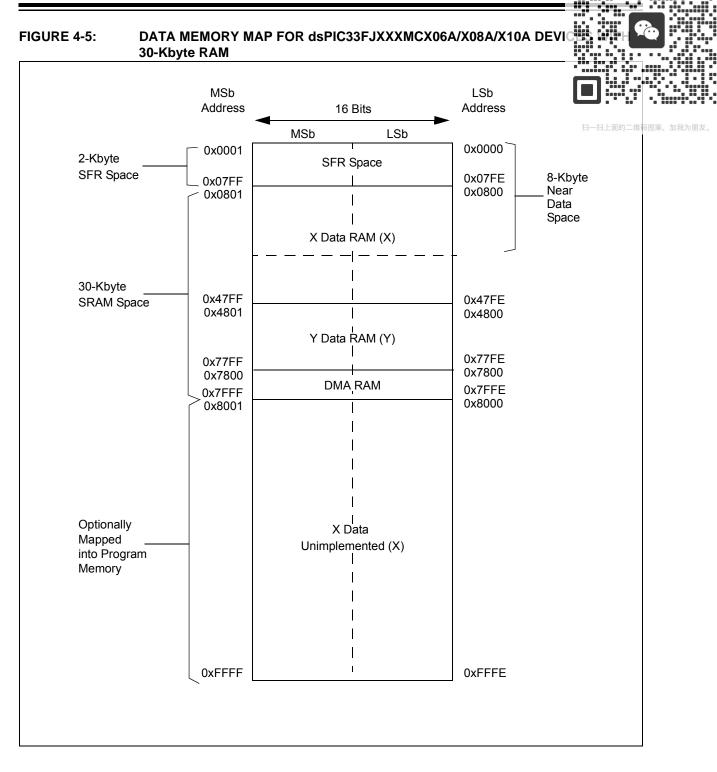
Note: The actual set of peripheral features and interrupts varies by the device. Please refer to the corresponding device tables and pinout diagrams for device-specific information.

4.2.4 NEAR DATA SPACE

The 8-Kbyte area between 0x0000 and 0x1FFF is referred to as the Near Data Space. Locations in this space are directly addressable via a 13-bit absolute address field within all memory direct instructions. Additionally, the whole data space is addressable using MOV instructions, which support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a working register as an Address Pointer.







4.2.5 X AND Y DATA SPACES

The core has two data spaces: X and Y. These data spaces can be considered either separate (for some DSP instructions) or as one unified, linear address range (for MCU instructions). The data spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X data space is used by all instructions and supports all addressing modes. There are separate read and write data buses for X data space. The X read data bus is the read data path for all instructions that view data space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y data space is used in concert with the X data space by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSAC, MPY, MPY.N and MSC) to provide two concurrent data read paths.

Both the X and Y data spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X data space.

All data memory writes, including in DSP instructions, view data space as combined X and Y address space. The boundary between the X and Y data spaces is device-dependent and is not user-programmable.

All Effective Addresses are 16 bits wide and point to bytes within the data space. Therefore, the data space address range is 64 Kbytes, or 32K words, though the implemented memory locations vary by device.

4.2.6 DMA RAM

Every dsPIC33FJXXXMCX06A/X08 contains 2 Kbytes of dual ported DM the end of Y data space. Memory lo data RAM and is in the DMA RA accessible simultaneously by the CPU and the



controller module. DMA RAM is utilized by the DMA maximax. controller to store data to be transferred to various peripherals using DMA, as well as data transferred from various peripherals using DMA. The DMA RAM can be accessed by the DMA controller without having to steal cycles from the CPU.

When the CPU and the DMA controller attempt to concurrently write to the same DMA RAM location, the hardware ensures that the CPU is given precedence in accessing the DMA RAM location. Therefore, the DMA RAM provides a reliable means of transferring DMA data without ever having to stall the CPU.

Addr Addr WREG0 0000 WREG1 0002 WREG2 0004 WREG3 0006 WREG4 0008 WREG5 000A WREG6 000C WREG7 000E WREG8 0010 WREG9 0012 WREG10 0014 WREG11 0016 WREG12 0018 WREG13 001A WREG14 001C WREG15 001E SPLIM 0020 ACCAL 0022 ACCAL 0024 ACCAL 0024 ACCB 0026 ACCB 0028 ACCBU 0020 ACCBU 0020 ACCBU 0020 ACCBU 0020 ACCBU 0026 PCH 0030 OU2E — PCH 0032 PCH 0034	<u>AP</u>		-	-		1	1	1		1		1			
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RCOUNT 0036									Page Addres		<u> </u>			0000	
DCOUNT 0038			-	<u> </u>				am Memor	y Visibility Pa	age Addres	ss Pointer I	Register		0000	
DOSTARTL 003A DOSTARTH 003C — — — — DOENDL 003E				Rep		ounter Regis	ster							XXXX	
DOSTARTH 003C — — — — — DO DOENDL 003E					DCOUN									XXXX	
DOENDL 003E DOENDH 0040 — — — —				1	STARTL<15	1				DOOTA			0	xxxx	
DOENDH 0040 — — — — SR 0042 OA OB SA			-			<u> </u>	_			DOSTA	RTH<5:0>			00xx	
SR 0042 OA OB SA					DENDL<15:	>				D 01			0	xxxx	
			-		DC					-				00xx	
	SB OAE		SAB	DA DL<2:0>	-	IPL2	IPL1	IPL0	RA	N IDL2	OV PSV	Z	С	0000	
CORCON 0044 — — — MODCON 0046 XMODEN YMODEN — —	US EDT	+				SATA	SATB	SATDW	ACCSAT	IPL3	-	RND	IF	0020	
MODCON 0046 XMODEN YMODEN — XMODSRT 0048	-		BW	M<3:0>	XS<15:1>		YVVIV	1<3:0>			200	M<3:0>		0000	
XMODSRT 0048 XMODEND 004A					XE<15:1>								0	xxxx	

Legend:

x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-1:	CPU CORE REGISTERS MAP (CONTINUED)
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SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Afi Resets		•
004C								YS<15:1>								0 0	面的三维码图 xxxx	案,加	我为朋友
004E								YE<15:1>								1	xxxx		l
0050	BREN								XB<14:0>								xxxx		I
0052	_	_						Disab	le Interrupts	s Counter F	Register						xxxx		I
0750	_	_	_	_	_	_	_	—	_		_		_	IW_BSR	IR_BSR	RL_BSR	0000		l
0752	_	_	—	—	—	—	_	—	—	_	—		—	IW_SSR	IR_SSR	RL_SSR	0000		I
	Addr 004C 004E 0050 0052 0750	Addr Bit 15 004C	Addr Bit 15 Bit 14 004C	Addr Bit 15 Bit 14 Bit 13 004C	Addr Bit 15 Bit 14 Bit 13 Bit 12 004C	Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 004C	Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 004C	Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 004C	Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 3 004C	Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 004C	Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 004C	Addr Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 7 004C	Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 004C	Addr Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 004C	Addr Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 004C - - - - - - - - - - - - - - - IW_BSR 004C - - - - - - - - - - - - - - - - - IW_BSR 0050 BREN - IW_BSR<	Addr Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 9 Bit 7 Bit 6 Bit 3 Bit 3 Bit 2 Bit 1 004C	SFR Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 004C	SPR Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0 Addr Addr 004C	SFR Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 2 Bit 1 Bit 0 Aff Resets 004C

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33FJXXXMCX06A/X08A/X10A

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CHANGE NOTIFICATION REGISTER MAP FOR dsPIC33FJXXXMCX10A DEVICES

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	214 O 11	All	
CNEN1	0060	CN15IE	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE	CN9IE	CN8IE	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000	
CNEN2	0062	—	_		—	—	_	_	_	CN23IE	CN22IE	CN21IE	CN20IE	CN19IE	CN18IE	CN17IE	CN16E	面的二维码	劉案 ,
CNPU1	0068	CN15PUE	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE	CN9PUE	CN8PUE	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000	l
CNPU2	006A	—	_	_	—	—	_	_		CN23PUE	CN22PUE	CN21PUE	CN20PUE	CN19PUE	CN18PUE	CN17PUE	CN16PUE	0000	l

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-3: CHANGE NOTIFICATION REGISTER MAP FOR dsPIC33FJXXXMCX08A DEVICES

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNEN1	0060	CN15IE	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE	CN9IE	CN8IE	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	0062	—	_	_	_	_	_	_	_			CN21IE	CN20IE	CN19IE	CN18IE	CN17IE	CN16IE	0000
CNPU1	0068	CN15PUE	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE	CN9PUE	CN8PUE	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	006A	_	_	_	_	_	_	_	_	_	_	CN21PUE	CN20PUE	CN19PUE	CN18PUE	CN17PUE	CN16PUE	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-4: CHANGE NOTIFICATION REGISTER MAP FOR dsPIC33FJXXXMCX06A DEVICES

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNEN1	0060	CN15IE	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE	CN9IE	CN8IE	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	0062	_	_	_	_	_	_	_	_	_	_	CN21IE	CN20IE	_	CN18IE	CN17IE	CN16IE	0000
CNPU1	0068	CN15PUE	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE	CN9PUE	CN8PUE	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	006A		_	_	_	_		_	_	_		CN21PUE	CN20PUE	_	CN18PUE	CN17PUE	CN16PUE	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-2:



TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP

TABLE	4-5:	INTE	RRUPT		ROLLER			AP		-	•					•				
SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets		•••••
INTCON1	0080	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	_	0000		
INTCON2	0082	ALTIVT	DISI	_	—	—	_	—	_	_	_	_	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000		
IFS0	0084	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000		
IFS1	0086	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	IC8IF	IC7IF	AD2IF	INT1IF	CNIF	_	MI2C1IF	SI2C1IF	0000		
IFS2	0088	T6IF	DMA4IF	_	OC8IF	OC7IF	OC6IF	OC5IF	IC6IF	IC5IF	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000		
IFS3	008A	FLTAIF	_	DMA5IF	—	_	QEIIF	PWMIF	C2IF	C2RXIF	INT4IF	INT3IF	T9IF	T8IF	MI2C2IF	SI2C2IF	T7IF	0000		0
IFS4	008C	—	_	_	—	_	_	—	—	C2TXIF	C1TXIF	DMA7IF	DMA6IF	—	U2EIF	U1EIF	FLTBIF	0000		S
IEC0	0094	_	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000		Ť
IEC1	0096	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	IC8IE	IC7IE	AD2IE	INT1IE	CNIE	_	MI2C1IE	SI2C1IE	0000		D
IEC2	0098	T6IE	DMA4IE	_	OC8IE	OC7IE	OC6IE	OC5IE	IC6IE	IC5IE	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000		C
IEC3	009A	FLTAIE	_	DMA5IE	_	—	QEIIE	PWMIE	C2IE	C2RXIE	INT4IE	INT3IE	T9IE	T8IE	MI2C2IE	SI2C2IE	T7IE	0000		25
IEC4	009C	_	_	_	_	_	_	_	_	C2TXIE	C1TXIE	DMA7IE	DMA6IE	_	U2EIE	U1EIE	FLTBIE	0000		$\tilde{\mathbf{\omega}}$
IPC0	00A4	—		T1IP<2:0>	•	—		OC1IP<2:()>	_		IC1IP<2:0>	•	—	11	NT0IP<2:0>	•	4444		33F
IPC1	00A6	—		T2IP<2:0>	•	—		OC2IP<2:()>	_		IC2IP<2:0>	•	—	D	MA0IP<2:0	>	4444		~''
IPC2	00A8	—	l	U1RXIP<2:)>	—		SPI1IP<2:	0>	_		SPI1EIP<2:0)>	—		T3IP<2:0>		4444		
IPC3	00AA	_	_	_	_	_	C	MA1IP<2	:0>	_		AD1IP<2:03	>	_	U	1TXIP<2:0	>	0444		XXXM
IPC4	00AC	_		CNIP<2:0	>	_	_	_	_	_		MI2C1IP<2:0)>	_	S	I2C1IP<2:0	>	4044		\mathbf{X}
IPC5	00AE	_		IC8IP<2:03	>	_		IC7IP<2:0	>	_		AD2IP<2:0	>	_	II	NT1IP<2:0>	>	4444		×
IPC6	00B0	—		T4IP<2:0>	•	—		OC4IP<2:()>	_		OC3IP<2:0	>	—	D	MA2IP<2:0	>	4444		
IPC7	00B2	—	l	U2TXIP<2:()>	—	L	J2RXIP<2:	:0>	_		INT2IP<2:0	>	—		T5IP<2:0>		4444		
IPC8	00B4	_		C1IP<2:0>	>	_	0	C1RXIP<2:	:0>	—		SPI2IP<2:0	>	_	SI	PI2EIP<2:0	>	4444		C
IPC9	00B6	_		IC5IP<2:03	>	_		IC4IP<2:0	>	—		IC3IP<2:0>	•	_	D	MA3IP<2:0	>	4444		×
IPC10	00B8	_		OC7IP<2:0	>	_		OC6IP<2:0)>	—		OC5IP<2:0	>	_	I	IC6IP<2:0>		4444		\mathbf{G}
IPC11	00BA	_		T6IP<2:0>	•	_	C	MA4IP<2	:0>	—	_	_	_	-	0	DC8IP<2:0>	•	4404		Ğ
IPC12	00BC	_		T8IP<2:0>	•	_	N	112C2IP<2	:0>	—		SI2C2IP<2:0)>	_		T7IP<2:0>		4444		×
IPC13	00BE	_	(C2RXIP<2:)>	_	1	INT4IP<2:	0>	_		INT3IP<2:0	>	_		T9IP<2:0>		4444		X06A/
IPC14	00C0	_	—	_	—	_		QEIIP<2:0)>	_		PWMIP<2:0	>	_		C2IP<2:0>		0444	╡	
IPC15	00C2	—		FLTAIP<2:0)>	—	_	—	—	-		DMA5IP<2:0)>	—	—	—	—	4040	╡	6
IPC16	00C4	—	—	—	—	_		U2EIP<2:0)>	—		U1EIP<2:02	>	—	F	LTBIP<2:0	>	0444	1 ∎	ĕ
IPC17	00C6	—	(C2TXIP<2:0)>	—	0	C1TXIP<2:	0>	—		DMA7IP<2:0)>	—	D	MA6IP<2:0	>	4444	1 ∎	X08A
INTTREG	00E0	_	_	_	—		ILR<	3:0>		_			VE	CNUM<6:0>				0000	│	2
	t					1	Deside												- 11	

Legend:

TABLE	4-6:	ТІМЕ	R REGI	STER N	ЛАР														•
SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1		∕4ll Pris€is	
TMR1	0100								Timer1	Register				l				0000	•
PR1	0102									Register 1							扫一扫	上面的亞維亞	图案,加
T1CON	0104	TON		TSIDL						_	TGATE	TCKPS	5<1:0>		TSYNC	TCS		0000	1
TMR2	0106								Timer2	Register								0000	
TMR3HLD	0108						Tim	er3 Holding	Register (fo	r 32-bit time	er operations	only)						xxxx	
TMR3	010A								Timer3	Register								0000	
PR2	010C									Register 2								FFFF	1
PR3	010E									Register 3								FFFF	
T2CON	0110	TON	_	TSIDL	_	_	_	—	_	_	TGATE	TCKPS	S<1:0>	T32	_	TCS	_	0000	
T3CON	0112	TON	_	TSIDL	_	_	_	_	_	_	TGATE	TCKPS	5<1:0>	_	_	TCS	_	0000	
TMR4	0114								Timer4	Register								0000	
TMR5HLD	0116						1	imer5 Holdi	ng Register	(for 32-bit o	perations onl	y)						xxxx	
TMR5	0118								Timer5	Register								0000	
PR4	011A								Period F	Register 4								FFFF	
PR5	011C								Period F	Register 5								FFFF	
T4CON	011E	TON	_	TSIDL	_	_	_	_	_	_	TGATE	TCKPS	S<1:0>	T32	—	TCS	_	0000	
T5CON	0120	TON	_	TSIDL	_	_	_	_	_		TGATE	TCKPS	5<1:0>	_	_	TCS	_	0000	
TMR6	0122								Timer6	Register								0000	
TMR7HLD	0124						1	imer7 Holdi	ng Register	(for 32-bit o	perations onl	y)						xxxx	
TMR7	0126									Register		·						0000	
PR6	0128									Register 6								FFFF	
PR7	012A									Register 7								FFFF	
T6CON	012C	TON	_	TSIDL	_	_	_	_	_	_	TGATE	TCKP	5<1:0>	T32	_	TCS	_	0000	
T7CON	012E	TON	_	TSIDL	_	_	_	_	_		TGATE	TCKPS		_	_	TCS	_	0000	1
TMR8	0130								Timer8	Register								0000	
TMR9HLD	0132						٦	īmer9 Holdi	ng Reaister	(for 32-bit o	perations onl	V)						xxxx	
TMR9	0134								<u> </u>	Register		,,						0000	
PR8	0136									Register 8								FFFF	
PR9	0138									Register 9								FFFF	
T8CON	013A	TON	_	TSIDL	_		_	_	_		TGATE	TCKPS	5<1:0>	T32	_	TCS	_	0000	
T9CON	013C	TON		TSIDL	_						TGATE	TCKP				TCS	_	0000	

TABLE 4	-7: I	NPUT (CAPTU	RE REC	SISTER	MAP													
SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets 扫上面的二维研	
IC1BUF	0140								Input 1 Ca	pture Regis	ter							xxxx	
IC1CON	0142		—	ICSIDL	—	_	—	—	—	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000	
IC2BUF	0144								Input 2 Ca	pture Regis	ter							xxxx	
IC2CON	0146		—	ICSIDL	—	_	—	—	—	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000	
IC3BUF	0148								xxxx										
IC3CON	014A	_	_	ICSIDL	_	_	_	_	_	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000	
IC4BUF	014C							Input 4 Capture Register											
IC4CON	014E	_	_	ICSIDL	_	_	— — ICTMR ICI<1:0> ICOV ICBNE ICM<2:0>											0000	
IC5BUF	0150								Input 5 Ca	pture Regis	ter							xxxx	
IC5CON	0152	_	_	ICSIDL	_	_	_	_	_	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000	
IC6BUF	0154								Input 6 Ca	pture Regis	ter							xxxx	
IC6CON	0156	_	_	ICSIDL	—	_	—	_	_	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000	
IC7BUF	0158								Input 7 Ca	pture Regis	ter							xxxx	
IC7CON	015A	_	_	ICSIDL	—	_	—	_	_	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000	
IC8BUF	015C								Input 8 Ca	pture Regis	ter							xxxx	
IC8CON	015E	_	_	ICSIDL	_	_	_	_	_	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000	

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x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

dsPIC33FJXXXMCX06A/X08A/X10A

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TABLE 4-	8: C SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	ER MA Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B LD Re	All esats
OC1RS	0180			•			-	Out	put Compar	e 1 Second	ary Registe	r	•				X	xxx
OC1R	0182								Output Co	ompare 1 Re	egister						—————————————————————————————————————	n Milli xxxx
OC1CON	0184	_		OCSIDL	_		_	_	—	_	_	—	OCFLT	OCTSEL		OCM<2:0>	0	0000
OC2RS	0186							Out	put Compar	e 2 Second	ary Registe	r					x	xxx
OC2R	0188		Output Compare 2 Register - OCSIDL - - - OCFLT OCTSEL OCM<2:0> Output Compare 3 Secondary Register														x	xxx
OC2CON	018A	—	_	OCSIDL	—	_	_	_	—	—		—	OCFLT	OCTSEL		OCM<2:0>	0	0000
OC3RS	018C		Output Compare 3 Secondary Register Output Compare 3 Register														x	xxx
OC3R	018E		Output Compare 3 Secondary Register Output Compare 3 Register Output Compare 3 Register OCSIDL — — — — OCFLT OCTSEL OCCM<2:0>														x	xxx
OC3CON	0190		_	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL		OCM<2:0>	0	0000
OC4RS	0192							Out	put Compar	e 4 Second	ary Registe	r					x	xxx
OC4R	0194			-	-				Output Co	ompare 4 Re	egister		-		-		x	xxx
OC4CON	0196	—	—	OCSIDL	—	—	—	—	—	—	_	—	OCFLT	OCTSEL		OCM<2:0>	0	0000
OC5RS	0198							Out	put Compar	e 5 Second	ary Registe	r					x	xxx
OC5R	019A								Output Co	ompare 5 Re	egister						x	xxx
OC5CON	019C	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL		OCM<2:0>	0	0000
OC6RS	019E							Out	put Compar	e 6 Second	ary Registe	r					x	xxx
OC6R	01A0							•	Output Co	ompare 6 Re	egister	•		T			x	xxx
OC6CON	01A2	—	_	OCSIDL	—	_	—	—	—	—	—	—	OCFLT	OCTSEL		OCM<2:0>	0	0000
OC7RS	01A4							Out	put Compar	e 7 Second	ary Registe	r					x	xxx
OC7R	01A6			1					Output Co	ompare 7 Re	egister		1	1	n		x	xxx
OC7CON	01A8	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL		OCM<2:0>	0	0000
OC8RS	01AA							Out	put Compar	e 8 Second	ary Registe	r					x	xxx
OC8R	01AC								Output Co	ompare 8 Re	egister			•			x	xxx
OC8CON	01AE	_	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL		OCM<2:0>	0	0000

x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

33FJXXXMCX06A/X08A/X10A

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TABLE 4-9: 8-OUTPUT PWM REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
P1TCON	01C0	PTEN		PTSIDL			_		_		PTOP	S<3:0>		PTCKP	S<1:0>	PTMO	D<1:0>	0000 0000 0000 0000
P1TMR	01C2	PTDIR						F	PWM Time	r Count Val	lue Registe	er						0000 0000 0000 0000
P1TPER	01C4	_						I	PWM Time	Base Peri	od Registe	r						0000 0000 0000 0000
P1SECMP	01C6	SEVTDIR						PW	/M Special	Event Con	npare Regi	ster						0000 0000 0000 0000
PWM1CON1	01C8	_	_	_	_	PMOD4	PMOD3	PMOD2	PMOD1	PEN4H	PEN3H	PEN2H	PEN1H	PEN4L	PEN3L	PEN2L	PEN1L	0000 0000 1111 1111
PWM1CON2	01CA	_	_	_	_		SEVOF	PS<3:0>		_	_	_	_	_	IUE	OSYNC	UDIS	0000 0000 0000 0000
P1DTCON1	01CC	DTBPS	S<1:0>			DTB<	<5:0>			DTAPS	S<1:0>			DTA<	<5:0>			0000 0000 0000 0000
P1DTCON2	01CE	_	_	_	_	_	_	_	_	DTS4A	DTS4I	DTS3A	DTS3I	DTS2A	DTS2I	DTS1A	DTS1I	0000 0000 0000 0000
P1FLTACON	01D0	FAOV4H	FAOV4L	FAOV3H	FAOV3L	FAOV2H	FAOV2L	0000 0000 0000 0000										
P1FLTBCON	01D2	FBOV4H	FBOV4L	FBOV3H	FBOV3L	FBOV2H	FBOV2L	FBOV1H	FBOV1L	FLTBM	_	_	_	FBEN4	FBEN3	FBEN2	FBEN1	0000 0000 0000 0000
P10VDCON	01D4	POVD4H	POVD4L	POVD3H	POVD3L	POVD2H	POVD2L	POVD1H	POVD1L	POUT4H	POUT4L	POUT3H	POUT3L	POUT2H	POUT2L	POUT1H	POUT1L	1111 1111 0000 0000
P1DC1	01D6							PW	M Duty Cyc	cle #1 Regi	ster							0000 0000 0000 0000
P1DC2	01D8							PW	M Duty Cyc	cle #2 Regi	ster							0000 0000 0000 0000
P1DC3	01DA							PW	M Duty Cyc	cle #3 Regi	ster							0000 0000 0000 0000
P1DC4	01DC							PW	I Duty Cyc	cle #4 Regi	ster							0000 0000 0000 0000

Legend: u = uninitialized bit, - = unimplemented, read as '0'

dsPIC33FJXXXMCX06A/X08A/X10A

TABLE 4-10: QEI REGISTER MAP

SFR Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		Re sot			
QEI1CON	01E0	CNTERR	_	QEISIDL	INDX	UPDN	Q	EIM<2:0	>	SWPAB	PCDOUT	TQGATE	TQCKP	S<1:0>	POSRES	TQCS	UPDN_SRC	0000		0000) 00	00
DFLT1CON	01E2	_	—	_		-	IMV<	:1:0>	CEID	QEOUT		QECK<2:0>		_	_	-	_	0000				
POS1CNT	01E4								Po	sition Cou	nter<15:0>							0000	0000	0000) 00	00
MAX1CNT	01E6																	1111	1111	1111	L 11	.11

Legend: u = uninitialized bit, - = unimplemented, read as '0'

TABLE 4-11: I2C1 REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
I2C1RCV	0200	—	_	_	_	_		_	_				I2C1 Recei	ve Register				0000	
I2C1TRN	0202	_	_	_	_	_	_	_	_	1004 Transmit Deviator									
I2C1BRG	0204	—	—	_	—	—		—				Baud Rat	e Generato	r Register				0000	
I2C1CON	0206	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000	
I2C1STAT	0208	ACKSTAT	TRSTAT	—	_		BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	0000	
I2C1ADD	020A	—	—	—	_	—						I2C1 Addre	ss Register					0000	
I2C1MSK	020C	_	—	_	_	_				I2C1 Address Register I2C1 Address Mask Register									

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-12: I2C2 REGISTER MAP

			-																
SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
I2C2RCV	0210	_	—	—	—	—	—	—	—				I2C2 Recei	ve Register				0000	
I2C2TRN	0212	_	_	_	_	_	_	_	_	1000 Transmit Deviator									
I2C2BRG	0214	_	_	_	_	_	_	_				Baud Rat	te Generato	r Register				0000	
I2C2CON	0216	I2CEN	_	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000	
I2C2STAT	0218	ACKSTAT	TRSTAT	_	_	_	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	0000	
I2C2ADD	021A	_	_	_	_	_	_					I2C2 Addre	ess Register					0000	
I2C2MSK	021C	—	_	_	_		—			I2C2 Address Register I2C2 Address Mask Register									

TABLE 4-13: UART1 REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	An Resets	•.'!#	
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	_	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSE	L<1:0>	STSEL	上面的二维码 0000	图案,加	1我为朋友
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN	UTXBF	TRMT	URXIS	EL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110		
U1TXREG	0224	_	_	_	_	_	_	_				UART1	Transmit Re	egister				xxxx		
U1RXREG	0226	_	-	_	—	_	_	_				UART1	Receive Re	egister				0000		
U1BRG	0228							Bau	d Rate Ger	nerator Preso	aler							0000		
Logondu			n Deest		montod ro	ad as 'o' B	a a a t v a lu a	a ara ahaw	n in havad	ممنعهما										i i

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-14: UART2 REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U2MODE	0230	UARTEN		USIDL	IREN	RTSMD		UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEI	L<1:0>	STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN	UTXBF	TRMT	URXISE	EL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	_	_	_	_	_		_				UART2	Transmit R	egister				xxxx
U2RXREG	0236	_	_	_	_	_		_				UART2	Receive R	egister				0000
U2BRG	0238							Baud	Rate Ger	erator Presc	aler							0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-15: SPI1 REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN		SPISIDL	—	—	—	_	_	_	SPIROV	_	—	_		SPITBF	SPIRBF	0000
SPI1CON1	0242	_	_	_	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>		PPRE	<1:0>	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	_	_	_	_	_	_	_	_	_	_	_	FRMDLY	_	0000
SPI1BUF	0248							SPI1 Trans	mit and Red	ceive Buffer	Register							0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-16: SPI2 REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI2STAT	0260	SPIEN		SPISIDL		_	—	_	_	_	SPIROV	—	_			SPITBF	SPIRBF	0000
SPI2CON1	0262		_	_	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>		PPRE	<1:0>	0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	_	_	_		_	_	_	_	_	_	_	FRMDLY	_	0000
SPI2BUF	0268							SPI2 Trans	smit and Re	ceive Buffer	Register							0000

TABLE 4-17: ADC1 REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1		All Fesets
ADC1BUF0	0300								ADC1 Dat	ta Buffer 0								XXXX
AD1CON1	0320	ADON	_	ADSIDL	ADDMABM	_	AD12B	FORI	VI<1:0>	:	SSRC<2:0>		_	SIMSAM	ASAM	SAMP	DƏNƏLi	面的口维码图
AD1CON2	0322	,	VCFG<2:0	>	_	_	CSCNA	CHP	S<1:0>	BUFS	_		SMPI	<3:0>		BUFM	ALTS	0000
AD1CON3	0324	ADRC	_			S	AMC<4:0>						ADCS	<7:0>				0000
AD1CHS123	0326	—	_		_		CH123N	NB<1:0>	CH123SB	—		—	—	—	CH1231	NA<1:0>	CH123SA	0000
AD1CHS0	0328	CH0NB	_	_		С	H0SB<4:0>	•		CH0NA	_	_		(CH0SA<4:0)>		0000
AD1PCFGH ⁽¹⁾	032A	PCFG31	PCFG30	PCFG29	PCFG28	PCFG27	PCFG26	PCFG25	PCFG24	PCFG23	PCFG22	PCFG21	PCFG20	PCFG19	PCFG18	PCFG17	PCFG16	0000
AD1PCFGL	032C	PCFG15	PCFG14	PCFG13	PCFG12	PCFG11	PCFG10	PCFG9	PCFG8	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000
AD1CSSH(1)	032E	CSS31	CSS30	CSS29	CSS28	CSS27	011 PCFG10 PCFG9 PCFG8 F				CSS22	CSS21	CSS20	CSS19	CSS18	CSS17	CSS16	0000
AD1CSSL	0330	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0	0000
AD1CON4	0332	_	_	-	_	-	-	_	_	_	_	_	—	_		DMABL<2:	0>	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Not all ANx inputs are available on all devices. Refer to the device pin diagrams for available ANx inputs.

TABLE 4-18: ADC2 REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADC2BUF0	0340								ADC2 Data	Buffer 0								xxxx
AD2CON1	0360	ADON	—	ADSIDL	ADDMABM	_	AD12B	FOR	VI<1:0>	:	SSRC<2:0>	>	_	SIMSAM	ASAM	SAMP	DONE	0000
AD2CON2	0362		VCFG<2:0>	>	_	_	CSCNA	CHP	S<1:0>	BUFS	_		SMPI	<3:0>		BUFM	ALTS	0000
AD2CON3	0364	ADRC	_	_		S	AMC<4:0>						ADC	S<7:0>				0000
AD2CHS123	0366	_	_	_	_	_	CH123N	IB<1:0>	CH123SB	_	_	_	_	_	CH123N	NA<1:0>	CH123SA	0000
AD2CHS0	0368	CH0NB	_	_	_		CH0S	B<3:0>		CH0NA	_	_	_		CH0S	A<3:0>		0000
Reserved	036A		_		_		—					—	—	_				0000
AD2PCFGL	036C	PCFG15	PCFG14	PCFG13	PCFG12	PCFG11	PCFG10	PCFG9	PCFG8	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000
Reserved	036E		_		_		—					—	—	_				0000
AD2CSSL	0370	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0	0000
AD2CON4	0372	_	_	_	_	_	_	_	_	_	_	_	_	_		DMABL<2:	0>	0000

ile Name Add	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 担一担上	All Res编码
A0CON 0380	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	-	-	AMODE	E<1:0>	—	—	MODE	<1:0>	0000
IAOREQ 0382	FORCE	—	—	_	_	—	—	—	-				IRQSEL<6:0	>			0000
A0STA 0384								ŝ	STA<15:0>								0000
AOSTB 0386	;							S	STB<15:0>								0000
A0PAD 0388	5							F	PAD<15:0>								0000
A0CNT 038A	· —	—	-		_						CNT	<9:0>					0000
A1CON 0380	CHEN	SIZE	DIR	HALF	NULLW		—	-	—	—	AMODE	E<1:0>		—	MODE	<1:0>	0000
A1REQ 038E	FORCE	—	—		_		—	—	—				IRQSEL<6:0	>			0000
A1STA 0390)							5	STA<15:0>								0000
A1STB 0392	2							5	STB<15:0>								0000
1A1PAD 0394								F	PAD<15:0>								0000
A1CNT 0396	i —	_	_	_	_	_					CNT	<9:0>					0000
1A2CON 0398	CHEN	SIZE	DIR	HALF	NULLW	-	—	_	—	_	AMODI	E<1:0>		_	MODE	<1:0>	0000
1A2REQ 039A	FORCE	_	_	_	_	_	_	_	_				IRQSEL<6:0	>			0000
A2STA 0390	;							ŝ	STA<15:0>								0000
A2STB 039E								S	STB<15:0>								0000
A2PAD 03A0)							F	PAD<15:0>								0000
A2CNT 03A2	2 —	_	_	_	_	_					CNT	<9:0>					0000
IA3CON 03A4	CHEN	SIZE	DIR	HALF	NULLW		—	_	_	_	AMODI	E<1:0>		_	MODE	<1:0>	0000
A3REQ 03A6	FORCE	—	—		_		—	—	—				IRQSEL<6:0	>			0000
A3STA 03A8	3							5	STA<15:0>								0000
A3STB 03AA	Λ.							5	STB<15:0>								0000
ABPAD 03AC)							F	PAD<15:0>								0000
MA3CNT 03AE	_	_	_	_	_	_					CNT	<9:0>					0000
MA4CON 03B0	CHEN	SIZE	DIR	HALF	NULLW	_	_	_	_	_	AMODE	E<1:0>	_	_	MODE	<1:0>	0000
AAREQ 03B2	FORCE	_	_	_	_	_	—	-	_				IRQSEL<6:0	>			0000
IA4STA 03B4	ł							Ś	STA<15:0>								0000
IA4STB 03B6	5							S	STB<15:0>								0000
1A4PAD 03B8	3							F	PAD<15:0>								0000
A4CNT 03BA	· -	—	—	—	_	—					CNT	<9:0>					0000
A5CON 03BC	CHEN	SIZE	DIR	HALF	NULLW	-	—	—	_	—	AMODE	E<1:0>	_	—	MODE	<1:0>	0000
1A5REQ 03BE	FORCE	—	—	—	—	_	—	_	_		-		IRQSEL<6:0	>			0000
MA5STA 03C0)								STA<15:0>	-							0000
ASSTB 03C2	2							5	STB<15:0>								0000

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TABLE 4-19: DMA REGISTER MAP (CONTINUED)

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	II I	All Resets
DMA5PAD	03C4								P	AD<15:0>								0000
DMA5CNT	03C6	_	_	_	_	—	—					CNT	<9:0>				扫一扫上	面的 一维码 图
DMA6CON	03C8	CHEN	SIZE	DIR	HALF	NULLW	_	_	_	_	_	AMOD	E<1:0>	_	_	MODE	<1:0>	0000
DMA6REQ	03CA	FORCE	_	_	_	_	_	_	_	_			I	RQSEL<6:0	>			0000
DMA6STA	03CC								S	TA<15:0>								0000
DMA6STB	03CE						STB<15:0> 0000 PAD<15:0> 0000											0000
DMA6PAD	03D0						STB<15:0> 0000 PAD<15:0> 0000											0000
DMA6CNT	03D2	_	_	_	_	_	_					CNT	<9:0>					0000
DMA7CON	03D4	CHEN	SIZE	DIR	HALF	NULLW	_	_	_	_	_	AMOD	E<1:0>	_	_	MODE	<1:0>	0000
DMA7REQ	03D6	FORCE	_	_	_	_	_	_	_	_			I	RQSEL<6:0	>			0000
DMA7STA	03D8								S	TA<15:0>								0000
DMA7STB	03DA								S	TB<15:0>								0000
DMA7PAD	03DC								P	AD<15:0>								0000
DMA7CNT	03DE	_	_	_	_	_	_					CNT	<9:0>					0000
DMACS0	03E0	PWCOL7	PWCOL6	PWCOL5	PWCOL4	PWCOL3	PWCOL2	PWCOL1	PWCOL0	XWCOL7	XWCOL6	XWCOL5	XWCOL4	XWCOL3	XWCOL2	XWCOL1	XWCOL0	0000
DMACS1	03E2	_	_	_	_		LSTCH	1<3:0>		PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0	0000
DSADR	03E4								DS	ADR<15:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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TABLE 4-20:ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0 OR 1

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 扫一扫上i	All Resata
C1CTRL1	0400	—	—	CSIDL	ABAT	—	RE	EQOP<2:0>	>	OPN	MODE<2:0>	>	—	CANCAP	—	—	WIN	0480
C1CTRL2	0402	_	—	_	(-)	—	—	<u> </u>	—	<u> </u>	—	—	1	D!	NCNT<4:0>	>		0000
C1VEC	0404	_	_	—	1	FI	ILHIT<4:0>		1	—			1	ICODE<6:0>	>			0000
C1FCTRL	0406	D	DMABS<2:0>	>			—	<u> </u>	- 7		—	—	1	,	FSA<4:0>			0000
C1FIFO	0408	_	—			FBP<5	5:0>			—	—			FNRB<	<5:0>	;	0000	
C1INTF	040A	_	—	TXBO	TXBP	RXBP	TXWAR	RXWAR	EWARN	IVRIF	WAKIF	ERRIF	—	FIFOIF	RBOVIF	RBIF	TBIF	0000
C1INTE	040C	_	—		/	—	—	—	/	IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE	0000
C1EC	040E	1			TERRCNT	Γ<7:0>				1			RERRCN	T<7:0>				0000
C1CFG1	0410	_				_			$\left[- \right]$	SJW<1:	1:0>			BRP<	.5:0>			0000
C1CFG2	0412	_	WAKFIL	—		—	SE'	G2PH<2:0>	<i>,</i> >	SEG2PHTS	SAM	S	EG1PH<2:	:0>	P	PRSEG<2:0)>	0000
C1FEN1	0414	FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8	FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0	FFFF
C1FMSKSEL1	0418	F7MSK	<<1:0>	F6MSł								0000						
C1FMSKSEL2	041A	F15MSk	K<1:0>	F14MS	SK<1:0>	F13MS	SK<1:0>	F12MS	K<1:0>	F11MSK<	<1:0>	F10MSk	K<1:0>	F9MSK	<1:0>	F8MSI	SK<1:0>	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-21: ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400- 041E							See	edefinition	when WIN	= x							
C1RXFUL1	0420	RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8	RXFUL7	RXFUL6	RXFUL5	RXFUL4	RXFUL3	RXFUL2	RXFUL1	RXFUL0	0000
C1RXFUL2	0422	RXFUL31	RXFUL30	RXFUL29	RXFUL28	RXFUL27	RXFUL26	RXFUL25	RXFUL24	RXFUL23	RXFUL22	RXFUL21	RXFUL20	RXFUL19	RXFUL18	RXFUL17	RXFUL16	0000
C1RXOVF1	0428	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
C1RXOVF2	042A	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000
C1TR01CON	0430	TXEN1	TXABT1	TXLARB1	TXERR1	TXREQ1	RTREN1	TX1PF	RI<1:0>	TXEN0	TXABAT0	TXLARB0	TXERR0	TXREQ0	RTREN0	TX0PF	RI<1:0>	0000
C1TR23CON	0432	TXEN3	TXABT3	TXLARB3	TXERR3	TXREQ3	RTREN3	TX3PF	RI<1:0>	TXEN2	TXABAT2	TXLARB2	TXERR2	TXREQ2	RTREN2	TX2PF	RI<1:0>	0000
C1TR45CON	0434	TXEN5	TXABT5	TXLARB5	TXERR5	TXREQ5	RTREN5	TX5PF	RI<1:0>	TXEN4	TXABAT4	TXLARB4	TXERR4	TXREQ4	RTREN4	TX4PF	RI<1:0>	0000
C1TR67CON	0436	TXEN7	TXABT7	TXLARB7	TXERR7	TXREQ7	RTREN7	TX7PF	RI<1:0>	TXEN6	TXABAT6	TXLARB6	TXERR6	TXREQ6	RTREN6	TX6PF	RI<1:0>	xxxx
C1RXD	0440							EC	AN1 Receiv	ved Data W	ord							xxxx
C1TXD	0442	ECAN1 Transmit Data Word												xxxx				

33FJXXXMCX06A/X08A/X10A

TABLE 4-22: ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1

	1	1	1	τ	1	Т	т `		<u> </u>			1	1	1	1	Т	••••ē	
File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit Ü	Al Rotett
	0400- 041E			<u>.</u>		<u> </u>	<u> </u>		See defin	ition when \	WIN = x					<u>.</u>		
C1BUFPNT1	0420		F3BF	P<3:0>			F2E	3P<3:0>			F1BF	?<3:0>			F0BP	<3:0>		0000
C1BUFPNT2	0422		F7BF	P<3:0>			F6E	3P<3:0>			F5BF	?<3:0>			F4BP	<3:0>		0000
C1BUFPNT3	0424		F11B	P<3:0>			F10	BP<3:0>			F9BF	?<3:0>			F8BP	<3:0>		0000
C1BUFPNT4	0426		F15B	P<3:0>			F14[BP<3:0>			F13B	P<3:0>			F12BF	P<3:0>		0000
C1RXM0SID	0430				SID-	<10:3>					SID<2:0>			MIDE	—	EID<	17:16>	xxxx
C1RXM0EID	0432				EID•	<15:8>							EID<	7:0>				xxxx
C1RXM1SID	0434				SID-	<10:3>					SID<2:0>		—	MIDE	—	EID<	17:16>	xxxx
C1RXM1EID	0436				EID<	<15:8>							EID<	7:0>		-		xxxx
C1RXM2SID	0438				SID<	<10:3>					SID<2:0>		—	MIDE	—	EID<	17:16>	xxxx
C1RXM2EID	043A				EID<	<15:8>							EID<	7:0>				xxxx
C1RXF0SID	0440				SID<	<10:3>					SID<2:0>		—	EXIDE	—	EID<	17:16>	xxxx
C1RXF0EID	0442				EID<	<15:8>							EID<	7:0>				xxxx
C1RXF1SID	0444					<10:3>					SID<2:0>		—	EXIDE	—	EID<	17:16>	XXXX
C1RXF1EID	0446					<15:8>							EID<	-				XXXX
C1RXF2SID	0448					<10:3>		<u> </u>			SID<2:0>		—	EXIDE	—	EID<	17:16>	XXXX
C1RXF2EID	044A					<15:8>							EID<					xxxx
C1RXF3SID	044C					<10:3>					SID<2:0>			EXIDE	-	EID<	17:16>	XXXX
C1RXF3EID	044E					<15:8>							EID<				17.10	XXXX
C1RXF4SID	0450				-	<10:3>					SID<2:0>		-	EXIDE	—	EID<	17:16>	XXXX
C1RXF4EID	0452					<15:8>							EID<				47.40	XXXX
C1RXF5SID	0454 0456				-	<10:3> <15:8>				_	SID<2:0>		EID<	EXIDE	—	EID<	17:16>	XXXX
C1RXF5EID	0456					<10:3>					SID<2:0>			EXIDE	_	EID-	17:16>	xxxx xxxx
C1RXF6EID	0458 045A					<15:8>				-	310~2.02		EID<		_		17.10-	xxxx
C1RXF7SID	045C					<10:3>					SID<2:0>			EXIDE	_	FID<	17:16>	XXXX
C1RXF7EID	045E					<15:8>					010-2.02		EID<					xxxx
C1RXF8SID	0460					<10:3>				+	SID<2:0>		_	EXIDE	_	EID<	17:16>	XXXX
C1RXF8EID	0462					<15:8>				+			EID<			1 2.2 .		XXXX
C1RXF9SID	0464					<10:3>				-	SID<2:0>			EXIDE	_	EID<	17:16>	xxxx
C1RXF9EID	0466				-	<15:8>				-			EID<			ı	-	xxxx
C1RXF10SID	0468	1			SID	<10:3>				1	SID<2:0>		—	EXIDE	_	EID<	17:16>	xxxx
C1RXF10EID	046A	1			EID	<15:8>				1			EID<	7:0>				xxxx



TABLE 4-22: ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 (CONTINUED)

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	, Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All	
	, tutul	Die io	BRIT	Bit IO	Dit 12	Bit II	Bit it	Bitto	Bitto	Bitt	Bitt	Bitto	BRA	BRO	DICE	Dit i		Resets 扫上面的三维码	图案,加我为朋友。
C1RXF11SID	046C				SID<	:10:3>					SID<2:0>		—	EXIDE	—	EID<1	17:16>	xxxx	
C1RXF11EID	046E				EID<	:15:8>							EID<	7:0>				xxxx	
C1RXF12SID	0470				SID<	:10:3>					SID<2:0>		_	EXIDE	_	EID<1	17:16>	xxxx	
C1RXF12EID	0472				EID<	:15:8>							EID<	7:0>				xxxx	
C1RXF13SID	0474				SID<	:10:3>					SID<2:0>		_	EXIDE	_	EID<1	17:16>	xxxx	
C1RXF13EID	0476				EID<	:15:8>							EID<	7:0>				xxxx	
C1RXF14SID	0478				SID<	:10:3>					SID<2:0>		—	EXIDE	—	EID<1	17:16>	xxxx	l l s
C1RXF14EID	047A				EID<	:15:8>							EID<	7:0>				xxxx	
C1RXF15SID	047C				SID<	:10:3>					SID<2:0>		—	EXIDE	_	EID<1	17:16>	xxxx	
C1RXF15EID	047E				EID<	:15:8>							EID<	7:0>				xxxx	

TABLE 4-2	3: E	CAN2 R	EGISTE	RMAP	WHEN W	VIN (C10	CTRL<0	>) = 0 (OR 1 F	OR dsPl	C33FJ	хххмс	708A/7	710A DE				
File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1		ali Pesets
C2CTRL1	0500	—	_	CSIDL	ABAT	—	R	EQOP<2:0	>	OPN	/ODE<2:0)>	_	CANCAP	—	_	WIN	0480
C2CTRL2	0502	_	_	_	_	_	-	_	—	_	—	—		D	NCNT<4:0)>	扫一扫上	面的口油和
C2VEC	0504	—	_	_		FI	LHIT<4:0>			_				ICODE<6:0)>			0000
C2FCTRL	0506	[MABS<2:0	>	—	_	_	_	—	_	—	—			FSA<4:0>			0000
C2FIFO	0508	—	—			FBP<5	:0>			_	—			FNRE	3<5:0>			0000
C2INTF	050A	_	_	ТХВО	TXBP	RXBP	TXWAR	RXWAR	EWARN	IVRIF	WAKIF	ERRIF	_	FIFOIF	RBOVIF	RBIF	TBIF	0000
C2INTE	050C	_	_	_	_	_	_	_	_	IVRIE	WAKIE	ERRIE	_	FIFOIE	RBOVIE	RBIE	TBIE	0000
C2EC	050E				TERRCN	T<7:0>							RERRC	NT<7:0>				0000
C2CFG1	0510	_	_	_	_	_	_	_	_	SJW<	1:0>			BRP	<5:0>			0000
C2CFG2	0512	_	WAKFIL	_	_	_	SE	G2PH<2:0)>	SEG2PHTS	SAM	SI	EG1PH<2	:0>	Р	RSEG<2:0)>	0000
C2FEN1	0514	FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8	FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0	FFFF
C2FMSKSEL1	0518	F7MSI	<<1:0>	F6MSI	K<1:0>	F5MSł	<<1:0>	F4MS	K<1:0>	F3MSK	<1:0>	F2MSł	<<1:0>	F1MSł	<<1:0>	F0MS	K<1:0>	0000
C2FMSKSEL2	051A	F15MS	K<1:0>	F14MS	K<1:0>	F13MS	K<1:0>	F12MS	SK<1:0>	F11MSK	<1:0>	F10MS	K<1:0>	F9MSł	<<1:0>	F8MS	K<1:0>	0000

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JXXXMCX06A/X08A/X10A

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-24: ECAN2 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0 FOR dsPIC33FJXXXMC708A/710A DEVICES

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets				
	0500- 051E							See	e definition	when WIN	= x											
C2RXFUL1	0520	RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8	RXFUL7	RXFUL6	RXFUL5	RXFUL4	RXFUL3	RXFUL2	RXFUL1	RXFUL0	0000				
C2RXFUL2	0522	RXFUL31	RXFUL30	RXFUL29	RXFUL28	RXFUL27	RXFUL26	RXFUL25	RXFUL24	RXFUL23	RXFUL22	RXFUL21	RXFUL20	RXFUL19	RXFUL18	RXFUL17	RXFUL16	0000				
C2RXOVF1	0528	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF09	RXOVF08	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000				
C2RXOVF2	052A	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000				
C2TR01CON	0530	TXEN1	TX ABAT1	TX LARB1	TX ERR1	TX REQ1	RTREN1	TX1PF	RI<1:0>	TXEN0	TX ABAT0	TX LARB0	TX ERR0	TX REQ0	RTREN0	TX0PF	RI<1:0>	0000				
C2TR23CON	0532	TXEN3	TX ABAT3	TX LARB3	TX ERR3	TX REQ3	RTREN3	TX3PF	RI<1:0>	TXEN2	TX ABAT2	TX LARB2	TX ERR2	TX REQ2	RTREN2	TX2PF	RI<1:0>	0000				
C2TR45CON	0534	TXEN5	TX ABAT5	TX LARB5	TX ERR5	TX REQ5	RTREN5	TX5PF	RI<1:0>	TXEN4	TX ABAT4	TX LARB4	TX ERR4	TX REQ4	RTREN4	TX4PF	RI<1:0>	0000				
C2TR67CON	0536	TXEN7	TX ABAT7	TX LARB7	TX ERR7	TX REQ7	RTREN7	TX7PF	RI<1:0>	TXEN6	TX ABAT6	TX LARB6	TX ERR6	TX REQ6	RTREN6	TX6PF	RI<1:0>	xxxx				
C2RXD	0540							EC	AN2 Recie	ved Data W	ord			xxxx								
C2TXD	0542							EC	CAN2 Trans	mit Data W	ord							xxxx				



File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 扫一扫	All Besets
	0500- 051E	I			I			Se	e definitio	n when WIN	= x	1	1		1	1		
C2BUFPNT1	0520		F3BF	P<3:0>			F2BF	P<3:0>			F1BP	<3:0>			F0BF	P<3:0>		0000
C2BUFPNT2	0522		F7BF	P<3:0>			F6BF	P<3:0>			F5BP	<3:0>			F4BF	?<3:0>		0000
C2BUFPNT3	0524		F11B	P<3:0>			F10B	P<3:0>			F9BP	<3:0>			F8BP	°<3:0>		0000
C2BUFPNT4	0526		F15B	P<3:0>			F14B	P<3:0>			F13BF	P<3:0>			F12B	P<3:0>		0000
C2RXM0SID	0530				SID<	10:3>					SID<2:0>		_	MIDE	—	EID<	17:16>	xxxx
C2RXM0EID	0532				EID<	15:8>							EID	<7:0>		_		xxxx
C2RXM1SID	0534				SID<	10:3>					SID<2:0>		—	MIDE	—	EID<	17:16>	xxxx
C2RXM1EID	0536				EID<	15:8>							EID	<7:0>				xxxx
C2RXM2SID	0538				SID<	10:3>					SID<2:0>			MIDE	—	EID<	17:16>	xxxx
C2RXM2EID	053A				EID<	15:8>							EID	<7:0>	•			xxxx
C2RXF0SID	0540				SID<	10:3>					SID<2:0>			EXIDE	—	EID<	17:16>	xxxx
C2RXF0EID	0542				EID<	15:8>							EID	<7:0>				xxxx
C2RXF1SID	0544				SID<	10:3>					SID<2:0>		—	EXIDE	—	EID<	17:16>	xxxx
C2RXF1EID	0546				EID<	15:8>							EID	<7:0>		1		xxxx
C2RXF2SID	0548				SID<	10:3>					SID<2:0>			EXIDE	—	EID<	17:16>	xxxx
C2RXF2EID	054A				EID<	15:8>							EID	<7:0>		1		xxxx
C2RXF3SID	054C				SID<						SID<2:0>			EXIDE		EID<	17:16>	xxxx
C2RXF3EID	054E				EID<								EID	<7:0>				XXXX
C2RXF4SID	0550				SID<						SID<2:0>			EXIDE	—	EID<	17:16>	XXXX
C2RXF4EID	0552				EID<								EID	<7:0>	1	r		XXXX
C2RXF5SID	0554				SID<						SID<2:0>			EXIDE	—	EID<	17:16>	XXXX
C2RXF5EID	0556				EID<								EID	<7:0>	1	1		xxxx
C2RXF6SID	0558				SID<						SID<2:0>		—	EXIDE	—	EID<'	17:16>	XXXX
C2RXF6EID	055A				EID<								EID	<7:0>				XXXX
C2RXF7SID	055C				SID<						SID<2:0>		—	EXIDE		EID<'	17:16>	XXXX
C2RXF7EID	055E				EID<									<7:0>				XXXX
C2RXF8SID	0560				SID<						SID<2:0>		_	EXIDE	—	EID<'	17:16>	XXXX
C2RXF8EID	0562				EID<									<7:0>				XXXX
C2RXF9SID	0564				SID<						SID<2:0>		-	EXIDE	—	EID<'	17:16>	XXXX
C2RXF9EID	0566				EID<						0.0.0		EID	<7:0>				XXXX
C2RXF10SID	0568 056A				SID< EID<						SID<2:0>		—	EXIDE <7:0>	—	EID<	17:16>	XXXX

TABLE 4-25: ECAN2 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 FOR dsPIC33FJXXXMC708A/710A DEVICES

TABLE 4-25: ECAN2 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 FOR dsPIC33FJXXXMC708A/710A DEVICES (CONTINUE)

							-	· · ·							-		<u></u>
File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	4II Restats
C2RXF11SID	056C				SID<	10:3>					SID<2:0>		—	EXIDE	—	EID<17:16>	xxxx
C2RXF11EID	056E				EID<	15:8>							EID<	:7:0>		扫-	一扫上面的云线码
C2RXF12SID	0570				SID<	10:3>					SID<2:0>		—	EXIDE	_	EID<17:16>	xxxx
C2RXF12EID	0572				EID<	15:8>							EID<	:7:0>			xxxx
C2RXF13SID	0574				SID<	10:3>					SID<2:0>		_	EXIDE	_	EID<17:16>	xxxx
C2RXF13EID	0576				EID<	15:8>							EID<	<7:0>			xxxx
C2RXF14SID	0578				SID<	10:3>					SID<2:0>		_	EXIDE		EID<17:16>	xxxx
C2RXF14EID	057A				EID<	15:8>							EID<	<7:0>			xxxx
C2RXF15SID	057C				SID<	10:3>					SID<2:0>		—	EXIDE	_	EID<17:16>	xxxx
C2RXF15EID	057E				EID<	15:8>							EID<	<7:0>			xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-26: PORTA REGISTER MAP⁽¹⁾

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	02C0	TRISA15	TRISA14	_		_	TRISA10	TRISA9		TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	C6FF
PORTA	02C2	RA15	RA14	_	_	_	RA10	RA9	_	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx
LATA	02C4	LATA15	LATA14	_	_	_	LATA10	LATA9	_	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	XXXX
ODCA ⁽²⁾	06C0	ODCA15	ODCA14	—	-	-	—	_	-		_	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for high pin count devices.

Note 1: The actual set of I/O port pins varies from one device to another. Please refer to the corresponding pinout diagrams.

TABLE 4-27: PORTB REGISTER MAP⁽¹⁾

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C6	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	02C8	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	02CA	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for high pin count devices.

Note 1: The actual set of I/O port pins varies from one device to another. Please refer to the corresponding pinout diagrams.



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TABLE 4-28: PORTC REGISTER MAP⁽¹⁾

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets 日上面的二维码	图案,
TRISC	02CC	TRISC15	TRISC14	TRISC13	TRISC12	_		—	—		—		TRISC4	TRISC3	TRISC2	TRISC1		F01E	
PORTC	02CE	RC15	RC14	RC13	RC12	_	_	_	_	_	_	_	RC4	RC3	RC2	RC1	_	xxxx	
LATC	02D0	LATC15	LATC14	LATC13	LATC12	_		-	-		—		LATC4	LATC3	LATC2	LATC1		xxxx	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for high pin count devices.

Note 1: The actual set of I/O port pins varies from one device to another. Please refer to the corresponding pinout diagrams.

TABLE 4-29: PORTD REGISTER MAP⁽¹⁾

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISD	02D2	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FFFF
PORTD	02D4	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
LATD	02D6	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
ODCD	06D2	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal for high pin count devices.

Note 1: The actual set of I/O port pins varies from one device to another. Please refer to the corresponding pinout diagrams.

TABLE 4-30: PORTE REGISTER MAP⁽¹⁾

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISE	02D8	_	_	_	_	_		TRISE9	TRISE8	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	01FF
PORTE	02DA	_	—	_	—	—	_	RE9	RE8	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
LATE	02DC	_	_	_	_	_	_	LATE9	LATE8	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal for high pin count devices.

Note 1: The actual set of I/O port pins varies from one device to another. Please refer to the corresponding pinout diagrams.

TABLE 4-31: PORTF REGISTER MAP⁽¹⁾

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	02DE	_	-	TRISF13	TRISF12	—	—	—	TRISF8	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	31FF
PORTF	02E0	_	_	RF13	RF12	_	_	_	RF8	RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
LATF	02E2	-	—	LATF13	LATF12		_		LATF8	LATF7	LATF6	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
ODCF	06DE	_	_	ODCF13	ODCF12	_	_	_	ODCF8	ODCF7	ODCF6	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal for high pin count devices.

Note 1: The actual set of I/O port pins varies from one device to another. Please refer to the corresponding pinout diagrams.



TABLE 4-32: PORTG REGISTER MAP⁽¹⁾

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit	All Nëseta	
TRISG	02E4	TRISG15	TRISG14	TRISG13	TRISG12		—	TRISG9	TRISG8	TRISG7	TRISG6		_	TRISG3	TRISG2	TRISG1	TRISG0	F3CF	
PORTG	02E6	RG15	RG14	RG13	RG12	_	_	RG9	RG8	RG7	RG6	_	_	RG3	RG2	RG1	RG0 ^{[3-1}	日上面的二维码 XXXX	图案,
LATG	02E8	LATG15	LATG14	LATG13	LATG12	_	_	LATG9	LATG8	LATG7	LATG6	_	_	LATG3	LATG2	LATG1	LATG0	xxxx]
ODCG	06E4	ODCG15	ODCG14	ODCG13	ODCG12	_	—	ODCG9	ODCG8	ODCG7	ODCG6	_		ODCG3	ODCG2	ODCG1	ODCG0	0000	

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal for high pin count devices.

Note 1: The actual set of I/O port pins varies from one device to another. Please refer to the corresponding pinout diagrams.

TABLE 4-33: SYSTEM CONTROL REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	0740	TRAPR	IOPUWR	—	—	—	—	—	VREGS	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	xxxx(1)
OSCCON	0742	_	(COSC<2:0>	>	_	1	NOSC<2:0	>	CLKLOCK	_	LOCK		CF	_	LPOSCEN	OSWEN	₀₃₀₀ (2)
CLKDIV	0744	ROI	[DOZE<2:0>	>	DOZEN	F	RCDIV<2:0)>	PLLPOS	T<1:0>	_		F	PLLPRE<4:	:0>		3040
PLLFBD	0746	_	_	_	_	_	_	_	PLLDIV<8:0>					0030				
OSCTUN	0748	_	-	_		—	_	_		—	—			TUN	l<5:0>			0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: RCON register Reset values dependent on type of Reset.

2: OSCCON register Reset values dependent on the FOSC Configuration bits and type of Reset.

TABLE 4-34: NVM REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0760	WR	WREN	WRERR	—	-	—	—	_	—	ERASE	_	—		NVMO	P<3:0>		0000(1)
NVMKEY	0766	_	—	_	_	-	_		_				NVMKE	Y<7:0>				0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset value shown is for POR only. Value on other Reset states is dependent on the state of memory write or erase operations at the time of Reset.

TABLE 4-35: PMD REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD	PWMMD		I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	C2MD	C1MD	AD1MD	0000
PMD2	0772	IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0774	T9MD	T8MD	T7MD	T6MD	—	—	—	—	_	_	—	-	_	_	I2C2MD	AD2MD	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for high pin count devices.

4.2.7 SOFTWARE STACK

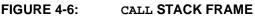
In addition to its use as a working register, the W15 register in the dsPIC33FJXXXMCX06A/X08A/X10A devices is also used as a software Stack Pointer. The Stack Pointer always points to the first available free word and grows from lower to higher addresses. It pre-decrements for stack pops and post-increments for stack pushes, as shown in Figure 4-6. For a PC push during any CALL instruction, the MSb of the PC is zero-extended before the push, ensuring that the MSb is always clear.

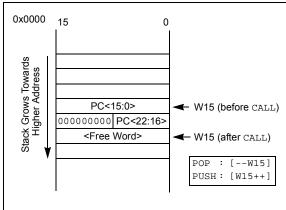
Note:	A PC push during exception processing
	concatenates the SRL register to the MSb
	of the PC prior to the push.

The Stack Pointer Limit register (SPLIM) associated with the Stack Pointer sets an upper address boundary for the stack. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM<0> is forced to '0' because all stack operations must be word-aligned. Whenever an EA is generated using W15 as a source or destination pointer, the resulting address is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal and a push operation is performed, a stack error trap will not occur. The stack error trap will occur on a subsequent push operation. Thus, for example, if it is desirable to cause a stack error trap when the stack grows beyond address 0x2000 in RAM, initialize the SPLIM with the value 0x1FFE.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0x0800. This prevents the stack from interfering with the Special Function Register (SFR) space.

A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.





4.2.8 DATA RAM PROTECT

The dsPIC33FJXXXMCX06A/X08 to be videously support data RAM protection features of the relation of the protected with Boot and Secure Code BSRAM (Secure RAM segment for BS) is accessible



4.3 Instruction Addressing Modes

The addressing modes in Table 4-36 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions are somewhat different from those in the other instruction types.

4.3.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire data space.

4.3.2 MCU INSTRUCTIONS

The 3-operand MCU instructions are of the following form:

Operand 3 = Operand 1 < function> Operand 2

where Operand 1 is always a working register (i.e., the addressing mode can only be Register Direct) which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

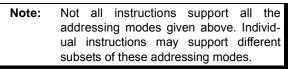




TABLE 4-36: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description	
File Register Direct	The address of the file register is specified explicitly.	
Register Direct	The contents of a register are accessed directly.	
Register Indirect	The contents of Wn forms the EA.	
Register Indirect Post-Modified	The contents of Wn forms the EA. Wn is post-modified (incremented or decremented) by a constant value.	世的国亲,加我为朋友。
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.	
Register Indirect with Register Offset	The sum of Wn and Wb forms the EA.	
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.	

4.3.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions and the DSP accumulator class of instructions provide a greater degree of addressing flexibility than other instructions. In addition to the Addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note:	For the MOV instructions, the addressing
	mode specified in the instruction can differ
	for the source and destination EA.
	However, the 4-bit Wb (register offset)
	field is shared between both source and
	destination (but typically only used by
	one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.3.4 MAC INSTRUCTIONS

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY. N, MOVSAC and MSC), also referred to as MAC instructions, utilize a simplified set of addressing modes to allow the user to effectively manipulate the Data Pointers through register indirect tables.

The 2-source operand prefetch registers must be members of the set {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 will always be directed to the Y AGU. The Effective Addresses generated (before and after modification) must, therefore, be valid addresses within X data space for W8 and W9, and Y data space for W10 and W11.

Note: Register Indirect with Register Offset Addressing mode is only available for W9 (in X space) and W11 (in Y space).

In summary, the following addressing modes are supported by the ${\tt MAC}$ class of instructions:

- · Register Indirect
- · Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.3.5 OTHER INSTRUCTIONS

Besides the various addressing modes outlined above, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ADD Acc, the source of an operand or result is implied by the opcode itself. Certain operations, such as NOP, do not have any operands.

4.4 Modulo Addressing

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

dsPIC33FJXXXMCX06A/X08

Modulo Addressing can operate in either data or program space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into program space) and Y data spaces. Modulo Addressing can operate on any W register pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing, since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can only be configured to operate in one direction, as there are certain restrictions on the buffer start address (for incrementing buffers) or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers which have a power-of-2 length. As these buffers satisfy the start and end address criteria, they may operate in a bidirectional mode (i.e., address boundary checks will be performed on both the lower and upper address boundaries).

4.4.1 START AND END ADDRESS

FIGURE 4-7:

The Modulo Addressing scheme requires that a starting and ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

Note:	Y space Modulo Addressing EA calcula-
	tions assume word-sized data (LSb of
	every EA is always clear).

The length of a circular buffer is not d is determined by the difference corresponding start and end address possible length of the circular buffer (64 Kbytes).

4.4.2 W ADDRESS REGISTER 由上面的二维码图案,加我为朋友。 SELECTION

The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags as well as a W register field to specify the W Address registers. The XWM and YWM fields select which registers will operate with Modulo Addressing. If XWM = 15, X RAGU and X WAGU Modulo Addressing are disabled. Similarly, if YWM = 15, Y AGU Modulo Addressing is disabled.

The X Address Space Pointer W register (XWM) to which Modulo Addressing is to be applied is stored in MODCON<3:0> (see Table 4-1). Modulo Addressing is enabled for X data space when XWM is set to any value other than 15 and the XMODEN bit is set at MODCON<15>.

The Y Address Space Pointer W register (YWM) to which Modulo Addressing is to be applied is stored in MODCON<7:4>. Modulo Addressing is enabled for Y data space when YWM is set to any value other than 15 and the YMODEN bit is set at MODCON<14>.

Byte MOV #0x1100, W0 Address MOV W0, XMODSRT ;set modulo start address MOV #0x1163, W0 ;set modulo end address MOV WO. MODEND MOV #0x8001, W0 0x1100 ;enable W1, X AGU for modulo MOV W0, MODCON #0x0000, W0 ;W0 holds buffer fill value MOV MOV #0x1110, W1 ;point W1 to buffer DO AGAIN, #0x31 ;fill the 50 buffer locations WO, [W1++] ;fill the next location MOV AGAIN: INC W0, W0 ; increment the fill value 0x1163 Start Addr = 0x1100 End Addr = 0x1163Length = 0x0032 Words

MODULO ADDRESSING OPERATION EXAMPLE



4.4.3 MODULO ADDRESSING APPLICABILITY

Modulo Addressing can be applied to the Effective Address (EA) calculation associated with any W register. It is important to realize that the address boundaries check for addresses less than or greater than the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes may, therefore, jump beyond boundaries and still be adjusted correctly.

Note: The modulo corrected Effective Address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the Effective Address. When an address offset (e.g., [W7+W2]) is used, Modulo Address correction is performed but the contents of the register remain unchanged.

4.5 Bit-Reversed Addressing

Bit-Reversed Addressing mode is intended to simplify data reordering for radix-2 FFT algorithms. It is supported by the X AGU for data writes only.

The modifier, which may be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order; thus, the only operand requiring reversal is the modifier.

4.5.1 BIT-REVERSED ADDRESSING IMPLEMENTATION

Bit-Reversed Addressing mode is enabled when the following conditions exist:

- The BWM bits (W register selection) in the MODCON register are any value other than 15 (the stack cannot be accessed using Bit-Reversed Addressing).
- 2. The BREN bit is set in the XBREV register.
- 3. The addressing mode used is Register Indirect with Pre-Increment or Post-Increment.

be zeros. XB<14:0> is the Bit-Reversed Address 'pivot point,' which is typically a constant.

If the length of a bit-reversed buffer is

the last 'N' bits of the data buffer start a

'pivot point,' which is typically a constant. **Line case** of **Line** an FFT computation, its value is equal to half of the FFT data buffer size. 月一月上面的二维码图案,加我为朋友

Note:	All bit-reversed EA calculations assume
	word-sized data (LSb of every EA is
	always clear). The XB value is scaled
	accordingly to generate compatible (byte)
	addresses.

When enabled, Bit-Reversed Addressing is only executed for Register Indirect with Pre-Increment or Post-Increment Addressing and word-sized data writes. It will not function for any other addressing mode or for byte-sized data; normal addresses are generated instead. When Bit-Reversed Addressing is active, the W Address Pointer is always added to the address modifier (XB) and the offset associated with the Register Indirect Addressing mode is ignored. In addition, as word-sized data is a requirement, the LSb of the EA is ignored (and always clear).

Note:	Modulo Addressing and Bit-Reversed Addressing should not be enabled
	together. In the event that the user
	attempts to do so, Bit-Reversed Address-
	ing will assume priority for the X WAGU,
	and X WAGU Modulo Addressing will be
	disabled. However, Modulo Addressing will
	continue to function in the X RAGU.

If Bit-Reversed Addressing has already been enabled by setting the BREN bit (XBREV<15>), then a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the Bit-Reversed Pointer.

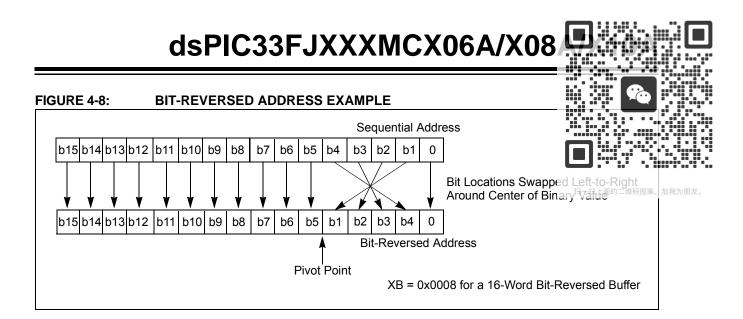


TABLE 4-37: BIT-REVERSED ADDRESS SEQUENCE (16-ENTRY)

		Norma	al Addres	SS			Bit-Rev	ersed Ac	Idress
A3	A2	A1	A0	Decimal	A3	A2	A1	A0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	8
0	0	1	0	2	0	1	0	0	4
0	0	1	1	3	1	1	0	0	12
0	1	0	0	4	0	0	1	0	2
0	1	0	1	5	1	0	1	0	10
0	1	1	0	6	0	1	1	0	6
0	1	1	1	7	1	1	1	0	14
1	0	0	0	8	0	0	0	1	1
1	0	0	1	9	1	0	0	1	9
1	0	1	0	10	0	1	0	1	5
1	0	1	1	11	1	1	0	1	13
1	1	0	0	12	0	0	1	1	3
1	1	0	1	13	1	0	1	1	11
1	1	1	0	14	0	1	1	1	7
1	1	1	1	15	1	1	1	1	15



4.6 Interfacing Program and Data Memory Spaces

The dsPIC33FJXXXMCX06A/X08A/X10A architecture uses a 24-bit wide program space and a 16-bit wide data space. The architecture is also a modified Harvard scheme, meaning that data can also be present in the program space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the dsPIC33FJXXXMCX06A/X08A/X10A architecture provides two methods by which program space can be accessed during operation:

- Using table instructions to access individual bytes or words anywhere in the program space
- Remapping a portion of the program space into the data space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated from time to time. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look ups from a large table of static data. It can only access the least significant word of the program word.

4.6.1 ADDRESSING PROGRAM

Since the address ranges for the data spaces are 16 and 24 bits, respectively needed to create a 23-bit or 24-bit proof from 16-bit data registers. The solution de interface method to be used.

For table operations, the 8-bit Table Page register (TBLPAG) is used to define a 32K word region within the program space. This is concatenated with a 16-bit EA to arrive at a full, 24-bit program space address. In this format, the Most Significant bit of TBLPAG is used to determine if the operation occurs in the user memory (TBLPAG<7> = 0) or the configuration memory (TBLPAG<7> = 1).

For remapping operations, the 8-bit Program Space Visibility register (PSVPAG) is used to define a 16K word page in the program space. When the Most Significant bit of the EA is '1', PSVPAG is concatenated with the lower 15 bits of the EA to form a 23-bit program space address. Unlike table operations, this limits remapping operations strictly to the user memory area.

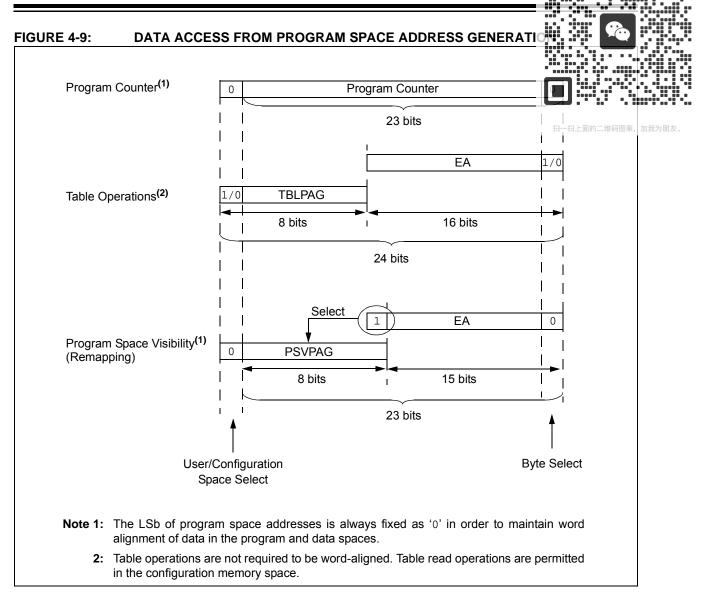
Table 4-38 and Figure 4-9 show how the program EA is created for table operations and remapping accesses from the data EA. Here, P<23:0> refers to a program space word, whereas D<15:0> refers to a data space word.

TABLE 4-38: PROGRAM SPACE ADDRESS CONSTRUCTION

	Access		Program Space Address								
Access Type	Space	<23>	<22:16>	<15>	<14:1>	<0>					
Instruction Access	User	0	0 PC<22:1>								
(Code Execution)		0xxx xxxx xxxx xxxx xxxx xxx0									
TBLRD/TBLWT	User	TB	LPAG<7:0>		Data EA<15:0>						
(Byte/Word Read/Write)		0	xxx xxxx	xxxx xxxx xxxx xxxx							
	Configuration	TB	LPAG<7:0>	Data EA<15:0>							
		1	xxx xxxx								
Program Space Visibility	User	0	PSVPAG<	7:0> Data EA<14:0> ⁽¹⁾							
(Block Remap/Read)		0	xxxx xxx	xx xxx xxxx xxxx xx							

Note 1: Data EA<15> is always '1' in this case, but is not used in calculating the program space address. Bit 15 of the address is PSVPAG<0>.

dsPIC33FJXXXMCX06A/X08



DATA ACCESS FROM PROGRAM 4.6.2 MEMORY USING TABLE **INSTRUCTIONS**

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the program space without going through data space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a program space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two 16-bit word wide address spaces residing side by side, each with the same address range. TBLRDL and TBLWTL access the space which contains the least significant data word, and TBLRDH and TBLWTH access the space which contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

TBLRDL (Table Read Low): In Word mode, it 1. maps the lower word of the program space location (P<15:0>) to a data address (D<15:0>).

In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when byte select is '1'; the lower byte is selected when it is '0'.

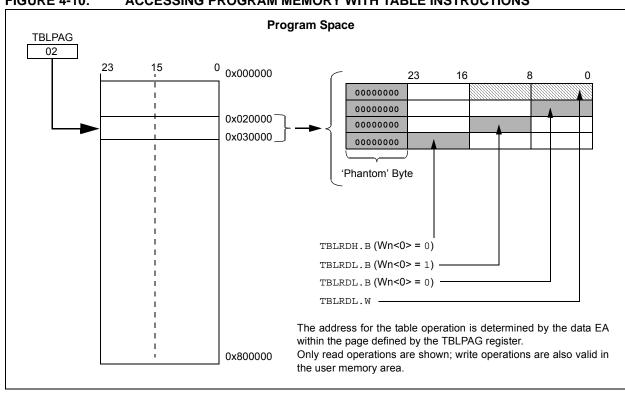
2. TBLRDH (Table Read High): In Wo maps the entire upper word of a progra (P<23:16>) to a data address. D<15:8>, the 'phantom' byte, will alw In Byte mode, it maps the upper or lo



the program word to D<7:0> of the data address, as above. Note that the datability of t always be '0' when the upper 'phantom' byte is selected (byte select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a program space address. The details of their operation are explained in Section 5.0 "Flash Program Memory".

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.



ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS FIGURE 4-10:

4.6.3 READING DATA FROM PROGRAM MEMORY USING PROGRAM SPACE VISIBILITY

The upper 32 Kbytes of data space may optionally be mapped into any 16K word page of the program space. This option provides transparent access of stored constant data from the data space without the need to use special instructions (i.e., TBLRDL/H).

Program space access through the data space occurs if the Most Significant bit of the data space EA is '1' and program space visibility is enabled by setting the PSV bit in the Core Control register (CORCON<2>). The location of the program memory space to be mapped into the data space is determined by the Program Space Visibility Page register (PSVPAG). This 8-bit register defines any one of 256 possible pages of 16K words in program space. In effect, PSVPAG functions as the upper 8 bits of the program memory address, with the 15 bits of the EA functioning as the lower bits. Note that by incrementing the PC by 2 for each program memory word, the lower 15 bits of data space addresses directly map to the lower 15 bits in the corresponding program space addresses.

Data reads to this area add an additional cycle to the instruction being executed, since two program memory fetches are required.

Although each data space address, 8000h and higher, maps directly into a corresponding program memory address (see Figure 4-11), only the lower 16 bits of the 24-bit program word are used to conupper 8 bits of any program space data should be programmed with '0000 0000' to force a NOP. This issues should the area of code ever executed.



Note: PSV access is temporarily disabled during table reads/writes.

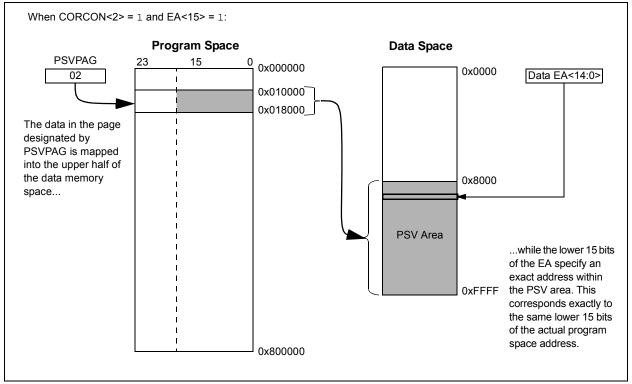
For operations that use PSV and are executed outside a REPEAT loop, the MOV and MOV.D instructions require one instruction cycle in addition to the specified execution time. All other instructions require two instruction cycles in addition to the specified execution time.

For operations that use PSV and are executed inside a REPEAT loop, there will be some instances that require two instruction cycles in addition to the specified execution time of the instruction:

- · Execution in the first iteration
- · Execution in the last iteration
- Execution prior to exiting the loop due to an interrupt
- Execution upon re-entering the loop after an interrupt is serviced

Any other iteration of the REPEAT loop will allow the instruction accessing data using PSV to execute in a single cycle.

FIGURE 4-11: PROGRAM SPACE VISIBILITY OPERATION



NOTES:



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5.0 FLASH PROGRAM MEMORY

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/X08A/ X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 5. "Flash Programming" (DS70191) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33FJXXXMCX06A/X08A/X10A devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

- 1. In-Circuit Serial Programming[™] (ICSP[™]) programming capability
- 2. Run-Time Self-Programming (RTSP)

ICSP allows a dsPIC33FJXXXMCX06A/X08A/X10A device to be serially programmed while in the end application circuit. This is simply done with two lines for programming clock and programming data (one of the alternate programming pin pairs: PGECx/PGEDx), and

three other lines for power (VDD), Master Clear (MCLR). This allow manufacture boards with unprogram then program the digital signal conshipping the product. This also allow firmware or a custom firmware to be program.



RTSP is accomplished using TBLFD (fable TEAM) and maximum transformed in the mead of the m

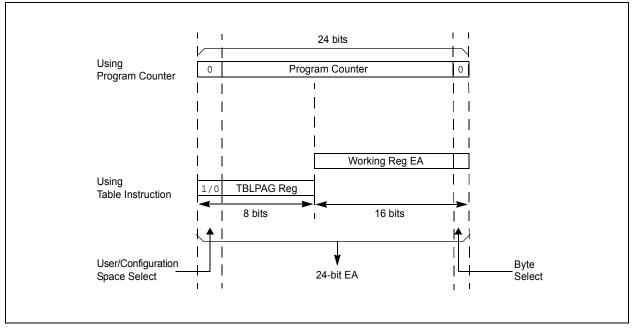
5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the table read and table write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS





5.2 RTSP Operation

The dsPIC33FJXXXMCX06A/X08A/X10A Flash program memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user to erase a page of memory at a time, which consists of eight rows (512 instructions), and to program one row or one word at a time. Table 26-12 shows typical erase and programming times. The 8-row erase pages and single row write rows are edge-aligned, from the beginning of program memory, on boundaries of 1536 bytes and 192 bytes, respectively.

The program memory implements holding buffers that can contain 64 instructions of programming data. Prior to the actual programming operation, the write data must be loaded into the buffers in sequential order. The instruction words loaded must always be from a group of 64 boundaries.

The basic sequence for RTSP programming is to set up a Table Pointer, then do a series of TBLWT instructions to load the buffers. Programming is performed by setting the control bits in the NVMCON register. A total of 64 TBLWTL and TBLWTH instructions are required to load the instructions.

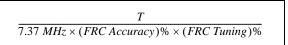
All of the table write operations are single-word writes (two instruction cycles), because only the buffers are written. A programming cycle is required for programming each row.

5.3 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

The programming time depends on the FRC accuracy (see Table 26-19) and the value of the FRC Oscillator Tuning register (see Register 9-4). Use the following formula to calculate the minimum and maximum values for the row write time, page erase time and word write cycle time parameters (see Table 26-12).

EQUATION 5-1: PROGRAMMING TIME



For example, if the device is operating at FRC accuracy will be ±5%. If the TUN<E Register 9-4) are set to `b11111, the rewrite time is equal to Equation 5-2.

EQUATION 5-2: MINIMUM ROW WRITE TIME 扫一扫上面的二维码图案,加我为朋友,

$$T_{RW} = \frac{11064 \ Cycles}{7.37 \ MHz \times (1 + 0.05) \times (1 - 0.00375)} = 1.435 ms$$

The maximum row write time is equal to Equation 5-3.

EQUATION 5-3: MAXIMUM ROW WRITE TIME

$$T_{RW} = \frac{11064 \ Cycles}{7.37 \ MHz \times (1 - 0.05) \times (1 - 0.00375)} = 1.586 ms$$

Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

5.4 Control Registers

There are two SFRs used to read and write the program Flash memory: NVMCON and NVMKEY.

The NVMCON register (Register 5-1) controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.

NVMKEY is a write-only register that is used for write protection. To start a programming or erase sequence, the user must consecutively write 0x55 and 0xAA to the NVMKEY register. Refer to **Section 5.3 "Programming Operations"** for further details.

NVMCON: FLASH MEMORY CONTROL REGISTER



R/SO-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	U-0	U-0	U-0	U-0				
WR	WREN	WRERR	_	—	—	_				
bit 15		-					bit a			
	(1)			(1)	(1)		an an Looks - With the se			
U-0	R/W-0 ⁽¹⁾	U-0	U-0	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾) 扫一扫卡雨的天街的图案,	加我为朋友。		
	ERASE	_			NVMOP	>(2)				
bit 7							bit 0	J		
Legend:		SO = Settable	Only bit]		
R = Readable	bit	W = Writable b	it	U = Unimpler	nented bit, read	as '0'				
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cle		x = Bit is u	nknown			
								_		
bit 15	WR: Write C		n na arama	r oroco oporatio	n The energies	n in colf tim	and and the hit is			
		by hardware onc			n. The operation	on is sell-un	ned and the bit is			
		n or erase operat			2					
bit 14	WREN: Write									
		Flash program/er	ase operati	ions						
		lash program/era								
bit 13	WRERR: Wr	rite Sequence Eri	or Flag bit							
	1 = An impre	oper program or	erase sequ	ence attempt, or	termination ha	s occurred (bit is set			
		tically on any set								
	•	gram or erase op		npleted normally	1					
bit 12-7	=	nted: Read as '0								
bit 6		se/Program Ena								
		the erase operation								
bit 5-4		the program open the program open open open open open open open open		CITIED BY NVMOR	<3:0> on the h	ext WR com	imand			
bit 3-0	-	>: NVM Operation		(2)						
DIL 3-0	If ERASE = 1		on Select bi							
		<u>⊥.</u> ìory bulk erase o	neration							
	1110 = Res e		peration							
		e General Segm	ent							
		e Secure Segme								
	1011 = Res e	erved								
		0011 = No operation								
		0010 = Memory page erase operation								
		0001 = No operation 0000 = Erase a single Configuration register byte								
			arationrog							
	<u>If ERASE = (</u> 1111 = No o									
	1111 = No 0	•								
	1101 = No o									
	1100 = No o									
	1011 = Res e	•								
	0011 = Mer	nory word prograi	n operatior	ı						
	0010 = No o	peration	-							
		nory row program								
	0000 = Prog	ram a single Cor	figuration r	egister byte						
Note 1. Th	aaa hita aan an	ly be reset on P(חר							

Note 1: These bits can only be reset on POR.

2: All other combinations of NVMOP<3:0> are unimplemented.

REGISTER 5-1:



The user can program one row of program Flash memory at a time. To do this, it is necessary to erase the 8-row erase page that contains the desired row. The general process is as follows:

- 1. Read eight rows of program memory (512 instructions) and store it in data RAM.
- 2. Update the program data in RAM with the desired new data.
- 3. Erase the block (see Example 5-1):
 - a) Set the NVMOP bits (NVMCON<3:0>) to '0010' to configure for block erase. Set the ERASE (NVMCON<6>) and WREN (NVMCON<14>) bits.
 - b) Write the starting address of the page to be erased into the TBLPAG and W registers.
 - c) Write 0x55 to NVMKEY.
 - d) Write 0xAA to NVMKEY.
 - e) Set the WR bit (NVMCON<15>). The erase cycle begins and the CPU stalls for the duration of the erase cycle. When the erase is done, the WR bit is cleared automatically.

- Write the first 64 instructions from date the program memory buffers (see Exc
- 5. Write the program block to Flash me
 - a) Set the NVMOP bits to '0001' to for row programming. Clear the and set the WREN bit.
 - b) Write 0x55 to NVMKEY.
 - c) Write 0xAA to NVMKEY.
 - d) Set the WR bit. The programming cycle begins and the CPU stalls for the duration of the write cycle. When the write to Flash memory is done, the WR bit is cleared automatically.
- Repeat steps 4 and 5 using the next available 64 instructions from the block in data RAM by incrementing the value in TBLPAG until all 512 instructions are written back to Flash memory.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPS, as shown in Example 5-3.

EXAMPLE 5-1: ERASING A PROGRAM MEMORY PAGE

: Set up NUMCON for block grade operation	
; Set up NVMCON for block erase operation	
MOV #0x4042, W0	i
MOV W0, NVMCON	; Initialize NVMCON
; Init pointer to row to be ERASED	
MOV #tblpage(PROG_ADDR), W0	;
MOV W0, TBLPAG	; Initialize PM Page Boundary SFR
MOV #tbloffset(PROG_ADDR), W0	; Initialize in-page EA[15:0] pointer
TBLWTL W0, [W0]	; Set base address of erase block
DISI #5	; Block all interrupts with priority <7
	; for next 5 instructions
MOV #0x55, W0	
MOV W0, NVMKEY	; Write the 55 key
MOV #0xAA, W1	;
MOV W1, NVMKEY	; Write the AA key
BSET NVMCON, #WR	; Start the erase sequence
NOP	; Insert two NOPs after the erase
NOP	; command is asserted



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EXAMPLE 5-2: LOADING THE WRITE BUFFERS

; Set up NVM	CON for row programming operat.	ions	
MOV	#0x4001, W0	;	·
MOV	W0, NVMCON	; Initialize NVMCON	•
; Set up a po	ointer to the first program me	mory location to be written	
; program men	mory selected, and writes enable	bled	
MOV	#0x0000, W0	; 扫一扫上面的二维码图案,加利	我为朋友
MOV	W0, TBLPAG	; Initialize PM Page Boundary SFR	
MOV	#0x6000, W0	; An example program memory address	
; Perform the	e TBLWT instructions to write [.]	the latches	
; 0th_program	m_word		
MOV	#LOW_WORD_0, W2	i	
MOV	<pre>#HIGH_BYTE_0, W3</pre>	i	
TBLWI	Ľ W2, [W0]	; Write PM low word into program latch	
TBLWI	'H W3, [W0++]	; Write PM high byte into program latch	
; 1st_program	m_word		
MOV	#LOW_WORD_1, W2	i	
MOV	#HIGH_BYTE_1, W3	i	
TBLWI	'L W2, [W0]	; Write PM low word into program latch	
TBLWI	'H W3, [W0++]	; Write PM high byte into program latch	
; 2nd_progra	am_word		
MOV	#LOW_WORD_2, W2	;	
MOV	<pre>#HIGH_BYTE_2, W3</pre>	;	
TBLWI	'L W2, [W0]	; Write PM low word into program latch	
TBLWI	'H W3, [W0++]	; Write PM high byte into program latch	
•			
•			
•			
; 63rd_progra	—		
MOV	#LOW_WORD_31, W2	;	
MOV	#HIGH_BYTE_31, W3	;	
	'L W2, [W0]	; Write PM low word into program latch	
TBLWI	'H W3, [W0++]	; Write PM high byte into program latch	
L			

EXAMPLE 5-3: **INITIATING A PROGRAMMING SEQUENCE**

DISI	#5	; Block all interrupts with priority <7
		; for next 5 instructions
MOV	#0x55, W0	
MOV	W0, NVMKEY	; Write the 55 key
MOV	#0xAA, W1	;
MOV	W1, NVMKEY	; Write the AA key
BSET	NVMCON, #WR	; Start the erase sequence
NOP		; Insert two NOPs after the
NOP		; erase command is asserted

NOTES:



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6.0 RESET

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/ X08A/X10A family of devices. However, it is not intended to be a comprereference source. hensive To complement the information in this data sheet, refer to Section 8. "Reset" (DS70192) in the "dsPIC33F/ PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal, SYSRST. The following is a list of device Reset sources:

- POR: Power-on Reset
- · BOR: Brown-out Reset
- MCLR: Master Clear Pin Reset
- SWR: RESET Instruction
- · WDT: Watchdog Timer Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Opcode and Uninitialized W Register Reset

A simplified block diagram of the shown in Figure 6-1.

Any active source of Reset will m signal active. Many registers associa and peripherals are forced to a kn



Most registers are unaffected by a Reset; their status is unknown on POR and unchanged by all other Research

Refer to the specific peripheral or CPU Note: section of this data sheet for register Reset states.

All types of device Reset will set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1). A POR will clear all bits except for the POR bit (RCON<0>), which is set. The user can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

The status bits in the RCON register Note: should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

FIGURE 6-1: **RESET SYSTEM BLOCK DIAGRAM** RESET Instruction Glitch Filter MCI R WDT Module Sleep or Idle BOR Internal SYSRST Regulator חח POR VDD Rise Detect Trap Conflict Illegal Opcode Uninitialized W Register

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REGISTER	6-1: RCON	I: RESET CON	ITROL REC	GISTER ⁽¹⁾			
R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	HMV.0
TRAPR	IOPUWR	_	—	_	_		WREGS(9)
pit 15							
							扫一扫上面的一维
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	^扫 R标 ^面 的一维
EXTR	SWR	SWDTEN ⁽²⁾	WDTO	SLEEP	IDLE	BOR	POR
oit 7							bit 0
Legend:							
R = Readab	ole bit	W = Writable b	it	U = Unimplei	mented bit, rea	d as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown
oit 15	1 = A Trap C	p Reset Flag bit onflict Reset has					
		onflict Reset has					
bit 14		egal Opcode or L			•		
	Address	al opcode detec Pointer caused al opcode or unin	a Reset			lized W regist	er used as an
bit 13-9	Unimplemer	nted: Read as '0	,				
bit 8	VREGS: Volt	tage Regulator S	tandby Durir	ng Sleep bit ⁽³⁾			
		egulator is active			ер		
bit 7	-	nal Reset (MCLF		Ū.	·		
	1 = A Master	Clear (pin) Rese Clear (pin) Rese	et has occur				
bit 6		are Reset (Instru					
		instruction has to instruction has r					
bit 5	SWDTEN: S	oftware Enable/[Disable of W	DT bit ⁽²⁾			
	1 = WDT is e 0 = WDT is d						
bit 4	WDTO: Wate	chdog Timer Time	e-out Flag bi	it			
		e-out has occurr e-out has not oc					
bit 3	SLEEP: Wak	ke-up from Sleep	Flag bit				
	1 = Device h	as been in Sleep as not been in S	mode				
bit 2		up from Idle Flag	-				
-	1 = Device w	as in Idle mode as not in Idle mo	-				
	All of the Reset sta	-	set or cleare	ed in software. S	Setting one of t	nese bits in soft	tware does not
	ause a device Re	eset.	(1) (-11

- 2: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.
- **3:** For dsPIC33FJ256MCX06A/X08A/X10A devices, this bit is unimplemented and reads back a programmed value.

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾ (CONTINUED)

- bit 1 BOR: Brown-out Reset Flag bit
 - 1 = A Brown-out Reset has occurred
 - 0 = A Brown-out Reset has not occurred
- bit 0 **POR:** Power-on Reset Flag bit
 - 1 = A Power-on Reset has occurred 0 = A Power-on Reset has not occurred
- **Note 1:** All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
 - 2: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.
 - **3:** For dsPIC33FJ256MCX06A/X08A/X10A devices, this bit is unimplemented and reads back a programmed value.



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Trap conflict event

W register access

RESET instruction

MCLR Reset

WDT time-out

BOR, POR

POR

Setting Event

Illegal opcode or uninitialized

PWRSAV #SLEEP instruction

PWRSAV #IDLE instruction



Flag Bit

TRAPR (RCON<15>)

EXTR (RCON<7>)

SWR (RCON<6>)

WDTO (RCON<4>)

SLEEP (RCON<3>)

IDLE (RCON<2>)

BOR (RCON<1>) POR (RCON<0>)

IOPUWR (RCON<14>)



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Note: All Reset flag bits may be set or cleared by the user software.

6.1 Clock Source Selection at Reset

If clock switching is enabled, the system clock source at device Reset is chosen, as shown in Table 6-2. If clock switching is disabled, the system clock source is always selected according to the oscillator Configuration bits. Refer to Section 9.0 "Oscillator Configuration" for further details.

TABLE 6-2: OSCILLATOR SELECTION vs. TYPE OF RESET (CLOCK SWITCHING ENABLED)

Reset Type	Clock Source Determinant
POR	Oscillator Configuration bits
BOR	(FNOSC<2:0>)
MCLR	COSC Control bits
WDTR	(OSCCON<14:12>)
SWR	

6.2 Device Reset Times

POR, BOR

POR. BOR

POR, BOR

POR, BOR POR, BOR

POR

The Reset times for various types of device Reset are <u>summarized</u> in Table 6-3. The System Reset signal, SYSRST, is released after the POR and PWRT delay times expire.

PWRSAV instruction, POR, BOR

The time at which the device actually begins to execute code also depends on the system oscillator delays, which include the Oscillator Start-up Timer (OST) and the PLL lock time. The OST and PLL lock times occur in parallel with the applicable SYSRST delay times.

The FSCM delay determines the time at which the FSCM begins to monitor the system clock source after the SYSRST signal is released.



TABLE 0-5.						
Reset Type	Clock Source	SYSRST Delay	System Clock Delay	FSCM Delay	See Seten	
POR	EC, FRC, LPRC	TPOR + TSTARTUP + TRST	_		2.9	
	ECPLL, FRCPLL	TPOR + TSTARTUP + TRST	TLOCK	TFSCM	1, 2, 3, 5, 6	
	XT, HS, SOSC	TPOR + TSTARTUP + TRST	Tost	TFSCM	相一扫上面的二维码图案, 1, 2, 3, 4, 5	
	XTPLL, HSPLL	TPOR + TSTARTUP + TRST	TOST + TLOCK	TFSCM	1, 2, 3, 4, 5, 6	
BOR	EC, FRC, LPRC	TSTARTUP + TRST	_	_	3	
	ECPLL, FRCPLL	TSTARTUP + TRST	Тьоск	TFSCM	3, 5, 6	
	XT, HS, SOSC	TSTARTUP + TRST	Tost	TFSCM	3, 4, 6	
	XTPLL, HSPLL	TSTARTUP + TRST	TOST + TLOCK	TFSCM	3, 4, 5, 6	
MCLR	Any Clock	Trst	_		3	
WDT	Any Clock	Trst	—		3	
Software	Any Clock	Trst	—		3	
Illegal Opcode	Any Clock	Trst	—		3	
Uninitialized W	Any Clock	Trst	—		3	
Trap Conflict	Any Clock	Trst	_		3	

TABLE 6-3:RESET DELAY TIMES FOR VARIOUS DEVICE RESETS

Note 1: TPOR = Power-on Reset delay (10 μ s nominal).

2: TSTARTUP = Conditional POR delay of 20 μs nominal (if on-chip regulator is enabled) or 64 ms nominal Power-up Timer delay (if regulator is disabled). TSTARTUP is also applied to all returns from powered-down states, including waking from Sleep mode if the regulator is enabled.

3: TRST = Internal state Reset time (20 µs nominal).

4: TOST = Oscillator Start-up Timer. A 10-bit counter counts 1024 oscillator periods before releasing the oscillator clock to the system.

5: TLOCK = PLL lock time (20 μs nominal).

6: TFSCM = Fail-Safe Clock Monitor delay (100 μs nominal).



6.2.1 POR AND LONG OSCILLATOR START-UP TIMES

The oscillator start-up circuitry and its associated delay timers are not linked to the device Reset delays that occur at power-up. Some crystal circuits (especially low-frequency crystals) have a relatively long start-up time. Therefore, one or more of the following conditions is possible after SYSRST is released:

- The oscillator circuit has not begun to oscillate.
- The Oscillator Start-up Timer has not expired (if a crystal oscillator is used).
- The PLL has not achieved a lock (if PLL is used).

The device will not begin to execute code until a valid clock source has been released to the system. Therefore, the oscillator and PLL start-up delays must be considered when the Reset delay time must be known.

6.2.2 FAIL-SAFE CLOCK MONITOR (FSCM) AND DEVICE RESETS

If the FSCM is enabled, it begins to monitor the system clock source when SYSRST is released. If a valid clock source is not available at this time, the device automatically switches to the FRC oscillator and the user can switch to the desired crystal oscillator in the Trap Service Routine.

6.2.2.1 FSCM Delay for Crystal a Clock Sources

When the system clock source is provided and on the PLL, a small delay automatically inserted after the POR and times. The FSCM does not begin to monitor the system

clock source until this delay expires. The FSCM delay time is nominally 500 μ s and provides additional time for the oscillator and/or PLL to stabilize. In most cases, the FSCM delay prevents an oscillator failure trap at a device Reset when the PWRT is disabled.

6.3 Special Function Register Reset States

Most of the Special Function Registers (SFRs) associated with the CPU and peripherals are reset to a particular value at a device Reset. The SFRs are grouped by their peripheral or CPU function and their Reset values are specified in each section of this manual.

The Reset value for each SFR does not depend on the type of Reset, with the exception of two registers. The Reset value for the Reset Control register, RCON, depends on the type of device Reset. The Reset value for the Oscillator Control register, OSCCON, depends on the type of Reset and the programmed values of the oscillator Configuration bits in the FOSC Configuration register.

7.0 INTERRUPT CONTROLLER

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/ X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 6. "Interrupts" (DS70184) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The interrupt controller for the dsPIC33FJXXXMCX06A/X08A/X10A family of devices reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33FJXXXMCX06A/X08A/X10A CPU. It has the following features:

- Up to eight processor exceptions and software traps
- Seven user-selectable priority levels
- Interrupt Vector Table (IVT) with up to 118 vectors
- A unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Alternate Interrupt Vector Table (AIVT) for debug support
- · Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The Interrupt Vector Table (IVT) is shown in Figure 7-1. The IVT resides in program memory, starting at location 000004h. The IVT contains 126 vectors consisting of eight nonmaskable trap vectors plus up to 118 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority; this priority is linked to their position in the vector table. All other things being equal, lower addresses have a higher natural priority. For example, the interrupt associated with vector 0 will take priority over interrupts at any other vector address. The dsPIC33FJXXXMCX06A/X08A devices implement up to 67 unique in nonmaskable traps. These are Table 7-1 and Table 7-2.



7.1.1 ALTERNATE INTERRUPT VEC TABLE H-RLEMO

The Alternate Interrupt Vector Table (AIVT) is located after the IVT, as shown in Figure 7-1. Access to the AIVT is provided by the ALTIVT control bit (INTCON2<15>). If the ALTIVT bit is set, all interrupt and exception processes use the alternate vectors instead of the default vectors. The alternate vectors are organized in the same manner as the default vectors.

The AIVT supports debugging by providing a means to switch between an application and a support environment without requiring the interrupt vectors to be reprogrammed. This feature also enables switching between applications for evaluation of different software algorithms at run time. If the AIVT is not needed, the AIVT should be programmed with the same addresses used in the IVT.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33FJXXXMCX06A/X08A/X10A device clears its registers in response to a Reset, which forces the PC to zero. The digital signal controller then begins program execution at location 0x000000. The user programs a GOTO instruction at the Reset address, which redirects program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT and AIVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.



	Reset – GOTO Instruction	0x000000	
	Reset – GOTO Address	0x000002	
	Reserved	0x000004	·····
	Oscillator Fail Trap Vector	_	
	Address Error Trap Vector	_	扫一扫上面的二维码图案,加
	Stack Error Trap Vector	_	
	Math Error Trap Vector	_	
	DMA Error Trap Vector	_	
	Reserved	_	
	Reserved	0.000011	
	Interrupt Vector 0	0x000014 —	
	Interrupt Vector 1		
	~		
	~	-	
		0x000070	
	Interrupt Vector 52 Interrupt Vector 53	0x00007C 0x00007E	Interrupt Vector Table (IVT) ⁽¹⁾
≥	Interrupt Vector 54	0x00007E	
orit		0x000080	
Pri	~	-	
er	~	-	
Ord	Interrupt Vector 116	0x0000FC	
a	Interrupt Vector 117	0x0000FE	
tr	Reserved	0x000100	
Decreasing Natural Order Priority	Reserved	0x000102	
bu	Reserved	0,000102	
asi	Oscillator Fail Trap Vector	-	
cre	Address Error Trap Vector		
De	Stack Error Trap Vector		
	Math Error Trap Vector		
	DMA Error Trap Vector	-	
	Reserved	-	
	Reserved	-	
	Interrupt Vector 0	0x000114 —	
	Interrupt Vector 1	1	
	~]	
	~		
	~		Alternate Interrupt Vector Table (AIVT) ⁽¹⁾
	Interrupt Vector 52	0x00017C	
	Interrupt Vector 53	0x00017E	
	Interrupt Vector 54	0x000180	
	~		
	~		
	~		
	Interrupt Vector 116		
\checkmark	Interrupt Vector 117	0x0001FE —	L I
v	Start of Code	0x000200	



TABLE 7-1: INTERRUPT VECTORS

ABLE 7-1:		PT VECTORS	1	
Vector Number	Interrupt Request (IRQ) Number	IVT Address	AIVT Address	Interrupt Source
8	0	0x000014	0x000114	INT0 – External Interrupt 0
9	1	0x000016	0x000116	IC1 – Input Capture 1 _{扫一扫上面的二维码图案, 加我}
10	2	0x000018	0x000118	OC1 – Output Compare 1
11	3	0x00001A	0x00011A	T1 – Timer1
12	4	0x00001C	0x00011C	DMA0 – DMA Channel 0
13	5	0x00001E	0x00011E	IC2 – Input Capture 2
14	6	0x000020	0x000120	OC2 – Output Compare 2
15	7	0x000022	0x000122	T2 – Timer2
16	8	0x000024	0x000124	T3 – Timer3
17	9	0x000026	0x000126	SPI1E – SPI1 Error
18	10	0x000028	0x000128	SPI1 – SPI1 Transfer Done
19	11	0x00002A	0x00012A	U1RX – UART1 Receiver
20	12	0x00002C	0x00012C	U1TX – UART1 Transmitter
21	13	0x00002E	0x00012E	ADC1 – ADC 1
22	14	0x000030	0x000130	DMA1 – DMA Channel 1
23	15	0x000032	0x000132	Reserved
24	16	0x000034	0x000134	SI2C1 – I2C1 Slave Events
25	17	0x000036	0x000136	MI2C1 – I2C1 Master Events
26	18	0x000038	0x000138	Reserved
27	19	0x00003A	0x00013A	Change Notification Interrupt
28	20	0x00003C	0x00013C	INT1 – External Interrupt 1
29	21	0x00003E	0x00013E	ADC2 – ADC 2
30	22	0x000040	0x000140	IC7 – Input Capture 7
31	23	0x000042	0x000142	IC8 – Input Capture 8
32	24	0x000044	0x000144	DMA2 – DMA Channel 2
33	25	0x000046	0x000146	OC3 – Output Compare 3
34	26	0x000048	0x000148	OC4 – Output Compare 4
35	27	0x00004A	0x00014A	T4 – Timer4
36	28	0x00004C	0x00014C	T5 – Timer5
37	29	0x00004E	0x00014E	INT2 – External Interrupt 2
38	30	0x000050	0x000150	U2RX – UART2 Receiver
39	31	0x000052	0x000152	U2TX – UART2 Transmitter
40	32	0x000054	0x000154	SPI2E – SPI2 Error
41	33	0x000056	0x000156	SPI1 – SPI1 Transfer Done
42	34	0x000058	0x000158	C1RX – ECAN1 Receive Data Ready
43	35	0x00005A	0x00015A	C1 – ECAN1 Event
44	36	0x00005C	0x00015C	DMA3 – DMA Channel 3
45	37	0x00005E	0x00015E	IC3 – Input Capture 3
46	38	0x000060	0x000160	IC4 – Input Capture 4
47	39	0x000062	0x000162	IC5 – Input Capture 5
48	40	0x000064	0x000164	IC6 – Input Capture 6
49	41	0x000066	0x000166	OC5 – Output Compare 5
50	42	0x000068	0x000168	OC6 – Output Compare 6
51	43	0x00006A	0x00016A	OC7 – Output Compare 7
52	44	0x00006C	0x00016C	OC8 – Output Compare 8
53	45	0x00006E	0x00016E	Reserved



TABLE 7-1: INTERRUPT VECTORS (CONTINUED)

Vector Number	Interrupt Request (IRQ) Number	IVT Address	AIVT Address	Interrupt Source	
54	46	0x000070	0x000170	DMA4 – DMA Channel 4	***************
55	47	0x000072	0x000172	T6 – Timer6 扫一扫上面的二维	一 赴码图案,加我为朋友。
56	48	0x000074	0x000174	T7 – Timer7	
57	49	0x000076	0x000176	SI2C2 – I2C2 Slave Events	
58	50	0x000078	0x000178	MI2C2 – I2C2 Master Events	
59	51	0x00007A	0x00017A	T8 – Timer8	
60	52	0x00007C	0x00017C	T9 – Timer9	
61	53	0x00007E	0x00017E	INT3 – External Interrupt 3	
62	54	0x000080	0x000180	INT4 – External Interrupt 4	
63	55	0x000082	0x000182	C2RX – ECAN2 Receive Data Ready	
64	56	0x000084	0x000184	C2 – ECAN2 Event	
65	57	0x000086	0x000186	PWM – PWM Period Match	
66	58	0x000088	0x000188	QEI – Position Counter Compare	
69	61	0x00008E	0x00018E	DMA5 – DMA Channel 5	
70	62	0x000090	0x000190	Reserved	
71	63	0x000092	0x000192	FLTA – MCPWM Fault A	
72	64	0x000094	0x000194	FLTB – MCPWM Fault B	
73	65	0x000096	0x000196	U1E – UART1 Error	
74	66	0x000098	0x000198	U2E – UART2 Error	
75	67	0x00009A	0x00019A	Reserved	
76	68	0x00009C	0x00019C	DMA6 – DMA Channel 6	
77	69	0x00009E	0x00019E	DMA7 – DMA Channel 7	
78	70	0x0000A0	0x0001A0	C1TX – ECAN1 Transmit Data Request	
79	71	0x0000A2	0x0001A2	C2TX – ECAN2 Transmit Data Request	
80-125	72-117	0x0000A4- 0x0000FE	0x0001A4- 0x0001FE	Reserved	

TABLE 7-2: TRAP VECTORS

Vector Number	IVT Address	AIVT Address	Trap Source
0	0x000004	0x000104	Reserved
1	0x000006	0x000106	Oscillator Failure
2	0x000008	0x000108	Address Error
3	0x00000A	0x00010A	Stack Error
4	0x00000C	0x00010C	Math Error
5	0x00000E	0x00010E	DMA Error Trap
6	0x000010	0x000110	Reserved
7	0x000012	0x000112	Reserved

7.3 Interrupt Control and Status Registers

dsPIC33FJXXXMCX06A/X08A/X10A devices implement a total of 30 registers for the interrupt controller:

- INTCON1
- INTCON2
- IFS0 through IFS4
- IEC0 through IEC4
- IPC0 through IPC17
- INTTREG

Global interrupt control functions are controlled from INTCON1 and INTCON2. INTCON1 contains the Interrupt Nesting Disable bit (NSTDIS) as well as the control and status flags for the processor trap sources. The INTCON2 register controls the external interrupt request signal behavior and the use of the Alternate Interrupt Vector Table.

The IFS registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

The IEC registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals. The IPC registers are used to set the level for each source of interrupt. E source can be assigned to one of eight



The INTTREG register contains interrupt vector number and the new priority level, which are latched into vector number

(VECNUM<6:0>) and Interrupt level^扫bit上(仰色R老奶奶多) ^{加我为朋友。} fields in the INTTREG register. The new interrupt priority level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence that they are listed in Table 7-1. For example, the INT0 (External Interrupt 0) is shown as having vector number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit in IEC0<0> and the INT0IP bits in the first position of IPC0 (IPC0<2:0>).

Although they are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. The CPU STATUS register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU interrupt priority level. The user can change the current CPU priority level by writing to the IPL bits.

The CORCON register contains the IPL3 bit, which together with IPL<2:0>, also indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 7-1 through Register 7-32 in the following pages.



REGISTER 7-1: SR: CPU STATUS REGISTER⁽¹⁾

R-0	R-0	R/C-0	R/C-0	R-0	R/C-0	R-0
OA	OB	SA	SB	OAB	SAB	DA
bit 15						

R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R-0	R/W-0	R/W-0	R/W-0	——扫—扫上面的二维和 R/W-0	冯图案,加我为朋友。
IPL2 ⁽²⁾	IPL1 ⁽²⁾	IPL0 ⁽²⁾	RA	N	OV	Z	С	
bit 7							bit 0	

Legend:

Legend:			
C = Clearable bit	R = Readable bit	U = Unimplemented bit, read as '0'	
S = Settable bit	W = Writable bit	-n = Value at POR	
'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 7-5

IPL<2:0>: CPU Interrupt Priority Level Status bits⁽²⁾

111 = CPU interrupt priority level is 7 (15), user interrupts disabled 110 = CPU interrupt priority level is 6 (14)

- 101 = CPU interrupt priority level is 5 (13)
- 100 = CPU interrupt priority level is 3 (13) 100 = CPU interrupt priority level is 4 (12)
- 011 = CPU interrupt priority level is 3 (11)
- 010 = CPU interrupt priority level is 2 (10)
- 001 = CPU interrupt priority level is 1 (9)
- 000 = CPU interrupt priority level is 0 (8)
- Note 1: For complete register details, see Register 3-1: "SR: CPU STATUS Register".
 - 2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU interrupt priority level. The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
 - 3: The IPL<2:0> status bits are read-only when NSTDIS (INTCON1<15>) = 1.

REGISTER 7-2: CORCON: CORE CONTROL REGISTER⁽¹⁾

U-0	U-0	R/W-0	R/W-0	R-0	R-0	R-0
_	—	US	EDT		DL<2:0>	
						bit 8
R/W-0	R/W-1	R/W-0	R/C-0	R/W-0	R/W-0	R/W-0
SATB	SATDW	ACCSAT	IPL3 ⁽²⁾	PSV	RND	IF
						bit 0
	C = Clearable	bit				
t	W = Writable	bit	-n = Value at I	POR	'1' = Bit is set	
0' = Bit is cleared 'x = Bit is unknown		U = Unimplemented bit, read as '0'				
	R/W-0 SATB	R/W-0 R/W-1 SATB SATDW C = Clearable W = Writable	— US R/W-0 R/W-1 R/W-0 SATB SATDW ACCSAT C = Clearable bit W = Writable bit	- US EDT R/W-0 R/W-1 R/W-0 R/C-0 SATB SATDW ACCSAT IPL3 ⁽²⁾ C = Clearable bit W = Writable bit -n = Value at I	- US EDT R/W-0 R/W-1 R/W-0 R/C-0 R/W-0 SATB SATDW ACCSAT IPL3 ⁽²⁾ PSV C = Clearable bit W = Writable bit -n = Value at POR	- US EDT DL<2:0> R/W-0 R/W-1 R/W-0 R/C-0 R/W-0 SATB SATDW ACCSAT IPL3 ⁽²⁾ PSV RND C = Clearable bit -n = Value at POR '1' = Bit is set

bit 3

IPL3: CPU Interrupt Priority Level Status bit 3⁽²⁾

- 1 = CPU interrupt priority level is greater than 7
- 0 = CPU interrupt priority level is 7 or less

Note 1: For complete register details, see Register 3-2: "CORCON: CORE Control Register".

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU interrupt priority level.



REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE
bit 15						C

								_加我
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	1
SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	1
bit 7							bit 0]

Legend:	1		11 - Halassin Constants († 1993)							
R = Readab		W = Writable bit	U = Unimplemented bit,							
-n = Value a	t POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown						
bit 15	NETDIE	Interrupt Neeting Disable bit								
DIL 15		Interrupt Nesting Disable bit upt nesting is disabled	l							
		upt nesting is enabled								
bit 14		: Accumulator A Overflow T	rap Flag bit							
		vas caused by overflow of A								
		vas not caused by overflow								
bit 13	OVBERR	: Accumulator B Overflow T	rap Flag bit							
		vas caused by overflow of A vas not caused by overflow								
bit 12	-	R: Accumulator A Catastrop								
		vas caused by catastrophic								
	0 = Trap v	was not caused by catastrop	phic overflow of Accumulator A	ł						
bit 11	COVBER	COVBERR: Accumulator B Catastrophic Overflow Trap Flag bit								
		vas caused by catastrophic vas not caused by catastrop	overflow of Accumulator B bhic overflow of Accumulator E	3						
bit 10	-	OVATE: Accumulator A Overflow Trap Enable bit								
	1 = Trap c 0 = Trap c	overflow of Accumulator A disabled								
bit 9	OVBTE: A	Accumulator B Overflow Tra	p Enable bit							
	1 = Trap o	overflow of Accumulator B								
	0 = Trap c	disabled								
bit 8	COVTE: (Catastrophic Overflow Trap	Enable bit							
	1 = Trap c 0 = Trap c	•	Accumulator A or B enabled							
bit 7	SFTACEF	RR: Shift Accumulator Error	Status bit							
		error trap was caused by an								
		•	y an invalid accumulator shift							
bit 6	-	: Arithmetic Error Status bit								
		error trap was caused by a c error trap was not caused b								
bit 5	DMACER	R: DMA Controller Error Sta	atus bit							
		controller error trap has occ								
		controller error trap has not								
bit 4		R: Arithmetic Error Status bi	it							
	1 = Math	error trap has occurred								



REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)

bit 3	ADDRERR: Address Error Trap Status bit 1 = Address error trap has occurred 0 = Address error trap has not occurred
bit 2	STKERR: Stack Error Trap Status bit
	 Stack error trap has occurred Stack error trap has not occurred
bit 1	OSCFAIL: Oscillator Failure Trap Status bit
	 1 = Oscillator failure trap has occurred 0 = Oscillator failure trap has not occurred
bit 0	Unimplemented: Read as '0'





R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	619
ALTIVT	DISI	—	_	—	—	— Г	
t 15						Ľ	bit
						挂	日一扫上面的二维码图
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP
oit 7							bit
_egend:							
R = Readab		W = Writable		•	mented bit, rea		
n = Value a	t POR	'1' = Bit is set	1	'0' = Bit is cle	ared	x = Bit is unki	nown
oit 15		able Alternate In	•	r Table bit			
		ernate Interrupt					
		ndard (default) v					
pit 14	DISI: DISI	Instruction Statu	is bit				
		struction is activ	-				
		struction is not a					
bit 13-5	-	ented: Read as '					
oit 4		ternal Interrupt	•	t Polarity Selec	t bit		
		t on negative ed t on positive edg					
oit 3	INT3EP: EX	ternal Interrupt	3 Edge Detec	t Polarity Selec	t bit		
		t on negative ed	0				
pit 2	•	t on positive edg ternal Interrupt 2		t Dolority Coloo	t h:t		
אנ∠		t on negative ed	•	a Polarity Selec			
		t on positive ed					
pit 1		ternal Interrupt	·	t Polarity Selec	t bit		
		t on negative ed	•				
		t on positive edg	0				
oit O		ternal Interrupt (·	t Polarity Selec	t bit		
		t on negative ed	•	2			

REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2



加我为朋友。

REGISTER 7-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	Γ
bit 15							C

							扫一扫上面的二维码图
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T2IF	OC2IF	IC2IF	DMA01IF	T1IF	OC1IF	IC1IF	INT0IF
bit 7							bit 0

Legend:	bla bit	\N/ - \N/ritchla hit	11 - Unimplemented bit	road on 'O'						
R = Reada		W = Writable bit	U = Unimplemented bit,							
-n = Value	alpor	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown						
bit 15	Unimplen	nented: Read as '0'								
bit 14	•		fer Complete Interrupt Flag S	tatus hit						
DIL 14		on a channel i bata mans	iei Complete interrupt Play S							
		ipt request has not occurred	t							
bit 13	AD1IF: AI	DC1 Conversion Complete I	nterrupt Flag Status bit							
	1 = Interru	pt request has occurred								
	0 = Interru	pt request has not occurred	ł							
bit 12		JART1 Transmitter Interrupt	Flag Status bit							
		1 = Interrupt request has occurred								
hit 11		upt request has not occurred								
bit 11		JART1 Receiver Interrupt F	lag Status Dit							
		 Interrupt request has occurred Interrupt request has not occurred 								
oit 10		SPI1IF: SPI1 Event Interrupt Flag Status bit								
	1 = Interru	upt request has occurred								
	0 = Interru	pt request has not occurred	ł							
bit 9		SPI1EIF: SPI1 Fault Interrupt Flag Status bit								
		1 = Interrupt request has occurred								
L H 0		0 = Interrupt request has not occurred								
bit 8		T3IF: Timer3 Interrupt Flag Status bit 1 = Interrupt request has occurred								
		ipt request has not occurred	ł							
bit 7		er2 Interrupt Flag Status bit								
		ipt request has occurred								
	0 = Interru	pt request has not occurred	ł							
bit 6		utput Compare Channel 2 Ir	nterrupt Flag Status bit							
		upt request has occurred	4							
L:1 C		upt request has not occurred								
bit 5	•	ut Capture Channel 2 Interr upt request has occurred	upt riag Status bit							
		ipt request has occurred	ł							
bit 4			fer Complete Interrupt Flag S	tatus bit						
		upt request has occurred								
	0 = Interru	pt request has not occurred	t							
bit 3		er1 Interrupt Flag Status bit								
		upt request has occurred	4							
	0 = Interru	pt request has not occurred	1							

REGISTER 7-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0 (CONTINUED)

- bit 2 OC1IF: Output Compare Channel 1 Interrupt Flag Status bit 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 1 IC1IF: Input Capture Channel 1 Interrupt Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 0 INTOIF: External Interrupt 0 Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred



扫一扫上面的二维码图案,加我为朋友。



REGISTER 7-6: IFS1: INTERRUPT FLAG STATUS REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	Π
bit 15	•		•	•			1

								扫一扫上面的二维码	马图案,加我为朋友。
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	
Ī	IC8IF	IC7IF	AD2IF	INT1IF	CNIF	—	MI2C1IF	SI2C1IF	
Ī	bit 7							bit 0	

Legend:										
R = Reada	ble bit	W = Writable bit	U = Unimplemented bit,	read as '0'						
-n = Value	at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown						
bit 15		UART2 Transmitter Interrupt	t Flag Status bit							
		upt request has occurred upt request has not occurred	4							
bit 14		U2RXIF: UART2 Receiver Interrupt Flag Status bit								
		upt request has occurred								
		upt request has not occurred	t							
bit 13	INT2IF: E	External Interrupt 2 Flag State	us bit							
		1 = Interrupt request has occurred								
		upt request has not occurred								
pit 12		T5IF: Timer5 Interrupt Flag Status bit								
	 I = Interrupt request has occurred Interrupt request has not occurred 									
bit 11	T4IF: Timer4 Interrupt Flag Status bit									
л		upt request has occurred								
		upt request has not occurred	t							
it 10	OC4IF: C	OC4IF: Output Compare Channel 4 Interrupt Flag Status bit								
		upt request has occurred								
	0 = Interr	upt request has not occurred	b							
bit 9	OC3IF: Output Compare Channel 3 Interrupt Flag Status bit									
		upt request has occurred	4							
oit 8		upt request has not occurred		otus hit						
лго		upt request has occurred	fer Complete Interrupt Flag St	alus bil						
		upt request has not occurred	t							
oit 7	IC8IF: Inp	out Capture Channel 8 Interr	upt Flag Status bit							
	1 = Interrupt request has occurred									
	0 = Interr	0 = Interrupt request has not occurred								
oit 6	IC7IF: Inp	out Capture Channel 7 Interr	upt Flag Status bit							
		upt request has occurred								
sit E		upt request has not occurred								
oit 5		DC2 Conversion Complete I	interrupt Flag Status bit							
		upt request has occurred upt request has not occurred	t							
oit 4		External Interrupt 1 Flag State								
		upt request has occurred								
		upt request has not occurred	t							

REGISTER 7-6: IFS1: INTERRUPT FLAG STATUS REGISTER 1 (CONTINUED)

- bit 3 CNIF: Input Change Notification Interrupt Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 2 Unimplemented: Read as '0'
- bit 1 MI2C1IF: I2C1 Master Events Interrupt Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 0 SI2C1IF: I2C1 Slave Events Interrupt Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred



扫一扫上面的二维码图案,加我为朋友。



REGISTER 7-7: IFS2: INTERRUPT FLAG STATUS REGISTER 2

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
T6IF	DMA4IF	—	OC8IF	OC7IF	OC6IF	OC5IF
bit 15						

							扫一扫上面的二维码	3图案,加我为朋友。
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
IC5IF	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	
bit 7							bit 0	

Legend:	ala hit	M = M/ritchic hit	= nimplomented bit	road as '0'						
R = Readat -n = Value a		W = Writable bit '1' = Bit is set	U = Unimplemented bit, '0' = Bit is cleared	x = Bit is unknown						
	al FUK									
bit 15	T6IF: Tim	er6 Interrupt Flag Status bit								
		upt request has occurred								
	0 = Interru	upt request has not occurred	I							
bit 14	DMA4IF:	DMA4IF: DMA Channel 4 Data Transfer Complete Interrupt Flag Status bit								
		1 = Interrupt request has occurred								
		upt request has not occurred	1							
bit 13	-	nented: Read as '0'								
bit 12		utput Compare Channel 8 Ir	iterrupt Flag Status bit							
		upt request has occurred upt request has not occurred	1							
bit 11		utput Compare Channel 7 Ir								
	1 = Interrupt request has occurred									
		upt request has not occurred	I							
bit 10	OC6IF: O	OC6IF: Output Compare Channel 6 Interrupt Flag Status bit								
		upt request has occurred								
		upt request has not occurred								
oit 9		utput Compare Channel 5 Ir	iterrupt Flag Status bit							
		 1 = Interrupt request has occurred 0 = Interrupt request has not occurred 								
bit 8	IC6IF: Input Capture Channel 6 Interrupt Flag Status bit									
	1 = Interrupt request has occurred									
	0 = Interru	upt request has not occurred	ł							
bit 7	IC5IF: Inp	ut Capture Channel 5 Interr	upt Flag Status bit							
	1 = Interrupt request has occurred									
		upt request has not occurred								
bit 6	-	ut Capture Channel 4 Interru	upt Flag Status bit							
		 1 = Interrupt request has occurred 0 = Interrupt request has not occurred 								
bit 5		ut Capture Channel 3 Interr								
	•	upt request has occurred								
	0 = Interru	upt request has not occurred	1							
bit 4	DMA3IF:	DMA Channel 3 Data Trans	fer Complete Interrupt Flag St	tatus bit						
		upt request has occurred	1							
L:1 0		upt request has not occurred								
bit 3		AN1 Event Interrupt Flag Sta upt request has occurred	alus dil							
		upt request has occurred	1							

REGISTER 7-7: IFS2: INTERRUPT FLAG STATUS REGISTER 2 (CONTINUED)

- bit 2 C1RXIF: ECAN1 Receive Data Ready Interrupt Flag Status bit 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 1 SPI2IF: SPI2 Event Interrupt Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 0 SPI2EIF: SPI2 Error Interrupt Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred



扫一扫上面的二维码图案,加我为朋友。



加我为朋友。

REGISTER 7-8: IFS3: INTERRUPT FLAG STATUS REGISTER 3

R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
FLTAIF	—	DMA5IF	—	—	QEIIF	PWMIF
bit 15						

							扫一扫上面的二维码图
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C2RXIF	INT4IF	INT3IF	T9IF	T8IF	MI2C2IF	SI2C2IF	T7IF
bit 7							bit 0

Legend:									
R = Readable	e bit	W = Writable bit	U = Unimplemented bit,	read as '0'					
-n = Value at	POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown					
bit 15		NM Fault A Interrupt Flag S	tatus bit						
	 I = Interrupt request has occurred I = Interrupt request has not occurred 								
bit 14	-	ented: Read as '0'							
bit 13	•		er Complete Interrupt Flag Sl	atus hit					
		ot request has occurred							
		ot request has not occurred							
bit 12-11	-	ented: Read as '0'							
bit 10	QEIIF: QEI	Event Interrupt Flag Status	s bit						
	1 = Interrupt request has occurred								
	0 = Interrupt request has not occurred								
bit 9	PWMIF: P	NM Interrupt Flag Status bit	t						
		ot request has occurred							
		ot request has not occurred							
bit 8		N2 Event Interrupt Flag Sta	tus bit						
		ot request has occurred ot request has not occurred							
bit 7	C2RXIF: ECAN2 Receive Data Ready Interrupt Flag Status bit								
		ot request has occurred							
		ot request has not occurred							
bit 6	INT4IF: Ex	ternal Interrupt 4 Flag Statu	is bit						
		ot request has occurred							
		ot request has not occurred							
bit 5		ternal Interrupt 3 Flag Statu	is bit						
	 1 = Interrupt request has occurred 0 = Interrupt request has not occurred 								
bit 4		r9 Interrupt Flag Status bit							
		ot request has occurred							
		ot request has not occurred							
bit 3	T8IF: Time	r8 Interrupt Flag Status bit							
		ot request has occurred							
	0 = Interru	ot request has not occurred							
bit 2		2C2 Master Events Interrup	t Flag Status bit						
		ot request has occurred							
	0 = Interru	ot request has not occurred							

REGISTER 7-8: IFS3: INTERRUPT FLAG STATUS REGISTER 3 (CONTINUED)

- bit 1 SI2C2IF: I2C2 Slave Events Interrupt Flag Status bit
 - 1 = Interrupt request has occurred
- 0 = Interrupt request has not occurred

 bit 0
 T7IF: Timer7 Interrupt Flag Status bit
 - to **I/IF:** Inner/Interrupt Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred



扫一扫上面的二维码图案,加我为朋友。



REGISTER 7-9: IFS4: INTERRUPT FLAG STATUS REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—
bit 15						

							扫一扫上面的二维码	马图案,加我为朋友。
R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	
C2TXIF	C1TXIF	DMA7IF	DMA6IF	_	U2EIF	U1EIF	FLTBIF	
bit 7	•	•	•				bit 0	

Legend:									
R = Readable bit		W = Writable bit	U = Unimplemented bit	, read as '0'					
-n = Value a	at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown					
bit 15-8	Unimple	Unimplemented: Read as '0'							
bit 7	C2TXIF:	ECAN2 Transmit Data Requ	est Interrupt Flag Status bit						
	1 = Interrupt request has occurred								
		rupt request has not occurred							
bit 6		ECAN1 Transmit Data Requ	est Interrupt Flag Status bit						
	 1 = Interrupt request has occurred 0 = Interrupt request has not occurred 								
bit 5	DMA7IF: DMA Channel 7 Data Transfer Complete Interrupt Flag Status bit								
DIL D	1 = Interrupt request has occurred								
	0 = Interrupt request has not occurred								
bit 4	DMA6IF: DMA Channel 6 Data Transfer Complete Interrupt Flag Status bit								
	1 = Interrupt request has occurred								
		0 = Interrupt request has not occurred							
bit 3	Unimple	mented: Read as '0'							
bit 2	U2EIF: U	JART2 Error Interrupt Flag St	atus bit						
	1 = Interr	rupt request has occurred							
	0 = Interrupt request has not occurred								
bit 1	U1EIF: UART1 Error Interrupt Flag Status bit								
		rupt request has occurred							
	0 = Interrupt request has not occurred								
bit 0	FLTBIF:	PWM Fault B Interrupt Flag S	Status bit						
	1 = Interrupt request has occurred								
	0 = Interr	rupt request has not occurred	1						



REGISTER 7-10: IEC0: INTERRUPT ENABLE CONTROL REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE
bit 15						L

							扫一扫上面的二维码图案,	_ 加我为
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INTOIE	1
bit 7							bit 0]

Legend:									
R = Readable bit -n = Value at POR		W = Writable bit	U = Unimplemented bit,						
		'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown					
bit 15	Unimple	mented: Read as '0'							
bit 14	DMA1IE	: DMA Channel 1 Data Trans	fer Complete Interrupt Enable	bit					
	1 = Inter	rupt request enabled							
		rupt request not enabled							
bit 13		ADC1 Conversion Complete I	nterrupt Enable bit						
		rupt request enabled							
hi+ 10		rupt request not enabled	- Enchla hit						
bit 12		UART1 Transmitter Interrupt rupt request enabled	Enable bit						
		rupt request not enabled							
bit 11		UART1 Receiver Interrupt E	nable bit						
		rupt request enabled							
	0 = Inter	rupt request not enabled							
bit 10	SPI1IE: S	SPI1IE: SPI1 Event Interrupt Enable bit							
		rupt request enabled							
		rupt request not enabled							
bit 9		: SPI1 Error Interrupt Enable	bit						
		rupt request enabled rupt request not enabled							
bit 8		ner3 Interrupt Enable bit							
		rupt request enabled							
		rupt request not enabled							
bit 7	T2IE: Tir	ner2 Interrupt Enable bit							
		rupt request enabled							
		rupt request not enabled							
bit 6		Dutput Compare Channel 2 Ir	nterrupt Enable bit						
		rupt request enabled rupt request not enabled							
bit 5		put Capture Channel 2 Interr	unt Enable bit						
DIL D		rupt request enabled							
		rupt request not enabled							
bit 4			fer Complete Interrupt Enable	bit					
		rupt request enabled							
	0 = Inter	rupt request not enabled							
bit 3		ner1 Interrupt Enable bit							
		rupt request enabled							
	0 = Inter	rupt request not enabled							

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REGISTER 7-10: IEC0: INTERRUPT ENABLE CONTROL REGISTER 0 (CONTINUED)

bit 2	OC1IE: Output Compare Channel 1 Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request not enabled
bit 1	IC1IE: Input Capture Channel 1 Interrupt Enable bit
	1 = Interrupt request enabled0 = Interrupt request not enabled
bit 0	INTOIE: External Interrupt 0 Enable bit
	1 = Interrupt request enabled

0 = Interrupt request not enabled

扫一扫上面的二维码图案,加我为朋友。



REGISTER 7-11: IEC1: INTERRUPT ENABLE CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE
bit 15			•			L

-							扫一扫上面的二维码图案,	加拔为加
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	1
IC8IE	IC7IE	AD2IE	INT1IE	CNIE	—	MI2C1IE	SI2C1IE	ĺ
bit 7							bit 0	1

Legend:										
R = Readab	le bit	W = Writable bit	U = Unimplemented bit,	read as '0'						
-n = Value at POR		'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown						
bit 15		JART2 Transmitter Interrupt	Enable bit							
		upt request enabled upt request not enabled								
bit 14		JART2 Receiver Interrupt E	nable hit							
		ipt request enabled								
		ipt request not enabled								
bit 13	INT2IE: E	xternal Interrupt 2 Enable bit	t							
		ipt request enabled								
1.1.40		ipt request not enabled								
bit 12		er5 Interrupt Enable bit								
		 1 = Interrupt request enabled 0 = Interrupt request not enabled 								
bit 11		T4IE: Timer4 Interrupt Enable bit								
		1 = Interrupt request enabled								
	0 = Interru	upt request not enabled								
bit 10		OC4IE: Output Compare Channel 4 Interrupt Enable bit								
		1 = Interrupt request enabled 0 = Interrupt request not enabled								
bit 9			terrupt Enable bit							
		OC3IE: Output Compare Channel 3 Interrupt Enable bit 1 = Interrupt request enabled								
		upt request not enabled								
bit 8	DMA2IE:	DMA Channel 2 Data Transf	fer Complete Interrupt Enable	e bit						
		upt request enabled								
bit 7		upt request not enabled	unt Enchlo hit							
	-	IC8IE: Input Capture Channel 8 Interrupt Enable bit 1 = Interrupt request enabled								
		ipt request not enabled								
bit 6	IC7IE: Inp	ut Capture Channel 7 Interro	upt Enable bit							
	1 = Interru	1 = Interrupt request enabled								
		upt request not enabled								
bit 5		DC2 Conversion Complete I	nterrupt Enable bit							
		1 = Interrupt request enabled 0 = Interrupt request not enabled								
bit 4		xternal Interrupt 1 Enable bit	t							
		upt request enabled	-							
	0 = Interru	upt request not enabled								

REGISTER 7-11: IEC1: INTERRUPT ENABLE CONTROL REGISTER 1 (CONTINUED)

bit 3	CNIE: Input Change Notification Interrupt Enable bit
	1 = Interrupt request enabled
	0 = Interrupt request not enabled
bit 2	Unimplemented: Read as '0'

- bit 1 MI2C1IE: I2C1 Master Events Interrupt Enable bit
 - 1 = Interrupt request enabled
 - 0 = Interrupt request not enabled
- bit 0 SI2C1IE: I2C1 Slave Events Interrupt Enable bit
 - 1 = Interrupt request enabled
 - 0 = Interrupt request not enabled





REGISTER 7-12: IEC2: INTERRUPT ENABLE CONTROL REGISTER 2

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0 •
T6IE	DMA4IE	—	OC8IE	OC7IE	OC6IE	OC5IE
bit 15						

							扫一扫上面的二维码图案,	加拔为月
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
IC5IE	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	1
bit 7							bit 0]

Legend:						
R = Readab	le bit	W = Writable bit	U = Unimplemented bit,	read as '0'		
-n = Value a	t POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		
bit 15	1 = Interi	ner6 Interrupt Enable bit rupt request enabled rupt request not enabled				
bit 14	 DMA4IE: DMA Channel 4 Data Transfer Complete Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request not enabled 					
bit 13	Unimple	mented: Read as '0'				
bit 12	OC8IE: Output Compare Channel 8 Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request not enabled					
bit 11 OC7IE: Output Compare Channel 7 Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request not enabled						
bit 10						
bit 9	1 = Interi	Dutput Compare Channel 5 Ir rupt request enabled rupt request not enabled	nterrupt Enable bit			
bit 8	1 = Interi	put Capture Channel 6 Interr rupt request enabled rupt request not enabled	upt Enable bit			
bit 7	1 = Interi	put Capture Channel 5 Interr upt request enabled upt request not enabled	upt Enable bit			
bit 6	1 = Interi	put Capture Channel 4 Interr upt request enabled upt request not enabled	upt Enable bit			
bit 5	1 = Interi	put Capture Channel 3 Interr upt request enabled upt request not enabled	upt Enable bit			
bit 4	1 = Interi	DMA Channel 3 Data Trans upt request enabled upt request not enabled	fer Complete Interrupt Enable	e bit		
bit 3	C1IE: EC 1 = Interr	CAN1 Event Interrupt Enable rupt request enabled rupt request not enabled	bit			

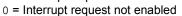
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REGISTER 7-12: IEC2: INTERRUPT ENABLE CONTROL REGISTER 2 (CONTINUED)

bit 2	C1RXIE: ECAN1 Receive Data Ready Interrupt Enable bit
	1 = Interrupt request enabled
	0 = Interrupt request not enabled
bit 1	SPI2IE: SPI2 Event Interrupt Enable bit
	1 = Interrupt request enabled
	0 = Interrupt request not enabled
bit 0	SPI2EIE: SPI2 Error Interrupt Enable bit
	 Left of a start of a start of the start

1 = Interrupt request enabled



扫一扫上面的二维码图案,加我为朋友。



REGISTER 7-13: IEC3: INTERRUPT ENABLE CONTROL REGISTER 3

R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
FLTAIE	—	DMA5IE	—	—	QEIIE	PWMIE
bit 15						

						1	3一扫上面的二维码图案,	加我产
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
C2RXIE	INT4IE	INT3IE	T9IE	T8IE	MI2C2IE	SI2C2IE	T7IE	1
bit 7							bit 0]

Legend:				
R = Readabl	e bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at	POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 15	1 = Interrup	VM Fault A Interrupt Enable t request enabled t request not enabled	e bit	
bit 14	-	ented: Read as '0'		
bit 13	1 = Interrup	MA Channel 5 Data Transf t request enabled t request not enabled	er Complete Interrupt Enable	bit
bit 12-11	Unimpleme	ented: Read as '0'		
bit 10	1 = Interrup	Event Interrupt Enable bit t request enabled t request not enabled		
bit 9	1 = Interrup	VM Error Interrupt Enable b t request enabled t request not enabled	Dit	
bit 8	1 = Interrup	N2 Event Interrupt Enable t t request enabled t request not enabled	Dit	
bit 7	1 = Interrup	CAN2 Receive Data Ready t request enabled t request not enabled	Interrupt Enable bit	
bit 6	1 = Interrup	ernal Interrupt 4 Enable bit t request enabled t request not enabled		
bit 5	1 = Interrup	ernal Interrupt 3 Enable bit t request enabled t request not enabled		
bit 4	T9IE: Timer 1 = Interrup	9 Interrupt Enable bit t request enabled t request not enabled		
bit 3	T8IE: Timer	8 Interrupt Enable bit t request enabled t request not enabled		
bit 2	MI2C2IE: I2 1 = Interrup	2C2 Master Events Interrup t request enabled t request not enabled	t Enable bit	



REGISTER 7-13: IEC3: INTERRUPT ENABLE CONTROL REGISTER 3 (CONTINUED)

- bit 1 SI2C2IE: I2C2 Slave Events Interrupt Enable bit
 - 1 = Interrupt request enabled
 - 0 = Interrupt request not enabled
 T7IE: Timer7 Interrupt Enable bit
 - 1 = Interrupt request enabled

bit 0

0 = Interrupt request not enabled





REGISTER 7-14: IEC4: INTERRUPT ENABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	_	—	—	—
bit 15						

						担	一扫上面的二维码图案,	加我为朋友。
R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	
C2TXIE	C1TXIE	DMA7IE	DMA6IE	—	U2EIE	U1EIE	FLTBIE	
bit 7	•						bit 0	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8	Unimplemented: Read as '0'
bit 7	C2TXIE: ECAN2 Transmit Data Request Interrupt Enable bit
	 1 = Interrupt request enabled 0 = Interrupt request not enabled
bit 6	C1TXIE: ECAN1 Transmit Data Request Interrupt Enable bit
	1 = Interrupt request enabled0 = Interrupt request not enabled
bit 5	DMA7IE: DMA Channel 7 Data Transfer Complete Enable Status bit
	1 = Interrupt request enabled
	0 = Interrupt request not enabled
bit 4	DMA6IE: DMA Channel 6 Data Transfer Complete Enable Status bit
	1 = Interrupt request enabled
	0 = Interrupt request not enabled
bit 3	Unimplemented: Read as '0'
bit 2	U2EIE: UART2 Error Interrupt Enable bit
	1 = Interrupt request enabled
	0 = Interrupt request not enabled
bit 1	U1EIE: UART1 Error Interrupt Enable bit
	1 = Interrupt request enabled
	0 = Interrupt request not enabled
bit 0	FLTBIE: PWM Fault B Interrupt Enable bit
	1 = Interrupt request enabled
	0 = Interrupt request not enabled



REGISTER 7-15: IPC0: INTERRUPT PRIORITY CONTROL REGISTER 0

					D/M/ 0					
1.7.6.1		10.00-0		10/00-1						
	1111 ~2.02				00111 \2.02					
R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0				
	IC1IP<2:0>				INT0IP<2:0>					
						bit 0				
) bit	W = Writable t	oit	U = Unimple	mented bit, rea	ad as '0'					
POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkn	iown				
Unimpleme	ented: Read as 'c)'								
-										
		-	ity interrupt)							
•		•	- • •							
•										
001 = Interrupt is priority 1										
		abled								
Unimpleme	ented: Read as 'C)'								
OC1IP<2:0	>: Output Compa	re Channel	1 Interrupt Prior	ity bits						
111 = Interr	rupt is priority 7 (h	nighest priori	ity interrupt)							
•										
•										
		abled								
	-									
-			errupt Priority b	vits						
•										
•										
		abled								
	•									
-			/ bits							
•		U	- 1/							
•										
• 001 - Inton										
(0) = men	rupt is priority 1									
	R/W-1 R/	R/W-1 R/W-0 T1IP<2:0> R/W-1 R/W-0 IC1IP<2:0> e bit W = Writable R POR '1' = Bit is set Unimplemented: Read as '0 T1IP<2:0>: Timer1 Interrupt 11 = Interrupt is priority 7 (f . 001 = Interrupt is priority 1 000 = Interrupt source is disa Unimplemented: Read as '0 OC1IP<2:0>: Output Compa 111 = Interrupt is priority 7 (f . 001 = Interrupt source is disa Unimplemented: Read as '0 OC1IP<2:0>: Input Capture C 111 = Interrupt is priority 7 (f . . 001 = Interrupt is priority 7 (f . <	R/W-1 R/W-0 R/W-0 T1IP<2:0> R/W-1 R/W-0 R/W-0 IC1IP<2:0> B bit W = Writable bit POR '1' = Bit is set Unimplemented: Read as '0' T1IP<2:0>: Timer1 Interrupt Priority bits 111 = Interrupt is priority 7 (highest priority) 001 = Interrupt is priority 1 000 = Interrupt source is disabled Unimplemented: Read as '0' OC1IP<2:0>: Output Compare Channel 111 = Interrupt is priority 7 (highest priority) 001 = Interrupt source is disabled Unimplemented: Read as '0' OC1IP<2:0>: Output Compare Channel 111 = Interrupt is priority 1 000 = Interrupt source is disabled Unimplemented: Read as '0' IC1IP<2:0>: Input Capture Channel 1 Int 111 = Interrupt is priority 7 (highest priority) 001 =	R/W-1 R/W-0 R/W-0 U-0 T1IP<2:0> - R/W-1 R/W-0 R/W-0 U-0 IC1IP<2:0> - R/W-1 R/W-0 R/W-0 U-0 IC1IP<2:0> - - IC1IP Bit is set '0' = Bit is cle Unimplemented: Read as '0' Interrupt is priority 1 000 = Interrupt source is disabled Unimplemented: Read as '0' Interrupt is priority 1 000 = Interrupt source is disabled Unimplemented: Read as '0' IC1IP Interrupt is priority 7 III = Interrupt is priority 7 Inigest priority interrupt III = Interrupt is priority 1 000 = Interrupt source is disabled Unimplemented: Read as '0' IIII = Interrupt is priority 1 III = Interrupt is priority 1 000 = Interrupt source is disabled Unimplemen	RW-1 R/W-0 R/W-0 U-0 R/W-1 T1IP<2:0> - R/W-1 R/W-0 R/W-0 U-0 R/W-1 IC1IP<2:0> - - - R/W-1 R/W-0 R/W-0 U-0 R/W-1 IC1IP<2:0> - - - R/W-1 IC1IP<2:0> - - R/W-1 IC1IP<2:0> - - R/W-1 IC1IP R/W-0 R/W-0 R/W-1 IC1IP IC1IP R/W-0 R/W-0 R/W-1 R/W-1 IC1IP R/W-1 R/W-1 R/W-1 R/W-1 IC1IP IC1IP R/W-1 R/W-1 R/W-1 IC1IP R/W-1 IC1IP R/W-1 III Interrupt is priority 1 Interrupt Priority bits II1 III Interrupt is priority 1 Interrupt Priority bits II1 III Interrupt is priority 7 (highest priority interrupt) II1 Interrupt is priority 1 Interrupt is priority 1 Interrupt is priority 1 Interrupt is priority 1 Interrupt i	RW-1 RW-0 RW-0 U-0 RW-1 RW-0 T1IP<2:0> - OC1IP<2:0> - OC1IP<2:0> RW-1 RW-0 RW-0 U-0 R/W-1 R/W-0 IC1IP<2:0> - INTOIP<2:0> - INTOIP<2:0> RW-1 R/W-0 R/W-0 U-0 R/W-1 R/W-0 IC1IP R/W-0 R/W-0 U-0 R/W-1 R/W-0 R/W-1 R/W-0 R/W-0 U-0 R/W-1 R/W-0 IC1IP R/W-0 IV-0 R/W-1 R/W-0 IV-0 R/W-1 R/W-0 R/W-0 U-0 R/W-1 R/W-0 IC1IP IC1IP R/W-0 IV-0 R/W-1 R/W-0 INTOIP IV-1 Bit is unknown INTOIP R/W-1 R/W-0 INTOIP INTOIP R/W-1 INTOIP R/W-1 R/W-1 INTOIP INTOIP INTOIP INTOIP INTOIP<				



REGISTER 7-16: IPC1: INTERRUPT PRIORITY CONTROL REGISTER 1

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0
_		T2IP<2:0>	1011 0	-		OC2IP<2:0
bit 15	•					Ľ

						Ŧ	3一扫上面的维码图案,	加技力
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0	
—		IC2IP<2:0>				DMA0IP<2:0>		
bit 7							bit 0	

Legend:									
R = Readab	le bit	W = Writable bit	U = Unimplemented bit,	read as '0'					
-n = Value a	t POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown					
bit 15	Unimple	emented: Read as '0'							
bit 14-12	-		pite						
	T2IP<2:0>: Timer2 Interrupt Priority bits 111 = Interrupt is priority 7 (highest priority interrupt)								
	•	iterrupt is priority 7 (nightest p	nonty interrupt)						
	•								
	•								
		Iterrupt is priority 1 Iterrupt source is disabled							
bit 11		emented: Read as '0'							
bit 10-8	-	2:0>: Output Compare Chan	nel 2 Interrupt Priority bits						
		<pre>111 = Interrupt is priority 7 (highest priority interrupt)</pre>							
	•								
	•								
		iterrupt is priority 1 iterrupt source is disabled							
bit 7	Unimple	emented: Read as '0'							
bit 6-4	IC2IP<2:0>: Input Capture Channel 2 Interrupt Priority bits								
	111 = I n	terrupt is priority 7 (highest p	riority interrupt)						
	•								
	•								
	• 001 = In	terrunt is priority 1							
	001 = Interrupt is priority 1 000 = Interrupt source is disabled								
bit 3		emented: Read as '0'							
bit 2-0	-		Transfer Complete Interrupt F	Priority bits					
		terrupt is priority 7 (highest p							
	•								
	•								
	•								
		terrupt is priority 1							
	000 = In	terrupt source is disabled							



图案.

bit 0

REGISTER 7-17: **IPC2: INTERRUPT PRIORITY CONTROL REGISTER 2** U-0 R/W-1 R/W-0 R/W-0 U-0 R/W-1 R/W-0 U1RXIP<2:0> ____ SPI1IP<2:0> ____ bit 15 U-0 R/W-1 R/W-0 R/W-0 U-0 R/W-1 R/W-0 R/W-0 SPI1EIP<2:0> T3IP<2:0> ____ bit 7 Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 Unimplemented: Read as '0' bit 14-12 U1RXIP<2:0>: UART1 Receiver Interrupt Priority bits 111 = Interrupt is priority 7 (highest priority interrupt) 001 = Interrupt is priority 1 000 = Interrupt source is disabled bit 11 Unimplemented: Read as '0' bit 10-8 SPI1IP<2:0>: SPI1 Event Interrupt Priority bits 111 = Interrupt is priority 7 (highest priority interrupt) 001 = Interrupt is priority 1 000 = Interrupt source is disabled bit 7 Unimplemented: Read as '0' bit 6-4 SPI1EIP<2:0>: SPI1 Error Interrupt Priority bits 111 = Interrupt is priority 7 (highest priority interrupt) 001 = Interrupt is priority 1 000 = Interrupt source is disabled bit 3 Unimplemented: Read as '0' T3IP<2:0>: Timer3 Interrupt Priority bits bit 2-0 111 = Interrupt is priority 7 (highest priority interrupt) 001 = Interrupt is priority 1 000 = Interrupt source is disabled



REGISTER 7-18: IPC3: INTERRUPT PRIORITY CONTROL REGISTER 3

						0_0_000
U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0
	_		_			DMA1IP<2:0
bit 15						

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	
		AD1IP<2:0>				U1TXIP<2:0>	
bit 7							bit 0

Legend:										
R = Readab	ole bit	W = Writable bit	U = Unimplemented bit	, read as '0'						
-n = Value a	at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown						
bit 15-11	Unimple	emented: Read as '0'								
bit 10-8	DMA1IP	DMA1IP<2:0>: DMA Channel 1 Data Transfer Complete Interrupt Priority bits								
	111 = In	terrupt is priority 7 (highest p	riority interrupt)							
	•									
	•									
	• 001 = In	terrunt is priority 1								
	001 = Interrupt is priority 1 000 = Interrupt source is disabled									
bit 7										
bit 6-4	AD1IP<2:0>: ADC1 Conversion Complete Interrupt Priority bits									
	111 = Interrupt is priority 7 (highest priority interrupt)									
	•									
	•									
	•									
	001 = Interrupt is priority 1 000 = Interrupt source is disabled									
h :+ 0		•								
bit 3	-	emented: Read as '0'								
bit 2-0		<2:0>: UART1 Transmitter In								
	111 = In	terrupt is priority 7 (highest p	riority interrupt)							
	•									
	•									
	001 = In	terrupt is priority 1								
	000 = In	terrupt source is disabled								



REGISTER 7-19: IPC4: INTERRUPT PRIORITY CONTROL REGISTER 4

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0
—		CNIP<2:0>		—	—	—
bit 15						

							扫一扫上面的二维码	3图案,加我为朋友。
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0	
—		MI2C1IP<2:0>		_		SI2C1IP<2:0>		
bit 7							bit 0	

Legend:										
R = Readab	le bit	W = Writable bit	U = Unimplemented bit,	, read as '0'						
-n = Value a	t POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown						
bit 15	Unimple	emented: Read as '0'								
bit 14-12	CNIP<2:0>: Change Notification Interrupt Priority bits									
	111 = In	terrupt is priority 7 (highest p	riority interrupt)							
	•									
	•									
	•	•								
	001 = Interrupt is priority 1 000 = Interrupt source is disabled									
bit 11-7	Unimplemented: Read as '0'									
oit 6-4	MI2C1IP<2:0>: I2C1 Master Events Interrupt Priority bits									
	<pre>111 = Interrupt is priority 7 (highest priority interrupt)</pre>									
	•									
	•									
	• 001 – In	terrupt is priority 1								
	001 = Interrupt is priority 1 000 = Interrupt source is disabled									
bit 3		emented: Read as '0'								
bit 2-0	-	<2:0>: I2C1 Slave Events Int	forrupt Priority bits							
DIL 2-0										
	111 = Interrupt is priority 7 (highest priority interrupt)									
	•									
	•									
	001 = ln	terrupt is priority 1								
		terrupt source is disabled								



REGISTER 7-20: IPC5: INTERRUPT PRIORITY CONTROL REGISTER 5

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0
—		IC8IP<2:0>		—		IC7IP<2:0
bit 15						

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	<u></u>
		AD2IP<2:0>		—		INT1IP<2:0>	
bit 7							bit 0

Legend:				
R = Readabl	e bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at	POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 15	Unimple	emented: Read as '0'		
bit 14-12	IC8IP<2	:0>: Input Capture Channel 8	3 Interrupt Priority bits	
	111 = In	nterrupt is priority 7 (highest p	priority interrupt)	
	•			
	•			
	001 = In	iterrupt is priority 1		
		iterrupt source is disabled		
bit 11	Unimple	emented: Read as '0'		
bit 10-8	IC7IP<2	:0>: Input Capture Channel 7	7 Interrupt Priority bits	
	111 = In	nterrupt is priority 7 (highest p	priority interrupt)	
	•			
	•			
	001 = In	terrupt is priority 1		
	000 = In	terrupt source is disabled		
bit 7	Unimple	emented: Read as '0'		
bit 6-4	AD2IP<	2:0>: ADC2 Conversion Corr	plete Interrupt Priority bits	
	111 = In	terrupt is priority 7 (highest p	priority interrupt)	
	•			
	•			
	001 = In	terrupt is priority 1		
	000 = In	terrupt source is disabled		
bit 3	Unimple	emented: Read as '0'		
bit 2-0	INT1IP<	2:0>: External Interrupt 1 Pri	ority bits	
	111 = In	terrupt is priority 7 (highest p	priority interrupt)	
	•			
	•			
	001 = In	terrupt is priority 1		
		iterrupt source is disabled		



REGISTER 7-21: IPC6: INTERRUPT PRIORITY CONTROL REGISTER 6 U-0 R/W-1 R/W-0 U-0 R/W-1 R/W-0

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	
—		T4IP<2:0>				OC4IP<2:0>	
bit 15	-						bit-8
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
_		OC3IP<2:0>				DMA2IP<2:0>	
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable b	oit	U = Unimpler	mented bit, rea	ad as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	Unimpleme	ented: Read as 'o)'				
bit 14-12	T4IP<2:0>:	Timer4 Interrupt	Priority bits				
		rupt is priority 7 (h	-	ity interrupt)			
	•						
	•						
	001 = Inter	rupt is priority 1					
		rupt source is disa	abled				
bit 11	Unimpleme	ented: Read as 'o)'				
bit 10-8	OC4IP<2:0	>: Output Compa	re Channel	4 Interrupt Prior	ity bits		
	111 = Inter	rupt is priority 7 (ł	nighest prior	ity interrupt)			
	•						
	•						
	001 = Inter	rupt is priority 1					
		rupt source is disa	abled				
bit 7	Unimpleme	ented: Read as '0)'				
bit 6-4	OC3IP<2:0	>: Output Compa	re Channel	3 Interrupt Prior	ity bits		
	111 = Inter	rupt is priority 7 (h	nighest prior	ity interrupt)			
	•						
	•						
	001 = Inter	rupt is priority 1					
		rupt source is disa	abled				
bit 3	Unimpleme	ented: Read as 'o)'				
bit 2-0	DMA2IP<2	:0>: DMA Channe	el 2 Data Tra	Insfer Complete	Interrupt Pric	ority bits	
	111 = Inter	rupt is priority 7 (h	nighest prior	ity interrupt)			
	•						
	•						
	-						
	001 = Inter	rupt is priority 1					



REGISTER 7-22: IPC7: INTERRUPT PRIORITY CONTROL REGISTER 7

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0
—		U2TXIP<2:0>				U2RXIP<2:0
bit 15						L

							扫一扫上面的二维码图案,	加我为朋
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0	
—		INT2IP<2:0>		_		T5IP<2:0>		1
bit 7							bit 0	

Legend:				
R = Readab	le bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value a	t POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 15	Unimple	mented: Read as '0'		
bit 14-12	U2TXIP- 111 = In 001 = In	2:0>: UART2 Transmitter In terrupt is priority 7 (highest p terrupt is priority 1		
		terrupt source is disabled		
bit 11	-	mented: Read as '0'		
bit 10-8	111 = In • • • • •	<2:0>: UART2 Receiver Inte terrupt is priority 7 (highest p terrupt is priority 1 terrupt source is disabled		
bit 7		mented: Read as '0'		
bit 6-4	111 = In • • • • •	2:0>: External Interrupt 2 Pri terrupt is priority 7 (highest p terrupt is priority 1 terrupt source is disabled		
bit 3	Unimple	mented: Read as '0'		
bit 2-0	111 = In • • • • •	D>: Timer5 Interrupt Priority t terrupt is priority 7 (highest p terrupt is priority 1 terrupt source is disabled		



REGISTER 7-23: IPC8: INTERRUPT PRIORITY CONTROL REGISTER 8

	<i>i</i> -25. ii Co		NONT							
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	- EM-D			
_		C1IP<2:0>		—		C1RXIP<2:0>				
it 15	·						bit-8			
							扫一扫上面的二维码图			
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0			
_		SPI2IP<2:0>				SPI2EIP<2:0>				
bit 7							bit 0			
Legend:										
R = Readabl		W = Writable t	bit	U = Unimple	mented bit, re	ad as '0'				
n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	iown			
bit 15	-	ented: Read as '0								
bit 14-12		ECAN1 Event In	-	-						
	111 = Inter	rupt is priority 7 (h	ighest prior	ity interrupt)						
	•									
	•									
		rupt is priority 1								
	000 = Inter	rupt source is disa	abled							
bit 11	Unimpleme	ented: Read as '0	2							
oit 10-8	C1RXIP<2:0>: ECAN1 Receive Data Ready Interrupt Priority bits									
	111 = Interrupt is priority 7 (highest priority interrupt)									
	•									
	•									
	001 = Inter	rupt is priority 1								
	000 = Inter	rupt source is disa	abled							
bit 7	Unimpleme	ented: Read as '0	2							
bit 6-4	SPI2IP<2:0	>: SPI2 Event Int	errupt Priori	ty bits						
	111 = Inter	rupt is priority 7 (h	ighest prior	ity interrupt)						
	•									
	•									
	• 001 = Inter	rupt is priority 1								
		rupt source is disa	abled							
bit 3		ented: Read as '0								
oit 2-0	-	:0>: SPI2 Error In		ity bits						
		rupt is priority 7 (h	-	-						
	•			/						
	•									
	• 001 = Inter	rupt is priority 1								
		rupt source is disa	abled							



REGISTER 7-24: IPC9: INTERRUPT PRIORITY CONTROL REGISTER 9

						<u></u>
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0
—		IC5IP<2:0>				IC4IP<2:0
bit 15						

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	
—		IC3IP<2:0>		—		DMA3IP<2:0>	
bit 7							bit 0

Legend:										
R = Readable	e bit	W = Writable bit	U = Unimplemented bit,	, read as '0'						
-n = Value at	POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown						
bit 15	Unimple	mented: Read as '0'								
bit 14-12	IC5IP<2:0>: Input Capture Channel 5 Interrupt Priority bits									
	111 = In	terrupt is priority 7 (highest p	priority interrupt)							
	•									
	•									
	001 = In	terrupt is priority 1								
		terrupt source is disabled								
bit 11	Unimple	mented: Read as '0'								
bit 10-8	IC4IP<2:0>: Input Capture Channel 4 Interrupt Priority bits									
	111 = In	terrupt is priority 7 (highest p	priority interrupt)							
	•									
	•									
	• 001 = In	terrupt is priority 1								
		terrupt source is disabled								
bit 7	Unimple	mented: Read as '0'								
bit 6-4	IC3IP<2:	:0>: Input Capture Channel 3	3 Interrupt Priority bits							
	111 = In	terrupt is priority 7 (highest p	priority interrupt)							
	•									
	•									
	001 = In	terrupt is priority 1								
		terrupt source is disabled								
bit 3	Unimple	mented: Read as '0'								
bit 2-0	DMA3IP	<2:0>: DMA Channel 3 Data	Transfer Complete Interrupt F	Priority bits						
	111 = In	terrupt is priority 7 (highest p	priority interrupt)							
	•									
	•									
	• 001 = In	terrupt is priority 1								
		terrupt source is disabled								



REGISTER 7-25: IPC10: INTERRUPT PRIORITY CONTROL REGISTER 10

			_							
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0				
—		OC7IP<2:0>		—		OC6IP<2:0>				
oit 15							bit-8			
							扫一扫上面的二维码图案,加我为用			
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0			
_		OC5IP<2:0>		—		IC6IP<2:0>				
bit 7							bit 0			
Legend:										
R = Readable	e bit	W = Writable b	it	U = Unimpler	mented bit, rea	ad as '0'				
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown			
bit 15	Unimplemer	nted: Read as '0	,							
bit 14-12	-	: Output Compar		Interrupt Prior	ity bits					
		.pt is priority 7 (h		-						
	•									
	•									
	• 001 = Interru	upt is priority 1								
		ipt source is disa	bled							
bit 11	Unimplemer	nted: Read as '0	,							
bit 10-8	OC6IP<2:0>: Output Compare Channel 6 Interrupt Priority bits									
	111 = Interrupt is priority 7 (highest priority interrupt)									
	•									
	•									
	• 001 = Interrupt is priority 1									
		ipt is priority i ipt source is disa	bled							
bit 7		nted: Read as '0								
bit 6-4	-	: Output Compar		Latorrupt Drior	ity hito					
DIL 0-4		pt is priority 7 (h		•	ity bits					
	•		ignest phon	ty interrupt)						
	•									
	•									
		upt is priority 1 upt source is disa	bled							
bit 3	Unimplemer	nted: Read as '0	,							
bit 2-0	IC6IP<2:0>:	Input Capture Cl	nannel 6 Inte	errupt Priority b	its					
	•			- • • •						
	•									
	•	upt is priority 1								



REGISTER 7-26: IPC11: INTERRUPT PRIORITY CONTROL REGISTER 11

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0
_		T6IP<2:0>				DMA4IP<2:0>
bit 15						Ľ

						1		加我为朋
U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0	
—	—	—	_			OC8IP<2:0>		1
bit 7							bit 0]

Legend:										
R = Readab	le bit	W = Writable bit	U = Unimplemented bit, read as '0'							
-n = Value a	It POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown						
bit 15	Unimple	mented: Read as '0'								
bit 14-12	T6IP<2:0)>: Timer6 Interrupt Priority b	pits							
	111 = In i	terrupt is priority 7 (highest p	riority interrupt)							
	•									
	•									
	• 001 = Ini	terrupt is priority 1								
		terrupt source is disabled								
bit 11	Unimplemented: Read as '0'									
bit 10-8	DMA4IP<2:0>: DMA Channel 4 Data Transfer Complete Interrupt Priority bits									
	111 = Interrupt is priority 7 (highest priority interrupt)									
	•									
	•									
	•	•								
	001 = Interrupt is priority 1 000 = Interrupt source is disabled									
h:+ 7 0		•								
bit 7-3	-	mented: Read as '0'								
bit 2-0		2:0>: Output Compare Chan								
	111 = Ini	terrupt is priority 7 (highest p	riority interrupt)							
	•									
	•									
	001 = In	terrupt is priority 1								
	000 = In	terrupt source is disabled								



REGISTER 7-27: IPC12: INTERRUPT PRIORITY CONTROL REGISTER 12

		_								
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	- HW-D			
_		T8IP<2:0>				MI2C2IP<2:0>				
t 15							• bit 8			
							扫一扫上面的二维			
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0			
		SI2C2IP<2:0>				T7IP<2:0>				
it 7							bit 0			
egend:										
R = Readable	bit	W = Writable b	it	U = Unimpler	mented bit, re	ad as '0'				
n = Value at I	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own			
oit 15	Unimpleme	ented: Read as '0	,							
bit 14-12	-	Timer8 Interrupt								
		rupt is priority 7 (h	-	tv interrupt)						
	•		.g	·, ·····						
	•									
	• 001 = Interr	rupt is priority 1								
		rupt source is disa	bled							
pit 11		ented: Read as '0								
oit 10-8	MI2C2IP<2:0>: I2C2 Master Events Interrupt Priority bits									
	111 = Interrupt is priority 7 (highest priority interrupt)									
	•									
	•									
	001 = Interr	rupt is priority 1								
		rupt source is disa	bled							
pit 7	Unimpleme	ented: Read as '0	,							
oit 6-4	SI2C2IP<2:	0>: I2C2 Slave E	vents Interru	upt Priority bits						
	111 = Interr	rupt is priority 7 (h	ighest priori	ty interrupt)						
	•									
	•									
	001 = Interr	rupt is priority 1								
		rupt source is disa	bled							
oit 3	Unimpleme	ented: Read as '0	,							
it 2-0	T7IP<2:0>:	Timer7 Interrupt	Priority bits							
	111 = Interr	rupt is priority 7 (h	ighest priori	ty interrupt)						
	•									
	•									
	0.01 = Interr	rupt is priority 1								
		upt source is disa								



REGISTER 7-28: IPC13: INTERRUPT PRIORITY CONTROL REGISTER 13

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0
—		C2RXIP<2:0>		_		INT4IP<2:0
bit 15						

-							扫一扫上面的二维码图案,	加我为朋
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0	
—		INT3IP<2:0>				T9IP<2:0>		1
bit 7							bit 0]

Legend:									
R = Readab	le bit	W = Writable bit	U = Unimplemented bit,	read as '0'					
-n = Value a	t POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown					
bit 15	Unimple	emented: Read as '0'							
bit 14-12	C2RXIP	<2:0>: ECAN2 Receive Data	Ready Interrupt Priority bits						
	111 = I n	terrupt is priority 7 (highest p	priority interrupt)						
	•								
	•								
	001 = In	terrupt is priority 1							
		terrupt source is disabled							
bit 11	Unimple	emented: Read as '0'							
bit 10-8	INT4IP<2:0>: External Interrupt 4 Priority bits								
	111 = Interrupt is priority 7 (highest priority interrupt)								
	•								
	•								
		terrupt is priority 1 terrupt source is disabled							
bit 7	Unimple	emented: Read as '0'							
bit 6-4	INT3IP<	2:0>: External Interrupt 3 Pri	ority bits						
	111 = I n	terrupt is priority 7 (highest p	priority interrupt)						
	•								
	•								
	• 001 = Interrupt is priority 1								
		terrupt source is disabled							
bit 3	Unimple	emented: Read as '0'							
bit 2-0	T9IP<2:	0>: Timer9 Interrupt Priority I	pits						
	111 = In	terrupt is priority 7 (highest p	priority interrupt)						
	•								
	•								
	001 = In	terrupt is priority 1							
		terrupt source is disabled							



REGISTER 7-29: IPC14: INTERRUPT PRIORITY CONTROL REGISTER 14

U-0	U-1	U-0	U-0	U-0	R/W-1	R/W-0	
 bit 15	—	—	—	_		QEIIP<2:0>	

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
_		PWMIP<2:0>		—		C2IP<2:0>	
bit 7							bit 0

Legend:				
R = Readab	le bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value a	It POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 15-11	Unimple	mented: Read as '0'		
bit 10-8	-	:0>: QEI Interrupt Priority bits	S	
	111 = Int • • • • •	errupt is priority 7 (highest p		
h:+ 7		errupt source is disabled		
bit 7	•	mented: Read as '0'	h 14-	
bit 6-4		2:0>: PWM Interrupt Priority		
	111 = Int •	errupt is priority 7 (highest p	riority interrupt)	
	•			
	•			
		errupt is priority 1 errupt source is disabled		
bit 3	Unimple	mented: Read as '0'		
bit 2-0	C2IP<2:0	>: ECAN2 Event Interrupt P	riority bits	
	111 = Int •	errupt is priority 7 (highest p	riority interrupt)	
		errupt is priority 1 errupt source is disabled		



REGISTER 7-30: IPC15: INTERRUPT PRIORITY CONTROL REGISTER 15

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0
—		FLTAIP<2:0>		—	—	_
bit 15						

							扫一扫上面的二维码图案,	加我为朋
U-0	R/W-1	R/W-0	R/W-0	U-0	U-1	U-0	U-0	
		DMA5IP<2:0>			_	—	—	
bit 7							bit 0	

Legend:				
R = Readab	le bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value a	t POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 15	Unimple	mented: Read as '0'		
bit 14-12	•	2:0>: PWM Fault A Interrupt	Priority hits	
511 14-12		terrupt is priority 7 (highest p	•	
	•			
		terrupt is priority 1 terrupt source is disabled		
bit 11-7	Unimple	mented: Read as '0'		
bit 6-4		<2:0>: DMA Channel 5 Data terrupt is priority 7 (highest p	Transfer Complete Interrupt F riority interrupt)	Priority bits
	•			
		terrupt is priority 1 terrupt source is disabled		
bit 3-0	Unimple	mented: Read as '0'		



REGISTER	7-31: IPC1	6: INTERRUP			REGISTER [·]	16	
U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	
_	—	—	_	—		U2EIP<2:0>	
bit 15							L. bi l 8
							扫一扫上面的二维码图案,加
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—		U1EIP<2:0>		—		FLTBIP<2:0>	
bit 7							bit 0
Legend: R = Readab	le bit	W = Writable	bit	U = Unimple	mented bit, re	ad as '0'	
R = Readab -n = Value a		W = Writable '1' = Bit is set		0' = Unimple 0' = Bit is cle		ad as '0' x = Bit is unkr	nown
bit 15-11 bit 10-8	U2EIP<2:0>	ented: Read as ' >: UART2 Error I rupt is priority 7 (nterrupt Prio	•			
		rupt is priority 1 rupt source is dis	abled				
L 10 🖛			- 1				

bit 7 Unimplemented: Read as '0'

- bit 6-4 U1EIP<2:0>: UART1 Error Interrupt Priority bits 111 = Interrupt is priority 7 (highest priority interrupt) 001 = Interrupt is priority 1 000 = Interrupt source is disabled
- bit 3 Unimplemented: Read as '0' bit 2-0 FLTBIP<2:0>: PWM Fault B Interrupt Priority bits
 - 111 = Interrupt is priority 7 (highest priority interrupt)

- 001 = Interrupt is priority 1
- 000 = Interrupt source is disabled



REGISTER 7-32: IPC17: INTERRUPT PRIORITY CONTROL REGISTER 17

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0
—		C2TXIP<2:0>		—		C1TXIP<2:0>
bit 15						

							扫一扫上面的二维码图案,	_ 加我为朋
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0	
—		DMA7IP<2:0>				DMA6IP<2:0	>	1
bit 7							bit 0]

Legend:				
R = Readable	e bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at	POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 15	Unimple	mented: Read as '0'		
bit 14-12	-		Request Interrupt Priority bits	;
		terrupt is priority 7 (highest p		
	•			
	•			
	• 001 = Ini	terrupt is priority 1		
		terrupt source is disabled		
bit 11	Unimple	mented: Read as '0'		
bit 10-8	C1TXIP<	<2:0>: ECAN1 Transmit Data	Request Interrupt Priority bits	;
	111 = In i	terrupt is priority 7 (highest p	riority interrupt)	
	•			
	•			
	001 = Ini	terrupt is priority 1		
		terrupt source is disabled		
bit 7	Unimple	mented: Read as '0'		
bit 6-4	DMA7IP	<2:0>: DMA Channel 7 Data	Transfer Complete Interrupt F	Priority bits
	111 = In i	terrupt is priority 7 (highest p	riority interrupt)	
	•			
	•			
	001 = In i	terrupt is priority 1		
	000 = In	terrupt source is disabled		
bit 3	Unimple	mented: Read as '0'		
bit 2-0	DMA6IP	<2:0>: DMA Channel 6 Data	Transfer Complete Interrupt F	Priority bits
	111 = In	terrupt is priority 7 (highest p	riority interrupt)	
	•			
	•			
		terrupt is priority 1		
	000 = In	terrupt source is disabled		



REGISTER 7-33: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER

U-0 U-0 U-0 R-0 R-0 R-0 - - - - ILR<3:0>	
bit 15	bit-8
	扫一扫上面的二维
U-0 R-0 R-0 R-0 R-0 R-0 R-0	R-0
WECNUM<6:0>	
bit 7	bit 0
Legend:	
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'	
-n = Value at POR (1' = Bit is set (0' = Bit is cleared x = Bit is un	known
bit 15-12 Unimplemented: Read as '0'	
bit 11-8 ILR<3:0>: New CPU Interrupt Priority Level bits	
1111 = CPU interrupt priority level is 15	
•	
•	
0001 = CPU interrupt priority level is 1	
0000 = CPU interrupt priority level is 0	
0000 = CPU interrupt priority level is 0	
0000 = CPU interrupt priority level is 0bit 7Unimplemented: Read as '0'	
0000 = CPU interrupt priority level is 0bit 7Unimplemented: Read as '0'bit 6-0VECNUM<6:0>: Vector Number of Pending Interrupt bits	
0000 = CPU interrupt priority level is 0bit 7Unimplemented: Read as '0'bit 6-0VECNUM<6:0>: Vector Number of Pending Interrupt bits	
0000 = CPU interrupt priority level is 0bit 7Unimplemented: Read as '0'bit 6-0VECNUM<6:0>: Vector Number of Pending Interrupt bits	



7.4 Interrupt Setup Procedures

7.4.1 INITIALIZATION

To configure an interrupt source, do the following:

- 1. Set the NSTDIS bit (INTCON1<15>) if nested interrupts are not desired.
- Select the user-assigned priority level for the interrupt source by writing the control bits in the appropriate IPCx register. The priority level will depend on the specific application and type of interrupt source. If multiple priority levels are not desired, the IPCx register control bits for all enabled interrupt sources may be programmed to the same non-zero value.

Note:	At a device Reset, the IPCx registers are
	initialized such that all user interrupt
	sources are assigned to priority level 4.

- 3. Clear the interrupt flag status bit associated with the peripheral in the associated IFSx register.
- 4. Enable the interrupt source by setting the interrupt enable control bit associated with the source in the appropriate IECx register.

7.4.2 INTERRUPT SERVICE ROUTINE

The method that is used to declare an Interrupt Service Routine (ISR) and initialize the IVT with the correct vector address will depend on the programming language (i.e., 'C' or assembler) and the language development toolsuite that is used to develop the application. In general, the user must clear the interrupt flag in the appropriate IFSx register for the source of interrupt that the ISR handles. Otherwise, the ISR will be re-entered immediately after exiting the routine. If the ISR is coded in assembly language, it must be terminated using a RETFIE instruction to unstack the saved PC value, SRL value and old CPU priority level.

7.4.3 TRAP SERVICE ROU

A Trap Service Routine (TSR) is c except that the appropriate trap a INTCON1 register must be cleared into the TSR.

7.4.4 INTERRUPT DISABLE 扫一扫上面的二维码图案,加我为朋友。

All user interrupts can be disabled using the following procedure:

- 1. Push the current SR value onto the software stack using the PUSH instruction.
- 2. Force the CPU to priority level 7 by inclusive ORing the value OEh with SRL.

To enable user interrupts, the POP instruction may be used to restore the previous SR value.

Note that only user interrupts with a priority level of 7 or less can be disabled. Trap sources (level 8-level 15) cannot be disabled.

The DISI instruction provides a convenient way to disable interrupts of priority levels 1-6 for a fixed period of time. Level 7 interrupt sources are not disabled by the DISI instruction.

NOTES:



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INT0

8.0 DIRECT MEMORY ACCESS (DMA)

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 22. "Direct Memory Access (DMA)" (DS70182) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 2: Some registers and associated bits
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

Direct Memory Access (DMA) is a very efficient mechanism of copying data between peripheral SFRs (e.g., the UART Receive register and Input Capture 1 buffer) and buffers or variables stored in RAM, with minimal CPU intervention. The DMA controller can automatically copy entire blocks of data without requiring the user software to read or write the peripheral Special Function Registers (SFRs) every time a peripheral interrupt occurs. The DMA controller uses a dedicated bus for data transfers, and therefore, does not steal cycles from the code execution flow of the CPU. To exploit the DMA capability, the corresponding user buffers or variables must be located in DMA RAM.

The dsPIC33FJXXXMCX06A/X08A/X10A peripherals that can utilize DMA are listed in Table 8-1 along with their associated Interrupt Request (IRQ) numbers.

TABLE 8-1: PERIPHERALS SUPPORT

Peripheral



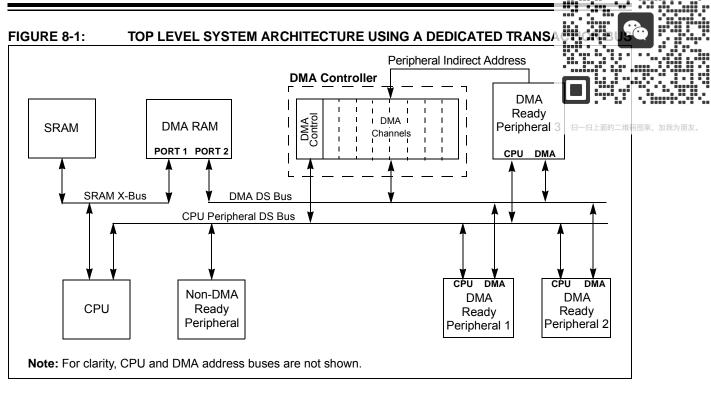
Input Capture 1	1
Input Capture 2	扫一扫上面的二维码图案,加
Output Compare 1	2
Output Compare 2	6
Timer2	7
Timer3	8
SPI1	10
SPI2	33
UART1 Reception	11
UART1 Transmission	12
UART2 Reception	30
UART2 Transmission	31
ADC1	13
ADC2	21
ECAN1 Reception	34
ECAN1 Transmission	70
ECAN2 Reception	55
ECAN2 Transmission	71

The DMA controller features eight identical data transfer channels. Each channel has its own set of control and status registers. Each DMA channel can be configured to copy data, either from buffers stored in dual port DMA RAM to peripheral SFRs, or from peripheral SFRs to buffers in DMA RAM.

The DMA controller supports the following features:

- · Word or byte-sized data transfers.
- Transfers from peripheral to DMA RAM or DMA RAM to peripheral.
- Indirect Addressing of DMA RAM locations with or without automatic post-increment.
- Peripheral Indirect Addressing In some peripherals, the DMA RAM read/write addresses may be partially derived from the peripheral.
- One-Shot Block Transfers Terminating DMA transfer after one block transfer.
- Continuous Block Transfers Reloading DMA RAM buffer start address after every block transfer is complete.
- Ping-Pong Mode Switching between two DMA RAM start addresses between successive block transfers, thereby filling two buffers alternately.
- · Automatic or manual initiation of block transfers.
- Each channel can select from 20 possible sources of data sources or destinations.

For each DMA channel, a DMA interrupt request is generated when a block transfer is complete. Alternatively, an interrupt can be generated when half of the block has been filled.





Each DMAC Channel x (x = 0, 1, 2, 3, 4, 5, 6 or 7) contains the following registers:

 A 16-Bit DMA Channel Control register (DMAxCON)

8.1

- A 16-Bit DMA Channel IRQ Select register (DMAxREQ)
- A 16-Bit DMA RAM Primary Start Address Offset register (DMAxSTA)

 A 16-Bit DMA RAM Secondary Star Offset register (DMAxSTB)



- A 16-Bit DMA Peripheral Address (DMAxPAD)
- A 10-Bit DMA Transfer Count regist

An additional pair of status registers, DMACS0 and DMACS1, are common to all DMAC channels.

REGISTER 8-1: DMAxCON: DMA CHANNEL x CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CHEN	SIZE	DIR	HALF	NULLW	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
—	—	AMODE<1:0>		—	—	MODE	=<1:0>
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	CHEN: Channel Enable bit
DIL 15	1 = Channel enabled
	0 = Channel disabled
bit 14	SIZE: Data Transfer Size bit
bit 14	1 = Byte
	0 = Word
bit 13	DIR: Transfer Direction bit (source/destination bus select)
	1 = Read from DMA RAM address; write to peripheral address
	0 = Read from peripheral address; write to DMA RAM address
bit 12	HALF: Early Block Transfer Complete Interrupt Select bit
	1 = Initiate block transfer complete interrupt when half of the data has been moved
	0 = Initiate block transfer complete interrupt when all of the data has been moved
bit 11	NULLW: Null Data Peripheral Write Mode Select bit
	1 = Null data write to peripheral in addition to DMA RAM write (DIR bit must also be clear)
	0 = Normal operation
bit 10-6	Unimplemented: Read as '0'
bit 5-4	AMODE<1:0>: DMA Channel Operating Mode Select bits
	11 = Reserved
	10 = Peripheral Indirect Addressing mode
	01 = Register Indirect without Post-Increment mode
	00 = Register Indirect with Post-Increment mode
bit 3-2	Unimplemented: Read as '0'
bit 1-0	MODE<1:0>: DMA Channel Operating Mode Select bits
	11 = One-Shot, Ping-Pong modes enabled (one block transfer from/to each DMA RAM buffer)
	10 = Continuous, Ping-Pong modes enabled
	01 = One-Shot, Ping-Pong modes disabled
	00 = Continuous, Ping-Pong modes disabled



REGISTER 8-2: DMAXREQ: DMA CHANNEL x IRQ SELECT REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
FORCE ⁽¹⁾	—	—	—	—	—	—
bit 15						

							扫一扫上面的二维码图
U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	IRQSEL6(2)	IRQSEL5(2)	IRQSEL4(2)	IRQSEL3(2)	IRQSEL2 ⁽²⁾	IRQSEL1(2)	IRQSEL0 ⁽²⁾
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FORCE:** Force DMA Transfer bit⁽¹⁾

1 = Force a single DMA transfer (Manual mode)

0 = Automatic DMA transfer initiation by DMA request

bit 14-7 Unimplemented: Read as '0'

- bit 6-0 IRQSEL<6:0>: DMA Peripheral IRQ Number Select bits⁽²⁾ 0000000-1111111 = DMAIRQ0-DMAIRQ127 selected to be Channel DMAREQ
- **Note 1:** The FORCE bit cannot be cleared by the user. The FORCE bit is cleared by hardware when the forced DMA transfer is complete.

2: See Table 8-1 for a complete listing of IRQ numbers for all interrupt sources.



DMAxSTA: DMA CHANNEL x RAM START ADDRESS OFFSET RE **REGISTER 8-3:**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		R/M-0	
			STA<	:15:8>		<u> </u>		
bit 15						Ľ	bit 8	
						ŧ	3一扫上面的二维码图案,	加我为朋友
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			STA	<7:0>				
bit 7							bit 0	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 STA<15:0>: Primary DMA RAM Start Address bits (source or destination)

DMAxSTB: DMA CHANNEL x RAM START ADDRESS OFFSET REGISTER B **REGISTER 8-4:**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STB	<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STE	3<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			bit	U = Unimplem	nented bit, rea	ad as '0'	
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unkn			nown				

STB<15:0>: Secondary DMA RAM Start Address bits (source or destination) bit 15-0



REGISTER 8-5: DMAXPAD: DMA CHANNEL x PERIPHERAL ADDRESS REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			PAD	<15:8>			
bit 15							bi t *8
							扫一扫上面的二维码图案,加到
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PAI	D<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable bit	t	U = Unimpler	nented bit, rea	ad as '0'	
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown

bit 15-0 PAD<15:0>: Peripheral Address Register bits

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

REGISTER 8-6: DMAxCNT: DMA CHANNEL x TRANSFER COUNT REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	CNT<	9:8> (2)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			CNT<	7:0> (2)			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 Unimplemented: Read as '0'

bit 9-0 CNT<9:0>: DMA Transfer Count Register bits⁽²⁾

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

2: Number of DMA transfers = CNT<9:0> + 1.



REGISTER 8-7: DMACS0: DMA CONTROLLER STATUS REGISTER 0

| R/C-0 |
|--------|--------|--------|--------|--------|--------|--------|
| PWCOL7 | PWCOL6 | PWCOL5 | PWCOL4 | PWCOL3 | PWCOL2 | PWC0_1 |
| bit 15 | | | | | | U |

							——扫上面的二维码图案,	加我为朋友。
R/C-0								
XWCOL7	XWCOL6	XWCOL5	XWCOL4	XWCOL3	XWCOL2	XWCOL1	XWCOL0	
bit 7	•					•	bit 0	

Legend:			C = Clearable bit	t
R = Readable	bit	W = Writable bit	U = Unimplemented bi	t, read as '0'
-n = Value at F	POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 15	1 = Write	Channel 7 Peripheral Write collision detected	e Collision Flag bit	
bit 14	PWCOL6 1 = Write	ite collision detected : Channel 6 Peripheral Write collision detected ite collision detected	e Collision Flag bit	
bit 13	PWCOL5 1 = Write	: Channel 5 Peripheral Write collision detected ite collision detected	e Collision Flag bit	
bit 12	PWCOL4 1 = Write	: Channel 4 Peripheral Write collision detected ite collision detected	e Collision Flag bit	
bit 11	1 = Write	: Channel 3 Peripheral Write collision detected ite collision detected	e Collision Flag bit	
bit 10	1 = Write	: Channel 2 Peripheral Write collision detected ite collision detected	e Collision Flag bit	
bit 9	1 = Write	: Channel 1 Peripheral Write collision detected ite collision detected	e Collision Flag bit	
bit 8	1 = Write	: Channel 0 Peripheral Write collision detected ite collision detected	e Collision Flag bit	
bit 7	1 = Write	: Channel 7 DMA RAM Writ collision detected ite collision detected	e Collision Flag bit	
bit 6	1 = Write	: Channel 6 DMA RAM Writ collision detected ite collision detected	e Collision Flag bit	
bit 5	1 = Write	: Channel 5 DMA RAM Writ collision detected ite collision detected	e Collision Flag bit	
bit 4	1 = Write	: Channel 4 DMA RAM Writ collision detected ite collision detected	e Collision Flag bit	



REGISTER 8-7: DMACS0: DMA CONTROLLER STATUS REGISTER 0 (CONTINUED)

bit 3	XWCOL3: Channel 3 DMA RAM Write Collision Flag bit 1 = Write collision detected 0 = No write collision detected
bit 2	XWCOL2: Channel 2 DMA RAM Write Collision Flag bit
	1 = Write collision detected0 = No write collision detected
bit 1	XWCOL1: Channel 1 DMA RAM Write Collision Flag bit
	1 = Write collision detected0 = No write collision detected
bit 0	XWCOL0: Channel 0 DMA RAM Write Collision Flag bit
	1 = Write collision detected
	0 = No write collision detected

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U-0	U-0	U-0	U-0	R-1	R-1	R-1					
0-0	0-0	0-0	0-0	K-1		R-1 CH<3:0>					
 oit 15	_		_		LOT		bit				
							3一扫上面的二维码图				
R-0	R-0	R-0	R-0	R-0	R-0	R-0	<u></u>				
PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0				
bit 7							bit				
lagandu											
Legend: R = Readable	bit	W = Writable	hit	U = Unimpler	nented hit re	ad as 'O'					
-n = Value at F		'1' = Bit is set		'0' = Bit is cle		x = Bit is unk	nown				
bit 15-12	Unimpleme	nted: Read as '	כ'								
bit 11-8	LSTCH<3:0:	>: Last DMA Ch	annel Active	bits							
	1111 = No DMA transfer has occurred since system Reset										
	1110-1000 = Reserved										
	0111 = Last data transfer was by DMA Channel 7 0110 = Last data transfer was by DMA Channel 6										
	0101 = Last data transfer was by DMA Channel 5										
	0100 = Last data transfer was by DMA Channel 4										
	0011 = Last data transfer was by DMA Channel 3 0010 = Last data transfer was by DMA Channel 2										
	0001 = Last data transfer was by DMA Channel 1										
	0000 = Last data transfer was by DMA Channel 0										
bit 7		PPST7: Channel 7 Ping-Pong Mode Status Flag bit									
		ΓB register selec ΓA register selec									
bit 6	PPST6: Cha	innel 6 Ping-Por	ig Mode Stati	us Flag bit							
		ΓB register seleo ΓA register seleo									
bit 5	PPST5: Channel 5 Ping-Pong Mode Status Flag bit										
		ΓB register seleo ΓA register seleo									
bit 4	PPST4: Channel 4 Ping-Pong Mode Status Flag bit										
	1 = DMA4STB register selected										
L:1 0	0 = DMA4STA register selected										
bit 3	PPST3: Channel 3 Ping-Pong Mode Status Flag bit										
	1 = DMA3STB register selected 0 = DMA3STA register selected										
bit 2	PPST2: Channel 2 Ping-Pong Mode Status Flag bit										
	1 = DMA2STB register selected 0 = DMA2STA register selected										
bit 1		•		ue Elaa hit							
bit 1		Innel 1 Ping-Por	-	uə riay vil							
		TA register selec									
bit 0	PPST0: Cha	innel 0 Ping-Por	ig Mode Stati	us Flag bit							
	1 = DMA0S1	B register selec	ted								

0 = DMA0STA register selected



REGISTER 8-9: DSADR: MOST RECENT DMA RAM ADDRESS

R-0	R-0	R-0	R-0	R-0	R-0	R-0	
			DSAE)R<15:8>			
bit 15							bit-8
							扫一扫上面的二维码
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSA	DR<7:0>			
bit 7							bit 0
Legend:							
R = Readable bi	t	W = Writable	bit	U = Unimpler	nented bit, re	ad as '0'	
-n = Value at PO	D	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown

bit 15-0 DSADR<15:0>: Most Recent DMA RAM Address Accessed by DMA Controller bits

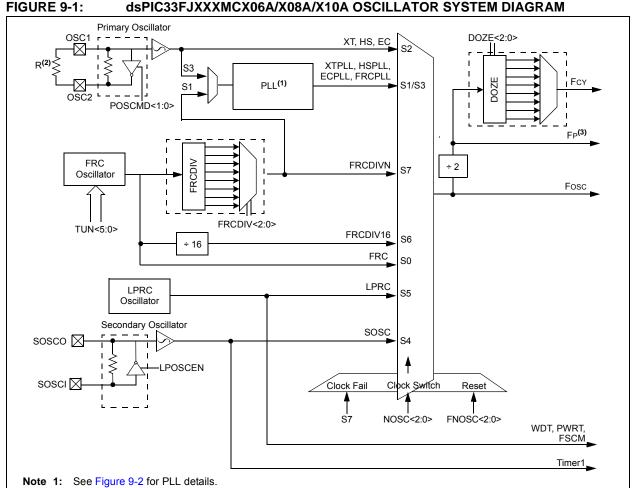


9.0 OSCILLATOR CONFIGURATION

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/ X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 7. "Oscillator" (DS70186) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33FJXXXMCX06A/X08A system provides the following:

- Various external and internal oscilla clock sources
- An on-chip PLL to scale the international frequency to the required system clock frequency
- The internal FRC oscillator can also be used 斯特智楽, 加我为朋友, the PLL, thereby allowing full-speed operation without any external clock generation hardware
- Clock switching between various clock sources
- Programmable clock postscaler for system power savings
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and takes fail-safe measures
- A Clock Control register (OSCCON)
- Nonvolatile Configuration bits for main oscillator selection
- A simplified diagram of the oscillator system is shown in Figure 9-1.



- 2: If the Oscillator is used with XT or HS modes, an extended parallel resistor with the value of 1 M Ω must be connected.
- 3: The term, FP refers to the clock source for all the peripherals, while FcY refers to the clock source for the CPU. Throughout this document FP and FcY are used interchangeably, except in the case of Doze mode. FP and FcY will be different when Doze mode is used in any ratio other than 1:1, which is the default.

9.1 CPU Clocking System

There are seven system clock options provided by the dsPIC33FJXXXMCX06A/X08A/X10A:

- FRC Oscillator
- FRC Oscillator with PLL
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Secondary (LP) Oscillator
- LPRC Oscillator
- · FRC Oscillator with Postscaler

9.1.1 SYSTEM CLOCK SOURCES

The FRC (Fast RC) internal oscillator runs at a nominal frequency of 7.37 MHz. The user software can tune the FRC frequency. User software can optionally specify a factor (ranging from 1:2 to 1:256) by which the FRC clock frequency is divided. This factor is selected using the FRCDIV<2:0> bits (CLKDIV<10:8>).

The primary oscillator can use one of the following as its clock source:

- 1. XT (Crystal): Crystals and ceramic resonators in the range of 3 MHz to 10 MHz. The crystal is connected to the OSC1 and OSC2 pins.
- 2. HS (High-Speed Crystal): Crystals in the range of 10 MHz to 40 MHz. The crystal is connected to the OSC1 and OSC2 pins.
- 3. EC (External Clock): External clock signal is directly applied to the OSC1 pin.

The secondary (LP) oscillator is designed for low power and uses a 32.768 kHz crystal or ceramic resonator. The LP oscillator uses the SOSCI and SOSCO pins.

The LPRC (Low-Power RC) internal oscillator runs at a nominal frequency of 32.768 kHz. It is also used as a reference clock by the Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The clock signals generated by the FRC and primary oscillators can be optionally applied to an on-chip Phase-Locked Loop (PLL) to provide a wide range of output frequencies for device operation. PLL configuration is described in **Section 9.1.3 "PLL Configuration**".

The FRC frequency depends on the FRC accuracy (see Table 26-19) and the value of the FRC Oscillator Tuning register (see Register 9-4).

9.1.2 SYSTEM CLOCK SELECTION

The oscillator source that is used at a device Power-on Reset event is selected using Configuration bit settings. The oscillator Configuration bit settings are located in the Configuration registers in the program memory. (Refer to **Section 23.1 "Configuration Bits**" for further details.) The Initial Oscillator Selection Configuration bits, FNOSC<2:0> (FOSCSEL<2:0>), and the Primary Oscillator Mode Select Configuration bits, POSCMD<1:0> (FOSC<1:0>), select a source that is used at a Power-on Resprimary oscillator is the default (un selection.



The Configuration bits allow users to choose twelve different clock modes, shown in Table 9

The output of the oscillator (or the output of the PLL if a PLL mode has been selected), FOSC, is divided by 2 to generate the device instruction clock (FCY) and the peripheral clock time base (FP). FCY defines the operating speed of the device and speeds up to 40 MHz are supported by the dsPIC33FJXXXMCX06A/X08A/ X10A architecture.

Instruction execution speed or device operating frequency, FCY, is given by the following equation:

EQUATION 9-1: DEVICE OPERATING FREQUENCY

$$FCY = \frac{FOSC}{2}$$

9.1.3 PLL CONFIGURATION

The primary oscillator and internal FRC oscillator can optionally use an on-chip PLL to obtain higher speeds of operation. The PLL provides a significant amount of flexibility in selecting the device operating speed. A block diagram of the PLL is shown in Figure 9-2.

The output of the primary oscillator or FRC, denoted as 'FIN', is divided down by a prescale factor (N1) of 2, 3, ... or 33 before being provided to the PLL's Voltage Controlled Oscillator (VCO). The input to the VCO must be selected to be in the range of 0.8 MHz to 8 MHz. Since the minimum prescale factor is 2, this implies that FIN must be chosen to be in the range of 1.6 MHz to 16 MHz. The prescale factor, 'N1', is selected using the PLLPRE<4:0> bits (CLKDIV<4:0>).

The PLL feedback divisor, selected using the PLLDIV<8:0> bits (PLLFBD<8:0>), provides a factor, 'M', by which the input to the VCO is multiplied. This factor must be selected such that the resulting VCO output frequency is in the range of 100 MHz to 200 MHz.

The VCO output is further divided by a postscale factor, 'N2'. This factor is selected using the PLLPOST<1:0> bits (CLKDIV<7:6>). 'N2' can be either 2, 4 or 8, and must be selected such that the PLL output frequency (Fosc) is in the range of 12.5 MHz to 80 MHz, which generates device operating speeds of 6.25-40 MIPS.

For a primary oscillator or FRC oscillator output, 'FIN', the PLL output, 'FOSC', is given by the following equation:

EQUATION 9-2: Fosc CALCULATION

 $FOSC = FIN \cdot \left(\frac{M}{N1 \cdot N2}\right)$

EQUATION 9-3:

 $FCY = \frac{FOSC}{2} = \frac{1}{2} ($

XT WITH P

EXAMPLE

 $(10000000 \cdot 3)$

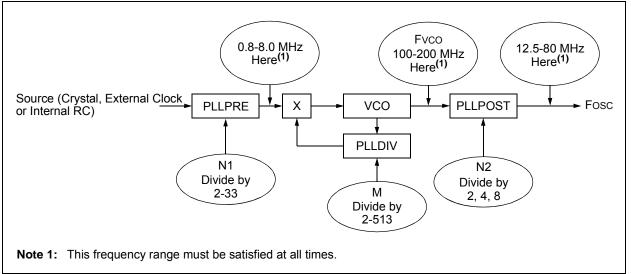
 $2 \cdot 2$

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For example, suppose a 10 MHz crystal is being used with "XT with PLL" as the selected oscillator mode. If PLLPRE<4:0> = 0, then N1 = 2. This yields a VCO input of 10/2 = 5 MHz, which is within the acceptable range of 0.8-8 MHz. If PLLDIV<8:0> = 0x1E, then M = 32. This yields a VCO output of 5 * 32 = 160 MHz, which is within the 100-200 MHz ranged needed.

If PLLPOST<1:0> = 0, then N2 = 2. This provides a Fosc of 160/2 = 80 MHz. The resultant device operating speed is 80/2 = 40 MIPS.





Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	See Note
Fast RC Oscillator with Divide-by-N (FRCDIVN)	Internal	xx	111	1, 2
Fast RC Oscillator with Divide-by-16 (FRCDIV16)	Internal	xx	110	1
Low-Power RC Oscillator (LPRC)	Internal	XX	101	1
Secondary (Timer1) Oscillator (Sosc)	Secondary	xx	100	1
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011	_
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011	_
Primary Oscillator (EC) with PLL (ECPLL)	Primary	00	011	1
Primary Oscillator (HS)	Primary	10	010	_
Primary Oscillator (XT)	Primary	01	010	—
Primary Oscillator (EC)	Primary	00	010	1
Fast RC Oscillator with PLL (FRCPLL)	Internal	XX	001	1
Fast RC Oscillator (FRC)	Internal	xx	000	1

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.



REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER^(1,3)

	Image: Figure 3-1: OSCCON: OSCILLATOR CONTROL REGISTER ^(1,3)									
U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	. F¢∕∀∖4-y			
_		COSC<2:0>		—		NOSC<2:0> ⁽²⁾				
bit 15							- bi : .8			
R/W-0	U-0	R-0	U-0	R/C-0	U-0	R/W-0	—————————————————————————————————————			
CLKLOCK	—	LOCK	—	CF	—	LPOSCEN	OSWEN			
bit 7	•	· ·				÷	bit 0			
Legend:		y = Value set fr	om Configu	ration bits on P	OR					
R = Readable	bit	W = Writable b	it	U = Unimpler	mented bit, re	ad as '0'				
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown			
bit 15	Unimpleme	nted: Read as '0'								
bit 14-12	COSC<2:0>	: Current Oscillat	or Selection	bits (read-only	')					
	101 = Low-F 100 = Secor 011 = Prima 010 = Prima 001 = Fast F	RC oscillator (FRC Power RC oscillator ndary oscillator (S ury oscillator (XT, I ury oscillator (XT, I RC Oscillator (FR RC oscillator (FRC	or (LPRC) losc) HS, EC) wit HS, EC) C) with Divi	h PLL	L (FRCDIVN	+ PLL)				
bit 11	Unimplemented: Read as '0'									
bit 10-8	NOSC<2:0>	: New Oscillator	Selection bit	ts ⁽²⁾						
	110 = Fast F 101 = Low-F 100 = Secor 011 = Prima 010 = Prima 001 = Fast F	RC oscillator (FRC RC oscillator (FRC Power RC oscillator ndary oscillator (S Iny oscillator (XT, I Iny oscillator (XT, I RC Oscillator (FR RC oscillator (FRC	C) with Divid or (LPRC) osc) HS, EC) wit HS, EC) C) with Divid	de-by-16 h PLL	LL (FRCDIVN	+ PLL)				
bit 7		Clock Lock Enab								
	PLL cor	SM0 = 1), then clo nfigurations may b nd PLL selections	e modified.	-			nen clock and			
bit 6		nted: Read as '0'								
bit 5	-	Lock Status bit (re								
	1 = Indicate	s that PLL is in lo	ck or PLL s			LL is disabled				
bit 4		nted: Read as '0'			č					
bit 3	CF: Clock Fa	ail Detect bit (read	d/clear by a	nnlication)						
	1 = FSCM h			pplication)						

2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL modes are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.

3: This register is reset only on a Power-on Reset (POR).

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER^(1,3) (CONTINUED)

- bit 2 Unimplemented: Read as '0'
- bit 1 LPOSCEN: Secondary (LP) Oscillator Enable bit
 - 1 = Enable secondary oscillator
 - 0 = Disable secondary oscillator
- bit 0 OSWEN: Oscillator Switch Enable bit
 - 1 = Request oscillator switch to selection specified by NOSC<2:0> bits
 - 0 = Oscillator switch is complete
- Note 1: Writes to this register require an unlock sequence. Refer to Section 7. "Oscillator" (DS70186) in the "dsPIC33F/PIC24H Family Reference Manual" for details.
 - 2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL modes are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.
 - 3: This register is reset only on a Power-on Reset (POR).



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REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER⁽²⁾

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	•
ROI		DOZE<2:0>		DOZEN ⁽¹⁾		FRCDIV<2:0>	
it 15							
	D 444 4		D 444 A	D 444 A	54440	5444.0	
R/W-0	R/W-1	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	OST<1:0>	—			PLLPRE<4:	0>	
pit 7							bit 0
egend:		v = Value set f	rom Configu	ration bits on P	OR		
R = Readable	e bit	W = Writable b	-	U = Unimplen		ad as '0'	
n = Value at		'1' = Bit is set		'0' = Bit is clea		x = Bit is unkr	nown
oit 15	ROI: Recove	er on Interrupt bit					
	1 = Interrup	ts will clear the D	OZEN bit a	nd the processo	r clock/peripł	neral clock ratio is	s set to 1:1
	•	ts have no effect					
oit 14-12		Processor Cloc	k Reduction	Select bits			
	000 = FCY/1						
	001 = FCY/2 010 = FCY/4						
	010 = FCY/4 011 = FCY/8						
	100 = Fcy/1	· · ·					
	101 = Fcy/3						
	110 = Fcy/6						
	111 = Fcy/1	-	(4)				
bit 11		ZE Mode Enable					
					pheral clocks	s and the process	sor clocks
		or clock/periphe					
bit 10-8)>: Internal Fast		or Postscaler bits	6		
	000 = FRC 0 001 = FRC 0	divide by 1 (defau	lit)				
	010 = FRC (
	011 = FRC 0						
	100 = FRC d						
	101 = FRC (
	110 = FRC (
sit 7 6		divide by 256	Nutrout Divide	or Soloot bito (al	na danatad a	o (N2) DLL posto	oplor)
bit 7-6					so denoted a	s 'N2', PLL posts	caler)
	00 = Output/ 01 = Output/						
	10 = Reserv						
	11 = Output/						
oit 5	-	nted: Read as '0	,				
oit 4-0	-			ut Divider bits (a	lso denoted a	as 'N1', PLL pres	caler)
-		ut/2 (default)				,F.co.	- /
	00001 = Inp						
	•						
	•						
	•						
	• • 11111 = Inp						

Note 1: This bit is cleared when the ROI bit is set and an interrupt occurs.

2: This register is reset only on a Power-on Reset (POR).

REGISTER	9-3: PLLF	BD: PLL FEE		ISOR REGIS	TER ⁽¹⁾		~
U-0	U-0	U-0	U-0	U-0	U-0	U-0	RØ40
_	—		_	—			PILLUIV<8>
bit 15							bit
	DAVA			DAMA	DAMA		一扫上面的二维码图案
R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
			PLLU	0IV<7:0>			
bit 7							bit (
Legend:							
R = Readab		W = Writable b		•	nented bit, read		
-n = Value a	It POR	'1' = Bit is set		0' = Bit is cleared x = Bit is			nown
bit 15-9 bit 8-0	-	= 3		s (also denoted	as 'M', PLL mu	ıltiplier)	
	•						
	•						
	•						
	000110000	= 50 (default)					
	•						
	•						
	•						
	111111111	= 513					

Note 1: This register is reset only on a Power-on Reset (POR).



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OSCTUN: FRC OSCILLATOR TUNING REGISTER⁽²⁾ **REGISTER 9-4:** U-0 U-0 U-0 U-0 U-0 U-0 U-0 ____ _ ____ ___ ____ ____ ____ bit 15 U-0 U-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 TUN<5:0>(1) ____ bit 7 bit 0 Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15-6 Unimplemented: Read as '0' TUN<5:0>: FRC Oscillator Tuning bits⁽¹⁾ bit 5-0 011111 = Center frequency + 11.625% (8.23 MHz) 011110 = Center frequency + 11.25% (8.20 MHz) 000001 = Center frequency + 0.375% (7.40 MHz) 000000 = Center frequency (7.37 MHz nominal) 111111 = Center frequency – 0.375% (7.345 MHz) 100001 = Center frequency - 11.625% (6.52 MHz) 100000 = Center frequency - 12% (6.49 MHz)

- **Note 1:** OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation and is neither characterized nor tested.
 - 2: This register is reset only on a Power-on Reset (POR).

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Applications are free to switch between any of the four clock sources (Primary, LP, FRC and LPRC) under software control at any time. To limit the possible side effects that could result from this flexibility, dsPIC33FJXXXMCX06A/X08A/X10A devices have a safeguard lock built into the switch process.

Note: Primary Oscillator mode has three different submodes (XT, HS and EC) which are determined by the POSCMD<1:0> Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device.

9.2.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSM1 Configuration bit in the Configuration register must be programmed to '0'. (Refer to **Section 23.1 "Configuration Bits"** for further details.) If the FCKSM1 Configuration bit is unprogrammed ('1'), the clock switching function and Fail-Safe Clock Monitor function are disabled. This is the default setting.

The NOSC control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSC bits (OSCCON<14:12>) reflect the clock source selected by the FNOSC Configuration bits.

The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled; it is held at '0' at all times.

9.2.2 OSCILLATOR SWITCHING SEQUENCE

At a minimum, performing a clock switch requires the following basic sequence:

- 1. If desired, read the COSC bits (OSCCON<14:12>) to determine the current oscillator source.
- 2. Perform the unlock sequence to allow a write to the OSCCON register high byte.
- Write the appropriate value to the NOSC control bits (OSCCON<10:8>) for the new oscillator source.
- 4. Perform the unlock sequence to allow a write to the OSCCON register low byte.
- 5. Set the OSWEN bit to initiate the oscillator switch.

Once the basic sequence is completed, the system clock hardware responds automatically as follows:

1. The clock switching hardware compares the COSC status bits with the new value of the NOSC control bits. If they are the same, then the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.

 If a valid clock switch has be LOCK (OSCCON<5>) and (OSCCON<3>) status bits are closed



- The new oscillator is turned on b tit is not currently running. If a must be turned on, the hardware waits until the Oscillator Start-up Timer (OST) expires的ff#the業, 加我为朋友, new source is using the PLL, the hardware waits until a PLL lock is detected (LOCK = 1).
- 4. The hardware waits for 10 clock cycles from the new clock source and then performs the clock switch.
- The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSC bit values are transferred to the COSC status bits.
- 6. The old clock source is turned off at this time, with the exception of LPRC (if WDT or FSCM is enabled) or LP (if LPOSCEN remains set).
 - Note 1: The processor continues to execute code throughout the clock switching sequence. Timing-sensitive code should not be executed during this time.
 - 2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.
 - 3: Refer to Section 7. "Oscillator" (DS70186) in the "dsPIC33F/PIC24H Family Reference Manual" for details.

9.3 Fail-Safe Clock Monitor (FSCM)

The Fail-Safe Clock Monitor (FSCM) allows the device to continue to operate even in the event of an oscillator failure. The FSCM function is enabled by programming. If the FSCM function is enabled, the LPRC internal oscillator runs at all times (except during Sleep mode) and is not subject to control by the Watchdog Timer.

In the event of an oscillator failure, the FSCM generates a clock failure trap event and switches the system clock over to the FRC oscillator. Then, the application program can either attempt to restart the oscillator or execute a controlled shutdown. The trap can be treated as a warm Reset by simply loading the Reset address into the oscillator fail trap vector.

If the PLL multiplier is used to scale the system clock, the internal FRC is also multiplied by the same factor on clock failure. Essentially, the device switches to FRC with PLL on a clock failure.

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NOTES:



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10.0 POWER-SAVING FEATURES

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/ X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 9. "Watchdog Timer and Power-Saving Modes" (DS70196) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33FJXXXMCX06A/X08A/X10A devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of circuits being clocked constitutes lower consumed power. dsPIC33FJXXXMCX06A/X08A/X10A devices can manage power consumption in four different ways:

- · Clock frequency
- Instruction-based Sleep and Idle modes
- · Software-controlled Doze mode
- · Selective peripheral control in software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

10.1 Clock Frequency and Clock Switching

dsPIC33FJXXXMCX06A/X08A/X10A devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSC bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in Section 9.0 "Oscillator Configuration".

10.2 Instruction-Based Po Modes



dsPIC33FJXXXMCX06A/X08A/X10A two special power-saving modes through the execution of a special PW

Sleep mode stops clock operation and halts all code maximum execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembly syntax of the PWRSAV instruction is shown in Example 10-1.

Note: SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

10.2.1 SLEEP MODE

Sleep mode has the following features:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate during Sleep mode since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals may continue to operate in Sleep mode. This includes items such as the input change notification on the I/O ports and peripherals that use an external clock input. Any peripheral that requires the system clock source for its operation is disabled in Sleep mode.

The device will wake-up from Sleep mode on any of the following events:

- · Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

On wake-up from Sleep, the processor restarts with the same clock source that was active when Sleep mode was entered.

EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX

PWRSAV#SLEEP_MODE; Put the device into SLEEP modePWRSAV#IDLE_MODE; Put the device into IDLE mode

10.2.2 IDLE MODE

Idle mode has the following features:

- The CPU stops executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see Section 10.4 "Peripheral Module Disable").
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device will wake from Idle mode on any of the following events:

- Any interrupt that is individually enabled
- Any device Reset
- · A WDT time-out

On wake-up from Idle, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the PWRSAV instruction or the first instruction in the ISR.

10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a PWRSAV instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

10.3 Doze Mode

Generally, changing clock speed and invoking one of the power-saving modes are the preferred strategies for reducing power consumption. There may be circumstances, however, where this is not practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed may introduce communication errors, while using a power-saving mode may stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.



Doze mode is enabled by setting the (CLKDIV<11>). The ratio between peripher clock speed is determined by the DO (CLKDIV<14:12>). There are eig configurations, from 1:1 to 1:128, with default setting.

It is also possible to use Doze mode to actively and the mathematic reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU idles, waiting for something to invoke an interrupt routine. Enabling the automatic return to full-speed CPU operation on interrupts is enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the CAN module has been configured for 500 kbps based on this device operating speed. If the device is now placed in Doze mode with a clock frequency ratio of 1:4, the CAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

10.4 Peripheral Module Disable

The Peripheral Module Disable registers (PMD) provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled via the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers will have no effect and read values will be invalid.

A peripheral module is only enabled if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC[®] DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note: If a PMD bit is set, the corresponding module is disabled after a delay of 1 instruction cycle. Similarly, if a PMD bit is cleared, the corresponding module is enabled after a delay of 1 instruction cycle (assuming the module control registers are already configured to enable module operation).



	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD	PWMMD	
pit 15						Ľ	bit
		54446		54446	-	D 444 a	日一扫上面的二维码图
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	C2MD	C1MD	AD1MD ⁽¹⁾
oit 7							bit
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown
bit 15	T5MD: Time	r5 Module Disal	ole bit				
		nodule is disable					
	0 = Timer5 n	nodule is enable	ed				
bit 14	T4MD: Time	r4 Module Disal	ole bit				
		nodule is disable nodule is enable					
bit 13		r3 Module Disal					
л 10		nodule is disable					
		nodule is enable					
bit 12	T2MD: Time	r2 Module Disal	ole bit				
	-	nodule is disable nodule is enable					
bit 11		r1 Module Disal					
	-	nodule is disable					
	0 = Timer1 n	nodule is enable	ed				
bit 10	QEI1MD: QE	EI1 Module Disa	ble bit				
		dule is disablec dule is enabled					
bit 9	PWMMD: PV	VM Module Dis	able bit				
	1 = PWM mo	dule is disabled	ł				
		dule is enabled					
bit 8	-	nted: Read as '					
bit 7		1 Module Disal					
		dule is disabled dule is enabled					
bit 6		T2 Module Disa	hle hit				
	1 = UART2 r	nodule is disabl	ed				
nit 5		nodule is enable					
bit 5		T1 Module Disa nodule is disabl					
	-	nodule is enable					
bit 4	SPI2MD: SP	12 Module Disa	ble bit				
511 4		E modulo Biod					

Note 1: The PCFGx bits have no effect if the ADC module is disabled by setting this bit. In this case, all port pins multiplexed with ANx will be in Digital mode.



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REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CO

- bit 3 SPI1MD: SPI1 Module Disable bit 1 = SPI1 module is disabled 0 = SPI1 module is enabled bit 2 C2MD: ECAN2 Module Disable bit 1 = ECAN2 module is disabled 0 = ECAN2 module is enabled bit 1 C1MD: ECAN1 Module Disable bit 1 = ECAN1 module is disabled 0 = ECAN1 module is enabled AD1MD: ADC1 Module Disable bit(1) bit 0 1 = ADC1 module is disabled 0 = ADC1 module is enabled
- **Note 1:** The PCFGx bits have no effect if the ADC module is disabled by setting this bit. In this case, all port pins multiplexed with ANx will be in Digital mode.



REGISTER 10-2:	PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD
bit 15						

R/W-0	i一扫上面的二维码图案,) R/W-0	加我为月						
OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	
bit 7			•	•		•	bit 0	

Legend:				
R = Readable		W = Writable bit	U = Unimplemented bit	
n = Value at P	OR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknowr
pit 15	IC8MD: Ir	nput Capture 8 Module Disabl	le bit	
		Capture 8 module is disabled Capture 8 module is enabled	l	
	1 = Input	nput Capture 7 Module Disabl Capture 7 module is disabled Capture 7 module is enabled		
	1 = Input	nput Capture 6 Module Disabl Capture 6 module is disabled Capture 6 module is enabled		
oit 12	IC5MD: Ir 1 = Input	nput Capture 5 Module Disabl Capture 5 module is disabled Capture 5 module is enabled		
oit 11	IC4MD: Ir 1 = Input	nput Capture 4 Module Disabl Capture 4 module is disabled Capture 4 module is enabled		
	1 = Input	nput Capture 3 Module Disabl Capture 3 module is disabled Capture 3 module is enabled		
oit 9	IC2MD: Ir 1 = Input	nput Capture 2 Module Disabl Capture 2 module is disabled Capture 2 module is enabled		
oit 8	IC1MD: Ir 1 = Input	nput Capture 1 Module Disabl Capture 1 module is disabled Capture 1 module is enabled	l	
oit 7	OC8MD: 1 = Outpu	Output Compare 8 Module Di It Compare 8 module is disab It Compare 8 module is enabl	isable bit led	
pit 6	0C7MD: 1 = Outpu	Output Compare 4 Module Di It Compare 7 module is disab It Compare 7 module is enabl	isable bit led	
oit 5	OC6MD: 1 = Outpu	Output Compare 6 Module Di It Compare 6 module is disab It Compare 6 module is enabl	isable bit led	
oit 4	OC5MD: 1 = Outpu	Output Compare 5 Module Di at Compare 5 module is disab at Compare 5 module is enabl	isable bit led	



REGISTER 10-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2 (CO

bit 3	OC4MD: Output Compare 4 Module Disable bit 1 = Output Compare 4 module is disabled 0 = Output Compare 4 module is enabled
bit 2	OC3MD: Output Compare 3 Module Disable bit 1 = Output Compare 3 module is disabled
	0 = Output Compare 3 module is enabled
bit 1	OC2MD: Output Compare 2 Module Disable bit
	 1 = Output Compare 2 module is disabled 0 = Output Compare 2 module is enabled
bit 0	OC1MD: Output Compare 1 Module Disable bit
	1 = Output Compare 1 module is disabled0 = Output Compare 1 module is enabled





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R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	0-0
T9MD	T8MD	T7MD	T6MD	_	—		
oit 15		•					bit 8
U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	目一扫上面的开线的图案,
_	_	—		_	_	I2C2MD	AD2MD ⁽¹⁾
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	oit	U = Unimplem	ented bit, rea	ad as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unk	nown
bit 15 bit 14 bit 13 bit 12	1 = Timer9 m 0 = Timer9 m T8MD: Timer8 m 0 = Timer8 m T7MD: Timer 1 = Timer7 m 0 = Timer7 m T6MD: Timer 1 = Timer6 m	9 Module Disab odule is disable odule is enable 8 Module Disab odule is disable odule is enable 7 Module Disab odule is enable 6 Module Disab odule is disable odule is disable	ed d ele bit ed ele bit ed ele bit ed				
bit 11-2		ted: Read as '0					
bit 1 bit 0	1 = I2C2 mod 0 = I2C2 mod	2 Module Disab ule is disabled ule is enabled Module Disable					
	1 = AD2 mod 0 = AD2 mod	ule is disabled ule is enabled					

Note 1: The PCFGx bits have no effect if the ADC module is disabled by setting this bit. In this case, all port pins multiplexed with ANx will be in Digital mode.

NOTES:



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11.0 I/O PORTS

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/ X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 10. "I/O Ports" (DS70193) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

All of the device pins (except VDD, VSS, MCLR and OSC1/CLKIN) are shared between the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

11.1 Parallel I/O (PIO) Ports

A parallel I/O port that shares a pin with a peripheral is, in general, subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the

output data and control signals of the also prevents "loop through", in whi output can drive the input of a periphesame pin. Figure 11-1 shows how por other peripherals and the associated they are connected.



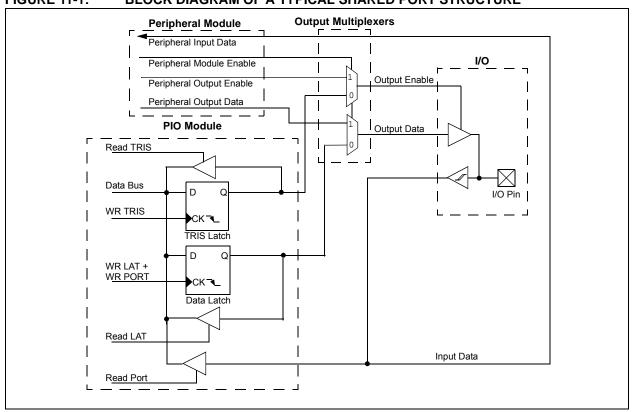
When a peripheral is enabled and actively indivingenan mathematical associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin may be read, but the output driver for the parallel port bit will be disabled. If a peripheral is enabled but the peripheral is not actively driving a pin, that pin may be driven by a port.

All port pins have three registers directly associated with their operation as digital I/O. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx), read the latch. Writes to the latch, write the latch. Reads from the port (PORTx), read the port pins, while writes to the port pins, write the latch.

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers, and the port pins will read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs. An example is the INT4 pin.







11.2 Open-Drain Configuration

In addition to the PORT, LAT and TRIS registers for data control, some port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (e.g., 5V) on any desired 5V tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

See the "**Pin Diagrams**" section for the available pins and their functionality.

11.3 Configuring Analog Port Pins

The ADxPCFGH, ADxPCFGL and TRIS registers control the operation of the ADC port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bit set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) is converted.

Clearing any bit in the ADxPCFGH or ADxPCFGL register configures the corresponding bit to be an analog pin. This is also the Reset state of any I/O pin that has an analog (ANx) function associated with it.

Note: In devices with two ADC modules, if the corresponding PCFG bit in either AD1PCFGH(L) and AD2PCFGH(L) is cleared, the pin is configured as an analog input.

When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level).

Pins configured as digital inputs will not convert an analog input. Analog levels on any pin that is defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

Note:	The voltage on an analog input pin can be
	between -0.3V to (VDD + 0.3 V).

11.4 I/O Port Write/Read Timi

One instruction cycle is required bet direction change or port write operation operation of the same port. Typically, the would be a NOP.

11.5 Input Change Notification

The input change notification function of the I/O ports allows the dsPIC33FJXXXMCX06A/X08A/X10A devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature is capable of detecting input change-of-states even in Sleep mode, when the clocks are disabled. Depending on the device pin count, there are up to 24 external signals (CN0 through CN23) that can be selected (enabled) for generating an interrupt request on a change-of-state.

There are four control registers associated with the CN module. The CNEN1 and CNEN2 registers contain the CN Interrupt Enable (CNxIE) control bits for each of the CN input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each CN pin also has a weak pull-up connected to it. The pull-ups act as a current source that is connected to the pin and eliminate the need for external resistors when push button or keypad devices are connected. The pull-ups are enabled separately using the CNPU1 and CNPU2 registers, which contain the Weak Pull-up Enable bits (CNxPUE) for each of the CN pins. Setting any of the control bits enables the weak pull-ups for the corresponding pins.

Note: Pull-ups on change notification pins should always be disabled whenever the port pin is configured as a digital output.

EXAMPLE 11-1: PORT WRITE/READ EXAMPLE

MOV0xFF00, W0; Configure PORTB<15:8> as inputsMOVW0, TRISBB; and PORTB<7:0> as outputsNOP; Delay 1 cyclebtssPORTB, #13; Next Instruction

11.6 I/O Helpful Tips

- 1. In some cases, certain pins as defined in TABLE 26-9: "DC Characteristics: I/O Pin Input Specifications" under "Injection Current", have internal protection diodes to VDD and VSS. The term "Injection Current" is also referred to as "Clamp Current". On designated pins, with sufficient external current limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings with nominal VDD with respect to the VSS and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes, that the resulting current being injected into the device that is clamped internally by the VDD and VSS power rails, may affect the ADC accuracy by four to six counts.
- I/O pins that are shared with any analog input pin. 2 (i.e., ANx), are always analog pins by default after any reset. Consequently, any pin(s) configured as an analog input pin, automatically disables the digital input pin buffer. As such, any attempt to read a digital input pin will always return a '0' regardless of the digital logic level on the pin if the analog pin is configured. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the analog pin configuration registers in the ADC module, (i.e., ADxPCFGL, AD1PCFGH), by setting the appropriate bit that corresponds to that I/O port pin to a '1'. On devices with more than one ADC, both analog pin configurations for both ADC modules must be configured as a digital I/O pin for that pin to function as a digital I/O pin.
- **Note:** Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.
- 3. Most I/O pins have multiple functions. Referring to the device pin diagrams in the data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name from left-to-right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1. This indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.

Each CN pin has a configurable pull-up resistor. The pull-ups a source connected to the pin, and need for external resistors in tions. The internal pull-up is to VDD. This is still above the minimum CMOS and TTL devices.



5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the VOH/IOH and VOL/IOL DC characteristic specification. The respective IOH and IOL current rating only applies to maintaining the corresponding output at or above the VOH and at or below the VOL levels. However, for LEDs unlike digital inputs of an externally connected device, they are not governed by the same minimum VIH/VIL levels. An I/O pin output can safely sink or source any current less than that listed in the absolute maximum rating section of the data sheet. For example:

VOH = 2.4v @ IOH = -8 mA and VDD = 3.3V

The maximum output current sourced by any 8 mA I/O pin = 12 mA.

LED source current < 12 mA is technically permitted. Refer to the VOH/IOH graphs in Section 26.0 "Electrical Characteristics" for additional information.

11.7 I/O Resources

Many useful resources related to I/O are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en546066

11.7.1 KEY RESOURCES

- Section 10. "I/O Ports" (DS70193)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

NOTES:



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12.0 **TIMER1**

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/ X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 11. "Timers"** (DS70205) in the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer, which can serve as the time counter for the Real-Time Clock (RTC) or operate as a free-running interval timer/counter. Timer1 can operate in three modes:

- 16-Bit Timer
- 16-Bit Synchronous Counter
- 16-Bit Asynchronous Counter

Timer1 also supports the following fe

- Timer gate operation
- · Selectable prescaler settings
- Timer operation during CPU Idle modes
- Interrupt on 16-bit Period register match of fallingax, 加我为朋友, edge of external gate signal

Figure 12-1 presents a block diagram of the 16-bit timer module.

To configure Timer1 for operation, do the following:

- 1. Set the TON bit (= 1) in the T1CON register.
- 2. Select the timer prescaler ratio using the TCKPS<1:0> bits in the T1CON register.
- 3. Set the Clock and Gating modes using the TCS and TGATE bits in the T1CON register.
- 4. Set or clear the TSYNC bit in T1CON to select synchronous or asynchronous operation.
- 5. Load the timer period value into the PR1 register.
- 6. If interrupts are required, set the interrupt enable bit, T1IE. Use the priority bits, T1IP<2:0>, to set the interrupt priority.

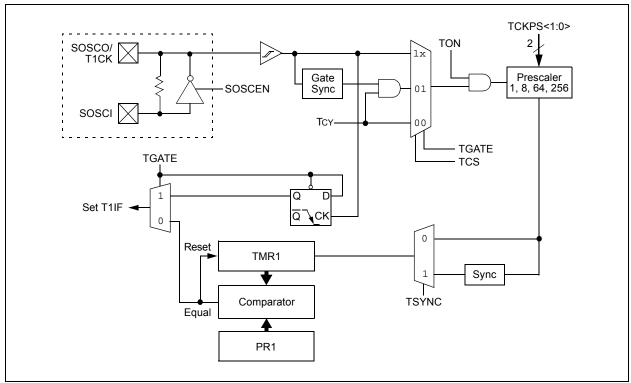


FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM



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REGISTER 12-1:	T1CON: TIMER1 CONTROL REGISTER	
----------------	--------------------------------	--

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0
TON	—	TSIDL	—	_	—	—
bit 15						

							扫一扫上面的二维码	马图案,
U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0	
	TGATE	TCKPS	S<1:0>	—	TSYNC	TCS	—	
bit 7							bit 0	

Legend:				
R = Readal	ole bit	W = Writable bit	U = Unimplemented bit,	, read as '0'
-n = Value a	at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 15	1 = Starts	ner1 On bit s 16-bit Timer1 s 16-bit Timer1		
bit 14	Unimple	mented: Read as '0'		
bit 13	TSIDL: S	Stop in Idle Mode bit		
		ontinue module operation wh inue module operation in Idle		
bit 12-7	Unimple	mented: Read as '0'		
bit 6	When T1 This bit is When T1 1 = Gate	s ignored.	1	
bit 5-4	TCKPS<	1:0>: Timer1 Input Clock Pre	escale Select bits	
	11 = 1:28 10 = 1:64 01 = 1:8 00 = 1:1			
bit 3	Unimple	mented: Read as '0'		
bit 2	<u>When TC</u> 1 = Sync 0 = Do no <u>When TC</u>	hronize external clock input ot synchronize external clock		
bit 1	TCS: Tim 1 = Exter	ner1 Clock Source Select bit rnal clock from T1CK pin (on nal clock (Fcy)		
bit 0	Unimple			

13.0 TIMER2/3, TIMER4/5, TIMER6/7 AND TIMER8/9

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/ X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 11. "Timers" (DS70205) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Timer2/3, Timer4/5, Timer6/7 and Timer8/9 modules are 32-bit timers that can also be configured as four independent 16-bit timers with selectable operating modes.

As a 32-bit timer, Timer2/3, Timer4/5, Timer6/7 and Timer8/9 operate in three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support the following features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- · Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules (Timer2 and Timer3 only)
- ADC1 Event Trigger (Timer2/3 only)
- ADC2 Event Trigger (Timer4/5 only)

Individually, all eight of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed above, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON, T5CON, T6CON, T7CON, T8CON and T9CON registers. T2CON, T4CON, T6CON and T8CON are shown in generic form in Register 13-1. T3CON, T5CON, T7CON and T9CON are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2, Timer4, Timer6 or Timer8 is the least significant word; Timer3, Timer5, Timer7 or Timer9 is the most significant word of the 32-bit timers.



Note: For 32-bit operation, Torow for and T9CON and T9CON and T9CON ignored. Only T2CON, and T8CON control bits and control. Timer2, Timer4, Timer6 and Timer8 clock and gate inputs are dilized for the 32-bit timer modules, but an interrupt is generated with the Timer3, Timer5, Ttimer7 and Timer9 interrupt flags.

To configure Timer2/3, Timer4/5, Timer6/7 or Timer8/9 for 32-bit operation, do the following:

- 1. Set the corresponding T32 control bit.
- 2. Select the prescaler ratio for Timer2, Timer4, Timer6 or Timer8 using the TCKPS<1:0> bits.
- 3. Set the Clock and Gating modes using the corresponding TCS and TGATE bits.
- Load the timer period value. PR3, PR5, PR7 or PR9 contains the most significant word of the value, while PR2, PR4, PR6 or PR8 contains the least significant word.
- If interrupts are required, set the interrupt enable bit, T3IE, T5IE, T7IE or T9IE. Use the priority bits, T3IP<2:0>, T5IP<2:0>, T7IP<2:0> or T9IP<2:0>, to set the interrupt priority. While Timer2, Timer4, Timer6 or Timer8 control the timer, the interrupt appears as a Timer3, Timer5, Timer7 or Timer9 interrupt.
- 6. Set the corresponding TON bit.

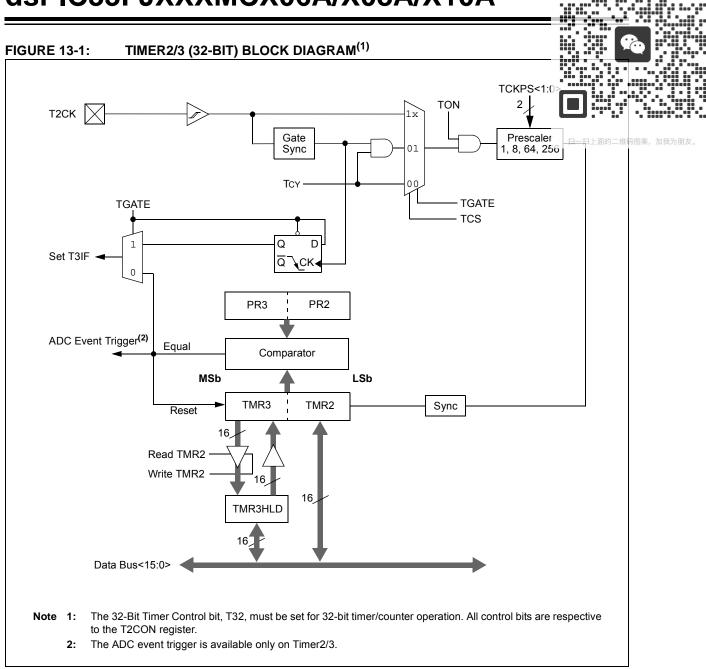
The timer value at any point is stored in the register pair, TMR3:TMR2, TMR5:TMR4, TMR7:TMR6 or TMR9:TMR8. TMR3, TMR5, TMR7 or TMR9 always contain the most significant word of the count, while TMR2, TMR4, TMR6 or TMR8 contain the least significant word.

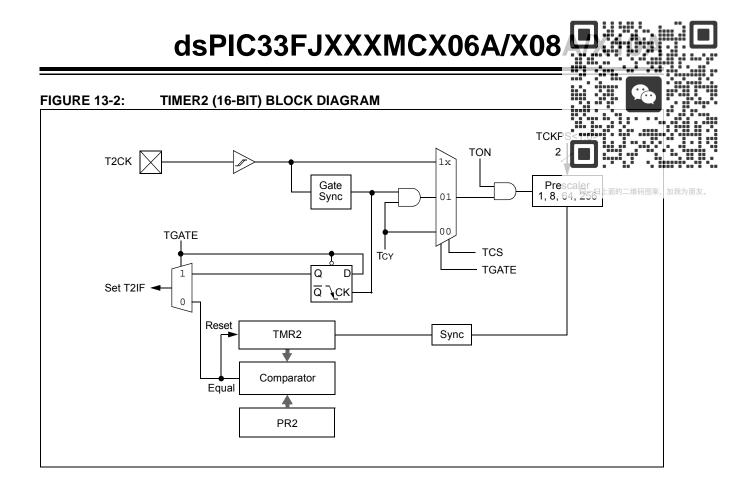
To configure any of the timers for individual 16-bit operation, do the following:

- 1. Clear the T32 bit corresponding to that timer.
- 2. Select the timer prescaler ratio using the TCKPS<1:0> bits.
- 3. Set the Clock and Gating modes using the TCS and TGATE bits.
- 4. Load the timer period value into the PRx register.
- 5. If interrupts are required, set the interrupt enable bit, TxIE. Use the priority bits, TxIP<2:0>, to set the interrupt priority.
- 6. Set the TON bit.

A block diagram for a 32-bit timer pair (Timer4/5) example is shown in Figure 13-1, and a timer (Timer4) operating in 16-bit mode example is shown in Figure 13-2.

Note: Only Timer2 and Timer3 can trigger a DMA data transfer.







REGISTER 13-1: TxCON (T2CON, T4CON, T6CON OR T8CON) CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0
TON	—	TSIDL	—	—	—	—
bit 15						

							扫一扫上面的二维码	马图案,
U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	
_	TGATE	TCKP	S<1:0>	T32	—	TCS ⁽¹⁾	_	
bit 7							bit 0	

Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value a	t POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			
bit 15	<u>When T3</u> 1 = Start 0 = Stop <u>When T3</u> 1 = Start	s 32-bit Timerx/y s 32-bit Timerx/y					
bit 14	Unimple	emented: Read as '0'					
bit 13		Stop in Idle Mode bit					
		ontinue module operation whether the second structure module operation in Identity of the second structure whether the second struct					
bit 12-7	Unimple	emented: Read as '0'					
bit 6	When TO This bit i When TO 1 = Gate	s ignored.	d				
bit 5-4	TCKPS 11 = 1:2 10 = 1:6 01 = 1:8 00 = 1:1	4	escale Select bits				
bit 3	1 = Time	Bit Timer Mode Select bit erx and Timery form a single erx and Timery act as two 16					
bit 2		emented: Read as '0'					
bit 1	1 = Exte	nerx Clock Source Select bit rnal clock from TxCK pin (or nal clock (FcY)					
bit 0	Unimple	mented: Read as '0'					

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REGISTER 13-2: TyCON (T3CON, T5CON, T7CON OR T9CON) CONTROL REGIST

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	
TON ⁽¹⁾	—	TSIDL ⁽²⁾	—	—	—	—	
bit 15							

-						3	日一日上面的二维码图案,	」加技
U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	
_	TGATE ⁽¹⁾	TCKPS	<1:0>(1)	—	—	TCS ^(1,3)	—	
bit 7							bit 0	

Legend:				
R = Read	able bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value	e at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 15		nery On bit ⁽¹⁾		
		s 16-bit Timery s 16-bit Timery		
bit 14	Unimple	mented: Read as '0'		
bit 13	TSIDL: S	otop in Idle Mode bit ⁽²⁾		
		ontinue module operation wh inue module operation in Idle		
bit 12-7	Unimple	mented: Read as '0'		
bit 6	TGATE:	Timery Gated Time Accumul	lation Enable bit ⁽¹⁾	
	When TO This bit is	<u>CS = 1:</u> s ignored.		
	$\frac{\text{When TC}}{1 = \text{Gate}}$	<u>CS = 0:</u> d time accumulation enablec	1	
		d time accumulation disable		
bit 5-4	TCKPS<	1:0>: Timer3 Input Clock Pre	escale Select bits ⁽¹⁾	
	11 = 1:2	56		
	10 = 1:64	1		
	01 = 1:8 00 = 1:1			
bit 3-2	Unimple	mented: Read as '0'		
bit 1	TCS: Tin	nery Clock Source Select bit	(1,3)	
		nal clock from TyCK pin (on nal clock (Fcy)	the rising edge)	
bit 0	Unimple	mented: Read as '0'		
Note 1:		peration is enabled (T2CON- set through T2CON.	<3> = 1), these bits have no ef	ffect on Timery operation; all time

- 2: When 32-bit timer operation is enabled (T32 = 1) in the Timer Control register (TxCON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.
- 3: The TyCK pin is not available on all timers. Refer to the "Pin Diagrams" section for the available pins.

NOTES:



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14.0 INPUT CAPTURE

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/ X08A/X10A family of devices. However, it is not intended to be a comprereference hensive source To complement the information in this data sheet, refer to Section 12. "Input Capture" (DS70198) in the "dsPIC33F/ PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The input capture module is useful in applications requiring frequency (period) and pulse measurement. The dsPIC33FJXXXMCX06A/X08A/X10A devices support up to eight input capture channels.

The input capture module captures the 16-bit value of the selected Time Base register when an event occurs at the ICx pin. The events that cause a capture event are listed below in three categories:

1. Simple Capture Event modes

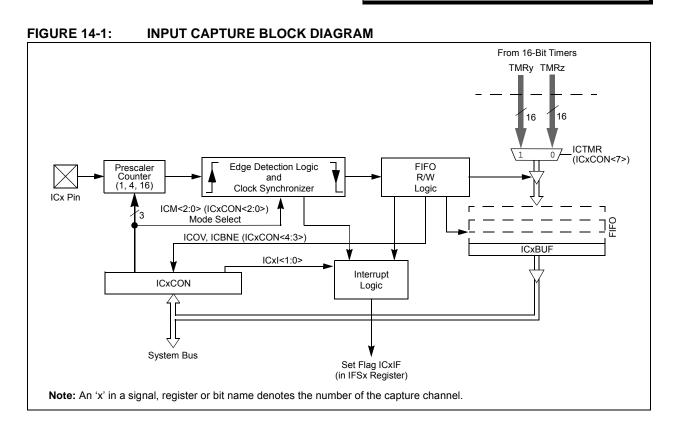
input at ICx pin

- Capture timer value on every - Capture timer value on every
- input at ICx pin 2. Capture timer value on every edge (rising and falling) of input at ICx pin 扫一扫上面的二维码图案,加我为朋友
- 3. Prescaler Capture Event modes
 - Capture timer value on every 4th rising edge of input at ICx pin
 - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base. The selected timer can use either an internal or external clock.

Other operational features include the following:

- · Device wake-up from capture pin during CPU Sleep and Idle modes
- · Interrupt on input capture event
- · 4-word FIFO buffer for capture values
 - Interrupt optionally generated after 1, 2, 3 or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts
- Only IC1 and IC2 can trigger a DMA data Note: transfer. If DMA data transfers are required, the FIFO buffer size must be set to '1' (ICI<1:0> = 00).







14.1 Input Capture Registers

REGISTER 14-1: ICxCON: INPUT CAPTURE x CONTROL REGISTER

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	
—	—	ICSIDL	—	—	—	—	
bit 15							扫一扫上面的二维硝图案,加我为朋友 Dit O

R/W-0	R/W-0	R/W-0	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0
ICTMR ⁽¹⁾	ICI<	:1:0>	ICOV	ICBNE		ICM<2:0>	
bit 7							bit 0

Legend:		HC = Hardware	Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13	ICSIDL: Input Capture Module Stop in Idle Control bit
	1 = Input capture module will halt in CPU Idle mode
	0 = Input capture module will continue to operate in CPU Idle mode
bit 12-8	Unimplemented: Read as '0'
bit 7	ICTMR: Input Capture Timer Select bits ⁽¹⁾
	 1 = TMR2 contents are captured on capture event 0 = TMR3 contents are captured on capture event
bit 6-5	ICI<1:0>: Select Number of Captures per Interrupt bits
	11 = Interrupt on every fourth capture event
	10 = Interrupt on every third capture event
	 01 = Interrupt on every second capture event 00 = Interrupt on every capture event
bit 4	ICOV: Input Capture Overflow Status Flag bit (read-only)
	1 = Input capture overflow occurred
	0 = No input capture overflow occurred
bit 3	ICBNE: Input Capture Buffer Empty Status bit (read-only)
	 1 = Input capture buffer is not empty; at least one more capture value can be read 0 = Input capture buffer is empty
bit 2-0	ICM<2:0>: Input Capture Mode Select bits
	 111 = Input capture functions as interrupt pin only when device is in Sleep or Idle mode (Rising edge detect only, all other control bits are not applicable.) 110 = Unused (module disabled) 101 = Capture mode, every 16th rising edge 100 = Capture mode, every 4th rising edge 011 = Capture mode, every rising edge
	 010 = Capture mode, every falling edge 001 = Capture mode, every edge (rising and falling) (ICI<1:0> bits do not control interrupt generation for this mode.) 000 = Input capture module turned off

15.0 OUTPUT COMPARE

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/ X08A/X10A families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "dsPIC33F/PIC24H Family Reference Manual", Section 13. "Output Compare" (DS70209), which is available on the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The output compare module can sele the Timer3 for its time base. The mod value of the timer with the value of convergence of the output pin change value matches the Compare register value. The compare module generates either a single

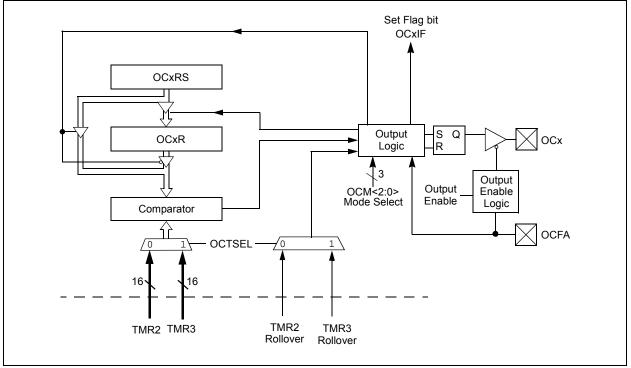


compare module generates either a single output multipulse, or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events.

The output compare module has multiple operating modes:

- Active-Low One-Shot mode
- Active-High One-Shot mode
- Toggle mode
- · Delayed One-Shot mode
- Continuous Pulse mode
- PWM mode without Fault Protection
- PWM mode with Fault Protection

FIGURE 15-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



15.1 Output Compare Modes

Configure the Output Compare modes by setting the appropriate Output Compare Mode bits (OCM<2:0>) in the Output Compare Control register (OCxCON<2:0>). Table 15-1 lists the different bit settings for the Output Compare modes. Figure 15-2 illustrates the output compare operation for various modes. The user

TABLE 15-1: OUTPUT COMPARE MODES

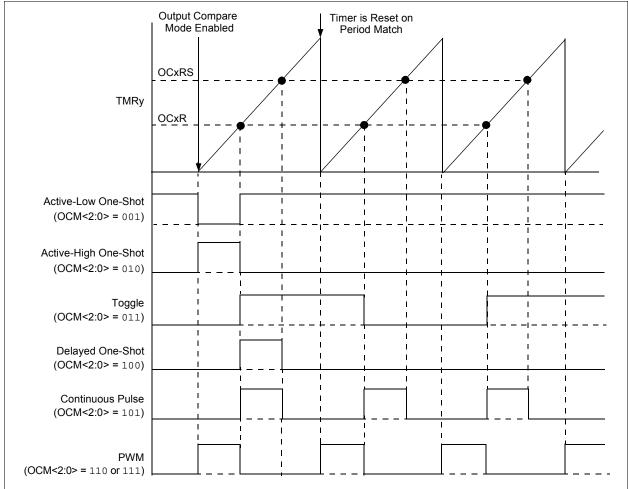
application must disable the associated writing to the Output Compare Contro avoid malfunctions.

Note: See Section 13. "Output (DS70209) in the "dsPIC Family Reference Manual" for OCxR and OCxRS register restrictions.

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OCM<2:0>	Mode	OCx Pin Initial State	OCx Interrupt Generation
000	Module Disabled	Controlled by GPIO register	_
001	Active-Low One-Shot	0	OCx rising edge
010	Active-High One-Shot	1	OCx falling edge
011	Toggle	Current output is maintained	OCx rising and falling edge
100	Delayed One-Shot	0	OCx falling edge
101	Continuous Pulse	0	OCx falling edge
110	PWM without Fault Protection	'0' if OCxR is zero,'1' if OCxR is non-zero	No interrupt
111	PWM with Fault Protection	'0' if OCxR is zero,'1' if OCxR is non-zero	OCFA falling edge for OC1 to OC4

FIGURE 15-2: OUTPUT COMPARE OPERATION





REGISTER 15-1: OCxCON: OUTPUT COMPARE x CONTROL REGISTER (x = 1, 2)

						0_0	
U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	
—	—	OCSIDL	—	—	—	—	T
bit 15							

U-0	U-0	U-0	R-0, HC	R/W-0	R/W-0	R/W-0	R/W-0
	_	—	OCFLT	OCTSEL		OCM<2:0>	
bit 7	l			I	I.		bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13	OCSIDL: Stop Output Compare in Idle Mode Control bit
	1 = Output Compare x halts in CPU Idle mode
	0 = Output Compare x continues to operate in CPU Idle mode
bit 12-5	Unimplemented: Read as '0'
bit 4	OCFLT: PWM Fault Condition Status bit
	1 = PWM Fault condition has occurred (cleared in hardware only)
	0 = No PWM Fault condition has occurred (this bit is only used when OCM<2:0> = 111)
bit 3	OCTSEL: Output Compare Timer Select bit
	1 = Timer3 is the clock source for Compare x
	0 = Timer2 is the clock source for Compare x
bit 2-0	OCM<2:0>: Output Compare Mode Select bits
	111 = PWM mode on OCx, Fault pin enabled
	110 = PWM mode on OCx, Fault pin disabled
	101 = Initialize OCx pin low, generate continuous output pulses on OCx pin
	100 = Initialize OCx pin low, generate single output pulse on OCx pin
	011 = Compare event toggles OCx pin
	010 = Initialize OCx pin high, compare event forces OCx pin low
	 001 = Initialize OCx pin low, compare event forces OCx pin high 000 = Output compare channel is disabled
	000 - Output compare channel is disabled

NOTES:



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16.0 MOTOR CONTROL PWM MODULE

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/ X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 14. "Motor Control PWM" (DS70187) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

This module simplifies the task of generating multiple, synchronized Pulse-Width Modulated (PWM) outputs. In particular, the following power and motion control applications are supported by the PWM module:

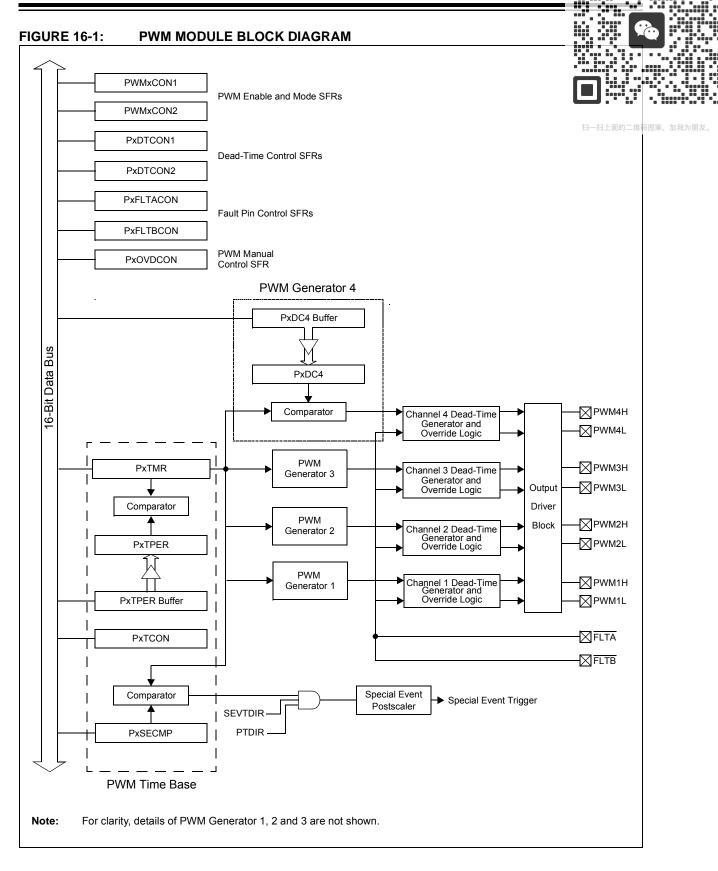
- · 3-Phase AC Induction Motor
- Switched Reluctance (SR) Motor
- Brushless DC (BLDC) Motor
- Uninterruptible Power Supply (UPS)

The PWM module has the followingEight PWM I/O pins with four duty

- Up to 16-bit resolution
- 'On-the-fly' PWM frequency chan
- Edge and Center-Aligned Output n
- Single Pulse Generation mode
- Interrupt support for asymmetrical updates in Center-Aligned mode
- Output override control for Electrically Commutative Motor (ECM) operation
- Special Event' comparator for scheduling other peripheral events
- Fault pins to optionally drive each of the PWM output pins to a defined state
- Duty cycle updates are configurable to be immediate or synchronized to the PWM time base

This module contains four duty cycle generators, numbered 1 through 4. The module has eight PWM output pins, numbered PWM1H/PWM1L through PWM4H/PWM4L. The eight I/O pins are grouped into high/low numbered pairs, denoted by the suffix H or L, respectively. For complementary loads, the low PWM pins are always the complement of the corresponding high I/O pin.

The PWM module allows several modes of operation which are beneficial for specific power control applications.





REGISTER 16-1: PXTCON: PWMx TIME BASE CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0
PTEN	—	PTSIDL	—	—	—	— [
bit 15						L

						1=		加我内
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	PTOPS	<3:0>		PTCK	PS<1:0>	PTMO	D<1:0>	
bit 7							bit 0	

Legend:						
R = Readable	bit W = Writable	e bit U = Unimplemented	bit, read as '0'			
-n = Value at I	POR '1' = Bit is se	et '0' = Bit is cleared	x = Bit is unknown			
bit 15	PTEN: PWM Time Base Ti	imer Enable bit				
	1 = PWM time base is on					
L:1 4 4	0 = PWM time base is off					
bit 14	Unimplemented: Read as					
bit 13	PTSIDL: PWM Time Base	•				
	 1 = PWM time base halts i 0 = PWM time base runs ir 					
bit 12-8	Unimplemented: Read as					
bit 7-4	PTOPS<3:0>: PWM Time Base Output Postscale Select bits					
2	1111 = 1:16 postscale					
	•					
	•					
	0001 = 1:2 postscale					
	0000 = 1:1 postscale					
bit 3-2	PTCKPS<1:0>: PWM Time	e Base Input Clock Prescale Select bi	its			
	•	t clock period is 64 Tcy (1:64 prescale	,			
		t clock period is 16 Tcy (1:16 prescale	2)			
	•	t clock period is 4 TCY (1:4 prescale) t clock period is TCY (1:1 prescale)				
bit 1-0	PTMOD<1:0>: PWM Time					
		rates in a Continuous Up/Down Coun	nt mode with interrupts for double			
	PWM updates					
	•	rates in a Continuous Up/Down Coun	it mode			
		rates in a Single Pulse mode				
	00 = PWM time base ope	erates in a Free-Running mode				



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REGISTER 16-2: PxTMR: PWMx TIMER COUNT VALUE REGISTER

							0_0_000
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
PTDIR				PTMR<14:8>	>		
bit 15							
							扫一扫
							DA

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTMF	R<7:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 PTDIR: PWM Time Base Count Direction Status bit (read-only) 1 = PWM time base is counting down 0 = PWM time base is counting up

bit 14-0 **PTMR <14:0>:** PWM Time Base Register Count Value bits

REGISTER 16-3: PxTPER: PWMx TIME BASE PERIOD REGISTER

R/W-0	R/W-0	R/W-0		
>				
		bit 8		
R/W-0	R/W-0	R/W-0		
		bit 0		
U = Unimplemented bit, read as '0'				
ared	d as '0' x = Bit is unknown			
		nented bit, read as '0'		

bit 15 Unimplemented: Read as '0'

bit 14-0 PTPER<14:0>: PWM Time Base Period Value bits



REGISTER 16-4: PXSECMP: PWMx SPECIAL EVENT COMPARE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTDIR ⁽¹⁾			SI	EVTCMP<14:8	_{}>} (2)	
bit 15						bit of the second se
						扫一扫上面的二维码图案,加我

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
SEVTCMP<7:0> ⁽²⁾								
bit 7							bit 0	

Legend:						
R = Readable bit	W = Writable bit	U = Unimplemented bit,	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 15SEVTDIR: Special Event Trigger Time Base Direction bit⁽¹⁾1 = A Special Event Trigger will occur when the PWM time base is counting downwards0 = A Special Event Trigger will occur when the PWM time base is counting upwardsbit 14-0SEVTCMP<14:0>: Special Event Compare Value bits⁽²⁾

Note 1: SEVTDIR is compared with PTDIR (PTMR<15>) to generate the Special Event Trigger.

2: SEVTCMP<14:0> is compared with PTMR<14:0> to generate the Special Event Trigger.



REGISTER 16-5: PWMxCON1: PWMx CONTROL REGISTER 1

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
—	—	—	—	PMOD4	PMOD3	PMOD2	
bit 15							C

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R/W-1	1							
PEN4H ⁽¹⁾	PEN3H ⁽¹⁾	PEN2H ⁽¹⁾	PEN1H ⁽¹⁾	PEN4L ⁽¹⁾	PEN3L ⁽¹⁾	PEN2L ⁽¹⁾	PEN1L ⁽¹⁾	ĺ
bit 7							bit 0	1

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12	Unimplemented: Read as '0'
bit 11-8	PMOD<4:1>: PWM I/O Pair Mode bits
	 1 = PWM I/O pin pair is in the Independent PWM Output mode 0 = PWM I/O pin pair is in the Complementary Output mode
bit 7-4	PEN4H:PEN1H: PWMxH I/O Enable bits ⁽¹⁾
	 1 = PWMxH pin is enabled for PWM output 0 = PWMxH pin is disabled; I/O pin becomes general purpose I/O
bit 3-0	PEN4L:PEN1L: PWMxL I/O Enable bits ⁽¹⁾
	1 = PWMxL pin is enabled for PWM output
	0 = PWMxL pin is disabled; I/O pin becomes general purpose I/O

Note 1: Reset condition of the PENxH and PENxL bits depends on the value of the PWMPIN Configuration bit in the FPOR Configuration register.

REGISTER 16-6: PWMxCON2: PWMx CONTROL REGISTER 2



LOISTEN					∠		
U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/74-0
—	—	—	_		SEVO	PS<3:0>	
t 15							bit 8
						扫·	一扫上面的二维码图案
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
_		<u> </u>			IUE	OSYNC	UDIS
it 7							bit 0
egend:							
= Readabl	e bit	W = Writable	bit	U = Unimpler	nented bit, rea	d as '0'	
i = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	iown
	1111 = 1:16 •						
	0001 = 1:2 p 0000 = 1:1 p						
it 7-3	Unimplemer	nted: Read as ')'				
t 2	IUE: Immedia	ate Update Ena	ble bit				
		to the active PD to the active PD			ed to the PWM	time base	
it 1	OSYNC: Out	put Override Sy	nchronizatio	n bit			
		verrides via the verrides via the				PWM time base dary	9
t 0		Update Disable					
		from Duty Cycle from Duty Cycle					



REGISTER 16-7: PxDTCON1: PWMx DEAD-TIME CONTROL REGISTER 1

								•••••	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	- EW-D		
DTBF	PS<1:0>			DTE	8<5:0>				
bit 15							• bi t •8	•	
							扫一扫上面的二维码	马图案,加我:	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
DTAF	PS<1:0>			DTA	<5:0>				
bit 7							bit 0		
Legend:									
R = Readable	e bit	W = Writable bi	t	U = Unimpler	nented bit, rea	id as '0'			
n = Value at	n = Value at POR '1' =			'0' = Bit is cleared			x = Bit is unknown		
bit 15-14	11 = Clock p 10 = Clock p 01 = Clock p	Dead-Time Uni eriod for Dead-Tin eriod for Dead-Tin eriod for Dead-Tin eriod for Dead-Tin eriod for Dead-Tin	me Unit B is me Unit B is me Unit B is	8 TCY 4 TCY 2 TCY					
bit 13-8	DTB<5:0>: \	Jnsigned 6-Bit De	ad-Time Val	lue for Dead-Ti	me Unit B bits	i			
bit 13-8 bit 7-6	DTAPS<1:0= 11 = Clock p 10 = Clock p 01 = Clock p	Jnsigned 6-Bit De .: Dead-Time Unit eriod for Dead-Tin eriod for Dead-Tin eriod for Dead-Tin eriod for Dead-Tin eriod for Dead-Tin	t A Prescale ne Unit A is ne Unit A is ne Unit A is	e Select bits 8 Tcy 4 Tcy 2 Tcy	me Unit B bits				



REGISTER 16-8: PxDTCON2: PWMx DEAD-TIME CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	- 6
bit 15						Ľ

								加我为
R/W-0	1							
DTS4A	DTS4I	DTS3A	DTS3I	DTS2A	DTS2I	DTS1A	DTS1I	ĺ
bit 7							bit 0	

Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 15-8	Unimplemented: Read as '0'						
bit 7	DTS4A: Dead-Time Select for PWM4 Signal Going Active bit						
	1 = Dead time provided from Unit B0 = Dead time provided from Unit A						
bit 6	DTS4I: Dead-Time Select for PWM4 Signal Going Inactive bit						
	1 = Dead time provided from Unit B0 = Dead time provided from Unit A						
bit 5	DTS3A: Dead-Time Select for PWM3 Signal Going Active bit						
	1 = Dead time provided from Unit B0 = Dead time provided from Unit A						
bit 4	DTS3I: Dead-Time Select for PWM3 Signal Going Inactive bit						
	1 = Dead time provided from Unit B0 = Dead time provided from Unit A						
bit 3	DTS2A: Dead-Time Select for PWM2 Signal Going Active bit						
	1 = Dead time provided from Unit B0 = Dead time provided from Unit A						
bit 2	DTS2I: Dead-Time Select for PWM2 Signal Going Inactive bit						
	1 = Dead time provided from Unit B0 = Dead time provided from Unit A						
bit 1	DTS1A: Dead-Time Select for PWM1 Signal Going Active bit						
	1 = Dead time provided from Unit B0 = Dead time provided from Unit A						
bit 0	DTS1I: Dead-Time Select for PWM1 Signal Going Inactive bit						
	1 = Dead time provided from Unit B0 = Dead time provided from Unit A						



REGISTER 16-9: PxFLTACON: PWMx FAULT A CONTROL REGISTER

| R/W-0 |
|--------|--------|--------|--------|--------|--------|--------|
| FAOV4H | FAOV4L | FAOV3H | FAOV3L | FAOV2H | FAOV2L | FAOV1H |
| bit 15 | • | | | • | | |

							扫一扫上面的二维码	马图案,加我为朋友。
R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	
FLTAM	—	—	—	FAEN4	FAEN3	FAEN2	FAEN1	
bit 7							bit 0	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR '1' = Bit is set		'0' = Bit is cleared	x = Bit is unknown

bit 15-8	FAOVxH<4:1>:FAOVxL<4:1>: Fault Input A PWM Override Value bits
	1 = The PWM output pin is driven active on an external Fault input event
	0 = The PWM output pin is driven inactive on an external Fault input event
bit 7	FLTAM: Fault A Mode bit
	1 = The Fault A input pin functions in the Cycle-by-Cycle mode0 = The Fault A input pin latches all control pins to the states programmed in FLTACON<15:8>
bit 6-4	Unimplemented: Read as '0'
bit 3	FAEN4: Fault Input A Enable bit
	1 = PWM4H/PWM4L pin pair is controlled by Fault Input A
	0 = PWM4H/PWM4L pin pair is not controlled by Fault Input A
bit 2	FAEN3: Fault Input A Enable bit
	1 = PWM3H/PWM3L pin pair is controlled by Fault Input A
	0 = PWM3H/PWM3L pin pair is not controlled by Fault Input A
bit 1	FAEN2: Fault Input A Enable bit
	1 = PWM2H/PWM2L pin pair is controlled by Fault Input A
	0 = PWM2H/PWM2L pin pair is not controlled by Fault Input A
bit 0	FAEN1: Fault Input A Enable bit
	1 = PWM1H/PWM1L pin pair is controlled by Fault Input A
	0 = PWM1H/PWM1L pin pair is not controlled by Fault Input A

REGISTER 16-10: PxFLTBCON: PWMx FAULT B CONTROL REGISTER



R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 FBOV4H FBOV4L FBOV3H FBOV3L FBOV2H FBOV2L FBOV1 bit 15 R/W-0 U-0 U-0 U-0 R/W-0 R/W-0 R/W-0 R/W-0 FBFN4⁽¹⁾ FBFN3(1) FBFN2⁽¹⁾ FBFN1⁽¹⁾ **FLTBM** bit 7 bit 0 Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15-8 FBOVxH<4:1>:FBOVxL<4:1>: Fault Input B PWM Override Value bits 1 = The PWM output pin is driven active on an external Fault input event 0 = The PWM output pin is driven inactive on an external Fault input event bit 7 FLTBM: Fault B Mode bit 1 = The Fault B input pin functions in the Cycle-by-Cycle mode 0 = The Fault B input pin latches all control pins to the states programmed in FLTBCON<15:8> bit 6-4 Unimplemented: Read as '0' bit 3 **FBEN4:** Fault Input B Enable bit⁽¹⁾ 1 = PWM4H/PWM4L pin pair is controlled by Fault Input B 0 = PWM4H/PWM4L pin pair is not controlled by Fault Input B FBEN3: Fault Input B Enable bit⁽¹⁾ bit 2 1 = PWM3H/PWM3L pin pair is controlled by Fault Input B 0 = PWM3H/PWM3L pin pair is not controlled by Fault Input B FBEN2: Fault Input B Enable bit⁽¹⁾ bit 1 1 = PWM2H/PWM2L pin pair is controlled by Fault Input B 0 = PWM2H/PWM2L pin pair is not controlled by Fault Input B FBEN1: Fault Input B Enable bit(1) bit 0 1 = PWM1H/PWM1L pin pair is controlled by Fault Input B 0 = PWM1H/PWM1L pin pair is not controlled by Fault Input B

Note 1: Fault A pin has priority over Fault B pin, if enabled.



REGISTER 16-11: PXOVDCON: PWMx OVERRIDE CONTROL REGISTER

R/W-1							
POVD4H	POVD4L	POVD3H	POVD3L	POVD2H	POVD2L	POVD1H	
bit 15							

							扫一扫上面的二维码	冯图案,
R/W-0								
POUT4H	POUT4L	POUT3H	POUT3L	POUT2H	POUT2L	POUT1H	POUT1L	
bit 7							bit 0	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 POVDxH<4:1>:POVDxL<4:1>: PWM Output Override bits

1 = Output on PWMx I/O pin is controlled by the PWM generator

0 = Output on PWMx I/O pin is controlled by the value in the corresponding POUTxH:POUTxL bit

bit 7-0 POUTxH<4:1>:POUTxL<4:1>: PWM Manual Output bits

1 = PWMx I/O pin is driven active when the corresponding POVDxH:POVDxL bit is cleared

0 = PWMx I/O pin is driven inactive when the corresponding POVDxH:POVDxL bit is cleared



x = Bit is unknown

REGISTER 16-12: PxDC1: PWMx DUTY CYCLE REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R474-0	
			PDC1	<15:8>				
bit 15							bit-8	
							扫一扫上面的二维码图案,	加我为朋友。
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			PDC	1<7:0>				
bit 7							bit 0	
Legend:								
R = Readable bit		W = Writable bit		U = Unimpler	nented bit, read	l as '0'		

'0' = Bit is cleared

bit 15-0 **PDC1<15:0>:** PWM Duty Cycle #1 Value bits

-n = Value at POR

REGISTER 16-13: PxDC2: PWMx DUTY CYCLE REGISTER 2

'1' = Bit is set

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDC	2<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDC	2<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable I	bit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 PDC2<15:0>: PWM Duty Cycle #2 Value bits



REGISTER 16-14: PxDC3: PWMx DUTY CYCLE REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	- EXV-D
			PDC	3<15:8>			
bit 15							bit-8
							<u> 扫一扫上面的二维码</u> 图案,
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDC	3<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit		W = Writable bit	t	U = Unimpler	nented bit, rea	id as '0'	
-n = Value at PO	R	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown

bit 15-0 PDC3<15:0>: PWM Duty Cycle #3 Value bits

REGISTER 16-15: PxDC4: PWMx DUTY CYCLE REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDC	4<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDC	4<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	bit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 PDC4<15:0>: PWM Duty Cycle #4 Value bits

17.0 QUADRATURE ENCODER INTERFACE (QEI) MODULE

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 15. "Quadrature Encoder Interface (QEI)" (DS70208) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

This section describes the Quadrature face (QEI) module and associated of The QEI module provides the interface encoders for obtaining mechanical per

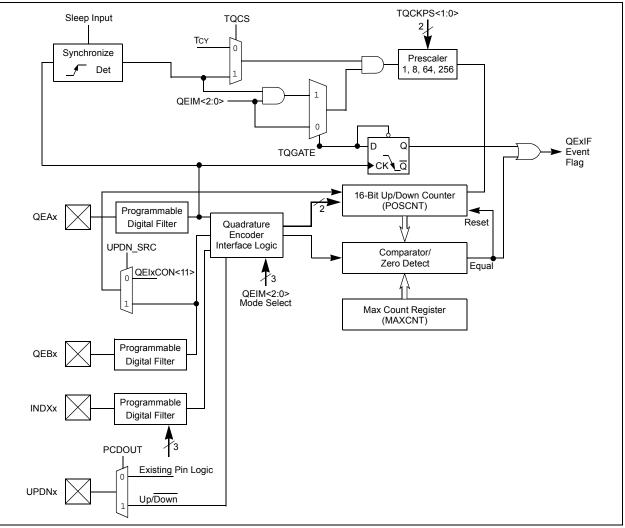


The operational features of the following:

- 扫一扫上面的二维码图案,加我为朋友。 phase signals and
- Three input channels for two phase signals and an index pulse
- 16-bit up/down position counter
- Count direction status
- Position Measurement (x2 and x4) mode
- Programmable digital noise filters on inputs
- Alternate 16-Bit Timer/Counter mode
- · Quadrature Encoder Interface interrupts

The QEI module's operating mode is determined by setting the appropriate bits, QEIM<2:0> (QEIxCON<10:8>). Figure 17-1 depicts the Quadrature Encoder Interface block diagram.





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REGISTER 17-1: QEIXCON: QEIX CONTROL REGISTER

 br 8	

								••••••••
R/W-0	U-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	RW0	
CNTERR		QEISIDL	INDEX	UPDN		QEIM<2:0>	▁┃■┃ःःःः	
bit 15							bit 8	
		-		5444.0			扫一扫上面的二维码	8图案,加我为月
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
SWPAB	PCDOUT	TQGATE	TQCK	PS<1:0>	POSRES	TQCS	UPDN_SRC ⁽¹⁾	
bit 7							bit 0	
_egend:								
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, rea	d as '0'		
-n = Value at F		'1' = Bit is set		'0' = Bit is cl		x = Bit is unk	nown	
bit 15	CNTERR: Co	ount Error Statu	is Flag hit					
		count error has	-					
		on count error l						
	(CNTERR fla	g only applies	when QEIM<	2:0> = '110' o	r'100')			
bit 14	Unimplemer	ted: Read as '	0'					
bit 13		op in Idle Mode						
		ue module ope			Idle mode			
		module operat						
bit 12		k Pin State Stat	us bit (read-o	only)				
	1 = Index pin 0 = Index pin	-						
bit 11	•	ion Counter Dir	ection Status	bit				
		counter directio						
		counter directio						
	(Read-only b	it when QEIM<	2:0> = '1xx'.	Read/write bit	when QEIM<2	: 0> = 001.)		
bit 10-8	QEIM<2:0>:	Quadrature En	coder Interfa	ce Mode Seleo	ct bits			
							natch (MAXCNT)	
					e) with Index Pu		natch (MAXCNT)	
					e) with Index Pu			
	011 = Unuse	d (module disa	bled)		,			
		d (module disa	bled)					
	001 = Starts	16-bit Timer ature Encoder	Interface/time	er off				
bit 7		ase A and Phas						
		and Phase B ir	•	•				
		and Phase B ir						
bit 6	PCDOUT: Pc	sition Counter	Direction Sta	te Output Ena	ble bit			
				-	I logic controls	state of I/O pin)	
	0 = Position of	counter directio	n status outp	ut disabled (n	ormal I/O pin op	peration)		
bit 5	TQGATE: Tir	ner Gated Time	e Accumulatio	on Enable bit				
	1 = Timer gat	ted time accum	ulation enabl	ed				
		ted time accum						

REGISTER 17-1: QEIXCON: QEIX CONTROL REGISTER (CONTINUED) bit 4-3 TQCKPS<1:0>: Timer Input Clock Prescale Select bits 11 = 1:256 prescale value 10 = 1:64 prescale value 01 = 1:8 prescale value 00 = 1:1 prescale value 扫一扫上面的二维码图案,加我为朋友。 (Prescaler utilized for 16-Bit Timer mode only.) bit 2 POSRES: Position Counter Reset Enable bit 1 = Index pulse resets position counter 0 = Index pulse does not reset position counter (Bit only applies when QEIM<2:0> = 100 or 110.) bit 1 TQCS: Timer Clock Source Select bit 1 = External clock from QEA pin (on the rising edge) 0 = Internal clock (TCY) UPDN_SRC: Position Counter Direction Selection Control bit⁽¹⁾ bit 0 1 = QEB pin state defines position counter direction 0 = Control/status bit, UPDN (QEICON<11>), defines Position Counter (POSxCNT) direction

Note 1: When configured for QEI mode, the control bit is a 'don't care'.



REGISTER 17-2: DFLTxCON: DIGITAL FILTER x CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	HANNED
_	—		—	—	IMV<	<2:0>	
bit 15							• bit 8
							扫一扫上面的二维
R/W-0		R/W-0		U-0	U-0	U-0	U-0
QEOUT		QECK<2:0>			—		<u> </u>
bit 7							bit 0
Legend:							
R = Readabl	e bit	W = Writable	bit	U = Unimplei	mented bit, read	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown
bit 15-11	Unimplem	nented: Read as '	o'				
bit 10-9	IMV<1:0>:	Index Match Valu	e bits				
	<u>In 4X Qua</u> IMV1 = Re IMV0 = Re	POSxCNT register drature Count Mod equired state of Ph equired state of Ph drature Count Mod	<u>de:</u> ase B input : ase A input :	signal for match			
	<u>In 4X Qua</u> IMV1 = Re IMV0 = Re <u>In 2X Qua</u> IMV1 = Se	drature Count Mod equired state of Ph	<u>de:</u> ase B input s ase A input s <u>de:</u> signal for inc	signal for match signal for match lex state match	on index pulse (0 = Phase A, 1	e 1 = Phase B)	
bit 8	In 4X Qua IMV1 = Re IMV0 = Re In 2X Qua IMV1 = Se IMV0 = Re CEID: Cou 1 = Interru	drature Count Mod equired state of Ph equired state of Ph drature Count Mod elects phase input	<u>de:</u> ase B input : ase A input : d <u>e:</u> signal for inc e selected Ph Disable bit rrors are disa	signal for match signal for match lex state match nase input signa abled	on index pulse (0 = Phase A, 1	e 1 = Phase B)	
bit 8 bit 7	In 4X Qua IMV1 = Re IMV0 = Re IMV1 = Se IMV0 = Re CEID: Cou 1 = Interru 0 = Interru QEOUT: C 1 = Digital	drature Count Moc equired state of Ph equired state of Ph drature Count Moc elects phase input equired state of the unt Error Interrupt I pts due to count e pts due to count e QEAx/QEBx/INDXx filter outputs enab	de: ase B input : ase A input : signal for inc e selected Pr Disable bit rrors are dis rrors are ena c Pin Digital F oled	signal for match signal for match lex state match nase input signa abled abled =ilter Output En	on index pulse (0 = Phase A, 3 Il for match on i	e 1 = Phase B)	
	In 4X Qua IMV1 = Re IMV0 = Re IMV1 = Se IMV0 = Re CEID: Cou 1 = Interru 0 = Interru QEOUT: C 1 = Digital 0 = Digital	drature Count Moc equired state of Ph drature Count Moc elects phase input equired state of the unt Error Interrupt I upts due to count e upts due to count e EAx/QEBx/INDXx filter outputs enab	de: ase B input : ase A input : signal for inc e selected Ph Disable bit rrors are disa rrors are ena c Pin Digital F oled oled (normal	signal for match signal for match lex state match nase input signa abled abled Filter Output En pin operation)	on index pulse (0 = Phase A, : Il for match on i able bit	e 1 = Phase B)	
bit 7	In 4X Qua IMV1 = Re IMV0 = Re IMV0 = Re IMV0 = Re CEID: Cou 1 = Interru 0 = Interru QEOUT: C 1 = Digital 0 = Digital QECK<2:(111 = 1:2; 110 = 1:12; 101 = 1:64 100 = 1:3; 011 = 1:4 001 = 1:2	drature Count Moc equired state of Ph equired state of Ph drature Count Moc elects phase input equired state of the unt Error Interrupt I pts due to count e pts due to count e QEAx/QEBx/INDXx filter outputs enab	de: ase B input : ase A input : signal for inc e selected Ph Disable bit rrors are disa rrors are ena c Pin Digital F oled oled (normal	signal for match signal for match lex state match nase input signa abled abled Filter Output En pin operation)	on index pulse (0 = Phase A, : Il for match on i able bit	e 1 = Phase B)	

18.0 SERIAL PERIPHERAL INTERFACE (SPI)

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/X08A/ X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 18. "Serial Peripheral Interface (SPI)" (DS70206) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Serial Peripheral Interface (SPI) module is a synchronous serial interface useful for communicating with other peripheral or microcontroller devices. These

peripheral devices may be serial registers, display drivers, ADC, etc. T compatible with SPI and SIOP from

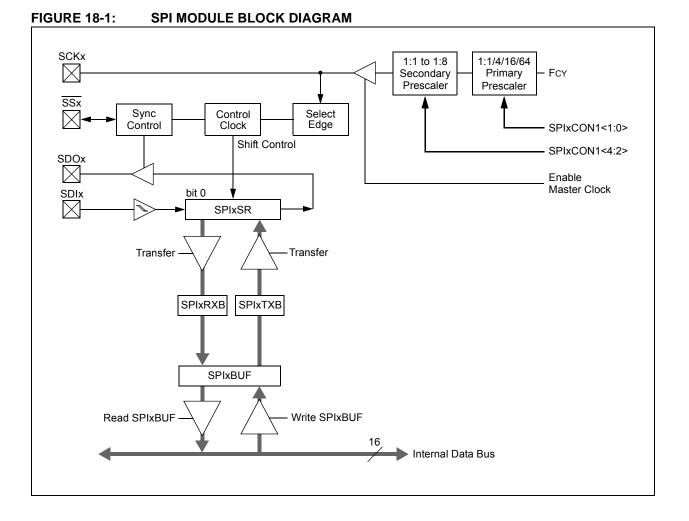


Note:	In this section, the Standard are referred to together as SPIx, or sepa-
	rately as SPI1 and SPI2. Special Functions, mathematical mathematica
	Registers will follow a similar notation.
	For example, SPIxCON refers to the
	control register for the SPI1 or SPI2
	module.

Each SPI module consists of a 16-bit shift register, SPIxSR (where x = 1 or 2), used for shifting data in and out, and a buffer register, SPIxBUF. A control register, SPIxCON, configures the module. Additionally, a status register, SPIxSTAT, indicates various status conditions.

The serial interface consists of 4 pins: SDIx (Serial Data Input), SDOx (Serial Data Output), SCKx (Shift Clock Input or Output) and SSx (Active-Low Slave Select).

In Master mode operation, SCK is a clock output, but in Slave mode, it is a clock input.





18.1 SPI Helpful Tips

- 1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
 - a) If FRMPOL (SPIxCON2<13>) = 1, use a pull-down resistor on SSx.
 - b) If FRMPOL = 0, use a pull-up resistor on $\frac{1}{SSx}$.

Note:	This	insures	that	the	first	fr	ame
	transr	nission a	after	initializa	ation	is	not
	shifte	d or corru	pted.				

- 2. In non-framed 3-wire mode, (i.e., not using SSx from a master):
 - a) If CKP (SPIxCON1<6>) = 1, always place a pull-up resistor on SSx.
 - b) If CKP = 0, always place a pull-down resistor on \overline{SSx} .
- **Note:** This will insure that during power-up and initialization the master/slave will not lose sync due to an errant SCK transition that would cause the slave to accumulate data shift errors for both transmit and receive appearing as corrupted data.
- FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame sync pulse is active on the SSx pin, which indicates the start of a data frame.

Note:	Not all third-party devices support Frame
	mode timing. Refer to the SPI electrical
	characteristics for details.

- In Master mode only, set the SMP bit (SPIxCON1<9>) to a '1' for the fastest SPI data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.
- 5. To avoid invalid slave read data to the master, the user's master software must guarantee enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPI shift register and is empty once the data transmission begins.

18.2 SPI Resources

Many useful resources related to SPI are the main product page of the Microchip w devices listed in this data sheet. This p which can be accessed using this link, latest updates and additional information.



18.2.1 KEY RESOURCES

- Section 18. "Serial Peripheral Interface (SPI)" (DS70206)
- Code Samples
- Application Notes
- Software Libraries
- · Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

18.3 SPI Control Registers

REGISTER 18-1: SPIx STAT: SPIx STATUS AND CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	
SPIEN	—	SPISIDL	—		—	—	
bit 15							扫一扫上面的二维稳道紧,加我为朋友。

U-0	R/C-0	U-0	U-0	U-0	U-0	R-0	R-0
—	SPIROV	—	—	_	—	SPITBF	SPIRBF
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	SPIEN: SPIx Enable bit
	1 = Enables module and configures SCKx, SDOx, SDIx and \overline{SSx} as serial port pins 0 = Disables module
bit 14	Unimplemented: Read as '0'
bit 13	SPISIDL: Stop in Idle Mode bit
	 1 = Discontinue module operation when device enters Idle mode 0 = Continue module operation in Idle mode
bit 12-7	Unimplemented: Read as '0'
bit 6	SPIROV: Receive Overflow Flag bit
	 1 = A new byte/word is completely received and discarded. The user software has not read the previous data in the SPIxBUF register. 0 = No overflow has occurred
bit 5-2	Unimplemented: Read as '0'
bit 1	SPITBF: SPIx Transmit Buffer Full Status bit
	1 = Transmit not yet started; SPIxTXB is full
	0 = Transmit started; SPIxTXB is empty Automatically set in hardware when CPU writes SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when SPIx module transfers data from SPIxTXB to SPIxSR.
bit 0	SPIRBF: SPIx Receive Buffer Full Status bit
	1 = Receive complete; SPIxRXB is full
	0 = Receive is not complete; SPIxRXB is empty
	Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when core reads SPIxBUF location, reading SPIxRXB.



REGISTER [·]	18-2: SPIxC	CON1: SPIx CO	ONTROL R	EGISTER 1						
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	- EWP			
_	—	—	DISSCK	DISSDO	MODE16	SMP	rak			
t 15							bit-8			
							扫一扫上面的二维			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
SSEN ⁽³⁾	CKP	MSTEN		SPRE<2:0>(2	:)	PPRE	<1:0> (2)			
it 7							bit 0			
egend:										
R = Readable	e bit	W = Writable t	bit	U = Unimpler	nented bit, rea	d as '0'				
n = Value at		'1' = Bit is set		'0' = Bit is cle		x = Bit is unk	known			
it 15-13	Unimpleme	nted: Read as '0	,							
it 12	DISSCK: Dis	sable SCKx Pin I	oit (SPI Mast	ter modes only)						
		SPI clock is disa SPI clock is enat	•	ctions as I/O						
bit 11	DISSDO: Disable SDOx Pin bit									
		n is not used by n is controlled by								
pit 10	MODE16: W	/ord/Byte Comm	unication Sel	lect bit						
		nication is word-w nication is byte-w	•)						
vit 9		Data Input Sampl								
	Master mode			tput time						
	0 = Input data sampled at middle of data output time									
	Slave mode: SMP must b	e cleared when S	SPIx is used	in Slave mode						
oit 8		Clock Edge Selec								
	1 = Serial ou	utput data change	es on transiti							
oit 7		e Select Enable I								
		used for Slave m								
		not used by mod		trolled by port fu	inction.					
oit 6	CKP: Clock	Polarity Select b	it							
		e for clock is a hi e for clock is a lo								
oit 5	MSTEN: Ma	ster Mode Enabl	e bit							
	1 = Master n 0 = Slave mo									
		t used in the Fra	med SPI mc	odes. The user s	should program	n this bit to '0' f	or the Framed			
	PI modes (FRM	EN = 1).	acondary pre	evalers to a val	ue of 1.1					

- 2: Do not set both the primary and secondary prescalers to a value of 1:1.
- **3:** This bit must be cleared when FRMEN = 1.

REGISTER 18-2: SPIXCON1: SPIX CONTROL REGISTER 1 (CONTINUED)

bit 4-2 SPRE<2:0>: Secondary Prescale bits (Master mode)⁽²⁾ 111 = Secondary prescale 1:1 110 = Secondary prescale 2:1 •



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- 000 = Secondary prescale 8:1
- bit 1-0 **PPRE<1:0>:** Primary Prescale bits (Master mode)⁽²⁾
 - 11 = Primary prescale 1:1
 - 10 = Primary prescale 4:1
 - 01 = Primary prescale 16:1
 - 00 = Primary prescale 64:1
- **Note 1:** The CKE bit is not used in the Framed SPI modes. The user should program this bit to '0' for the Framed SPI modes (FRMEN = 1).
 - **2:** Do not set both the primary and secondary prescalers to a value of 1:1.
 - 3: This bit must be cleared when FRMEN = 1.



REGISTER 18-3: SPIxCON2: SPIx CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
FRMEN	SPIFSD	FRMPOL	—	—	—	—
bit 15						

							扫一扫上面的二维码	马图案,加我为朋友。
U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	
	—		_		—	FRMDLY	—	
bit 7							bit 0	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

FRMEN: Framed SPIx Support bit
 1 = Framed SPIx support enabled (SSx pin used as frame Sync pulse input/output) 0 = Framed SPIx support disabled
SPIFSD: Frame Sync Pulse Direction Control bit
1 = Frame Sync pulse input (slave)
0 = Frame Sync pulse output (master)
FRMPOL: Frame Sync Pulse Polarity bit
1 = Frame Sync pulse is active-high
0 = Frame Sync pulse is active-low
Unimplemented: Read as '0'
FRMDLY: Frame Sync Pulse Edge Select bit
1 = Frame Sync pulse coincides with first bit clock
0 = Frame Sync pulse precedes first bit clock
Unimplemented: This bit must not be set to '1' by the user application.

19.0 INTER-INTEGRATED CIRCUIT (I²C[™])

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/X08A/ X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 19. "Inter-Integrated Circuit (I²C[™])" (DS70195) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Inter-Integrated Circuit (I²C) module, with its 16-bit interface, provides complete hardware support for both Slave and Multi-Master modes of the I²C serial communication standard.

The dsPIC33FJXXXMCX06A/X08A/X10A devices have up to two I²C interface modules, denoted as I2C1 and I2C2. Each I²C module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each I^2C module 'x' (x = 1 or 2) offers the following key features:

- I²C interface supports both master and slave operation
- I²C Slave mode supports 7-bit and 10-bit addressing
- I²C Master mode supports 7 and 10-bit addressing
- I²C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the I²C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I²C supports multi-master operation: it detects bus collision and will arbitrate accordingly

19.1 **Operating Modes**

master on an I²C bus.

The hardware fully implements all th functions of the I²C Standard specifications, as well as 7 and 10-l



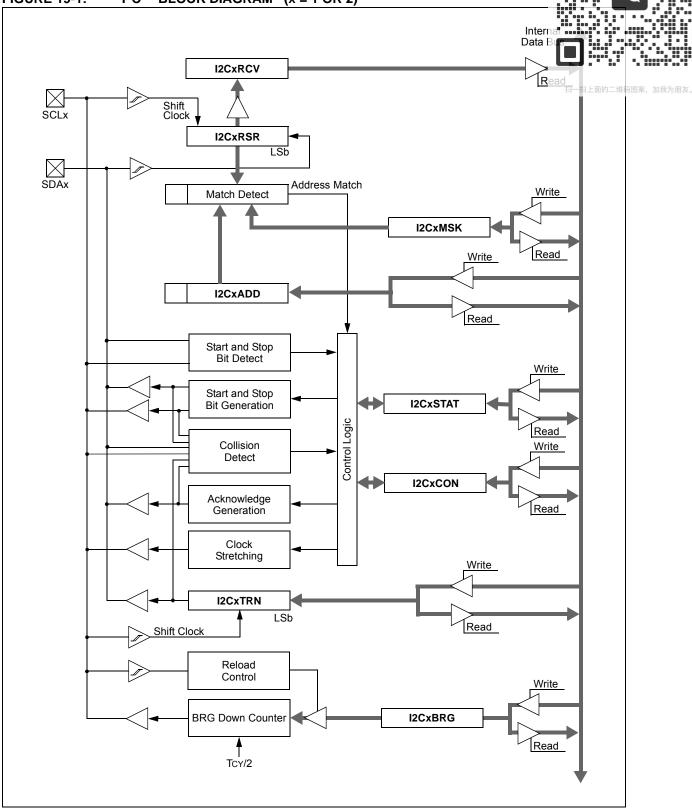
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The following types of I²C operation are supported:

- I²C slave operation with 7-bit addressing
- I²C slave operation with 10-bit addressing
- I²C master operation with 7-bit or 10-bit addressing

For details about the communication sequence in each of these modes, please refer to the "dsPIC33F/PIC24H Family Reference Manual".

FIGURE 19-1: I^2C^{TM} BLOCK DIAGRAM (x = 1 OR 2)





19.2 ²C Resources

Many useful resources related to I^2C are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser:
	http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en546066

19.2.1 KEY RESOURCES

- Section 11. "Inter-Integrated Circuit™ (I²C™)" (DS70195)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

19.3 I²C Control Register

I2CxCON and I2CxSTAT are corregisters, respectively. The I2Cx readable and writable. The lower siver read-only. The remaining bits of read/write.

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I2CxRSR is the shift register used for shifting data, whereas I2CxRCV is the buffer register to which data bytes are written, or from which data bytes are read. I2CxRCV is the receive buffer. I2CxTRN is the transmit register to which bytes are written during a transmit operation.

The I2CxADD register holds the slave address. A status bit, ADD10, indicates 10-bit Address mode. The I2CxBRG acts as the Baud Rate Generator (BRG) reload value.

In receive operations, I2CxRSR and I2CxRCV together form a double-buffered receiver. When I2CxRSR receives a complete byte, it is transferred to I2CxRCV and an interrupt pulse is generated.

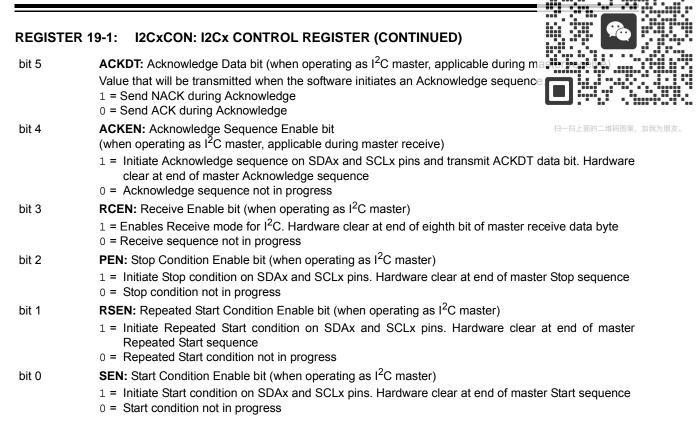


REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER

Ī	R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	
ſ	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	Γ
ſ	bit 15							Ľ

							扫一扫上面的二维码	马图案,加我为朋友。
R/W-0	R/W-0	R/W-0	R/W-0, HC					
GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	
bit 7							bit 0	

Legend:		U = Unimplemented bit, read as '0'						
R = Readable bit		W = Writable bit	HS = Hardware Settable bit	HC = Hardware Clearable bi				
-n = Value a	at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				
bit 15	1 = Enab		nfigures the SDAx and SCLx pins ™ pins are controlled by port func					
bit 14		mented: Read as '0'						
bit 13		: Stop in Idle Mode bit						
	1 = Disco		ien device enters an Idle mode e mode					
bit 12	SCLREL	: SCLx Release Control bit (when operating as I ² C slave)					
	0 = Hold <u>If STREN</u> Bit is R/V at beginr <u>If STREN</u>	V (i.e., software may write '0 ing of slave transmission. H ↓ = 0: ፩ (i.e., software may only writ	ch) ' to initiate stretch and write '1' to ardware clear at end of slave rece te '1' to release clock). Hardware o	ption.				
bit 11			ement Interface (IPMI) Enable bit					
	1 = IPMI	mode is enabled; all addres mode disabled						
bit 10	1 = I2Cx	0-Bit Slave Address bit ADD is a 10-bit slave addres ADD is a 7-bit slave address						
bit 9	1 = Slew	Disable Slew Rate Control rate control disabled rate control enabled	bit					
bit 8	1 = Enat	MBus Input Levels bit le I/O pin thresholds complia ble SMBus input thresholds	ant with SMBus specification					
bit 7	1 = Enal rece	General Call Enable bit (whe ble interrupt when a general ption) eral call address disabled	n operating as I ² C slave) call address is received in the I20	CxRSR (module is enabled for				
bit 6	STREN: Used in o 1 = Enab		stretching					





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REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	
ACKSTAT	TRSTAT		—	—	BCL	GCSTAT	
bit 15							

							扫一扫上面的二维码	图案,
R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	ĺ
IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	
bit 7 bit 0								

C = Clearable bit Settable bit HSC = Hardware Settable/Clearable bit ed x = Bit is unknown									
er transmit operation)									
transmit operation)									
 1 = Master transmit is in progress (8 bits + ACK) 0 = Master transmit is not in progress Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge. 									
 1 = A bus collision has been detected during a master operation 0 = No collision Hardware set at detection of bus collision. 									
dress. Hardware clear at Stop detection.									
t address. Hardware clear at Stop detection.									
·									
because the I ² C module is busy									
le busy (cleared by software).									
is still holding the previous byte									
KRCV (cleared by software).									
)									
e address									
set by reception of slave byte.									

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED) bit 4 P: Stop bit 1 = Indicates that a Stop bit has been detected last 0 = Stop bit was not detected last Hardware set or clear when Start, Repeated Start or Stop detected. bit 3 S: Start bit 1 = Indicates that a Start (or Repeated Start) bit has been detected last 0 = Start bit was not detected last Hardware set or clear when Start, Repeated Start or Stop detected. **R_W:** Read/Write Information bit (when operating as I²C slave) bit 2 1 = Read – indicates data transfer is output from slave 0 = Write – indicates data transfer is input to slave Hardware set or clear after reception of I²C device address byte. RBF: Receive Buffer Full Status bit bit 1 1 = Receive complete; I2CxRCV is full 0 = Receive not complete; I2CxRCV is empty Hardware set when I2CxRCV is written with received byte. Hardware clear when software reads I2CxRCV. bit 0 TBF: Transmit Buffer Full Status bit 1 = Transmit in progress, I2CxTRN is full 0 = Transmit complete, I2CxTRN is empty Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.



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REGISTER 19-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	_	_	_	—	AMSK9
bit 15						

							扫一扫上面的二维码图
R/W-0							
AMSK7	AMSK6	AMSK5	AMSK4	AMSK3	AMSK2	AMSK1	AMSK0
bit 7							bit 0

Legend:					
R = Readable bit	W = Writable bit	U = Unimplemented bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-10 Unimplemented: Read as '0'

bit 9-0

AMSKx: Mask for Address bit x Select bits

1 = Enable masking for bit x of incoming message address; bit match not required in this position

0 = Disable masking for bit x; bit match required in this position

20.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/ X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 17. "UART" (DS70188) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

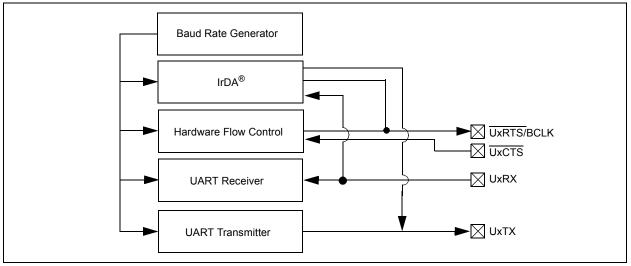
The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33FJXXXMCX06A/X08A/X10A device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the UxCTS and UxRTS pins and also includes an IrDA[®] encoder and decoder.

The primary features of the UART rFull-Duplex, 8-bit or 9-bit Data Tra



- through the UxTX and UxRX PinsEven, Odd or No Parity Options (for
- One or Two Stop bits
 - Hardware Flow Control Option with UxCTS and UxRTS Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Ranging from 10 Mbps to 38 bps at 40 MIPS
- 4-Deep First-In-First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-bit mode with Address Detect (9th bit = 1)
- · Transmit and Receive Interrupts
- A Separate Interrupt for all UART Error Conditions
- Loopback mode for Diagnostic Support
- Support for Sync and Break Characters
- Supports Automatic Baud Rate Detection
- IrDA Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA Support
- A simplified block diagram of the UART is shown in Figure 20-1. The UART module consists of these key important hardware elements:
- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver





- **Note 1:** Both UART1 and UART2 can trigger a DMA data transfer. If U1TX, U1RX, U2TX or U2RX is selected as a DMA IRQ source, a DMA transfer occurs when the U1TXIF, U1RXIF, U2TXIF or U2RXIF bit gets set as a result of a UART1 or UART2 transmission or reception.
 - 2: If DMA transfers are required, the UART TX/RX FIFO buffer must be set to a size of 1 byte/word (i.e., UTXISEL<1:0> = 00 and URXISEL<1:0> = 00).



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20.1 UART Helpful Tips

- 1. In multi-node direct-connect UART networks, receive inputs UART react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the idle state, the default of which is logic high, (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a start bit detection and will cause the first byte received after the device has been initialized to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
 - a) If URXINV = 0, use a pull-up resistor on the RX pin.
 - b) If URXINV = 1, use a pull-down resistor on the RX pin.
- 2. The first character received on a wake-up from Sleep mode caused by activity on the UxRX pin of the UART module will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock relative to the incoming UxRX bit timing is no longer synchronized, resulting in the first character being invalid. This is to be expected.

20.2 UART Resources

Many useful resources related to UART on the main product page of the Microchi the devices listed in this data sheet. This p which can be accessed using this link, latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en546066

20.2.1 KEY RESOURCES

- Section 17. "UART" (DS70188)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools



REGISTER 20-1: UXMODE: UARTX MODE REGISTER

REGISTER 2	U-1: UXMO	DE: UARTX M	ODE REGI	SIER						
R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	RW.0			
UARTEN ⁽¹⁾		USIDL	IREN ⁽²⁾	RTSMD	—	UEN	<1:0>			
it 15						扫	一扫上面的二维构体象,			
R/W-0, HC	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEI	_<1:0>	STSEL			
it 7			-			-	bit 0			
.egend:		HC = Hardwar	e Clearable b	oit						
R = Readable	bit	W = Writable b	bit	U = Unimpler	mented bit, read	as '0'				
n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown			
it 15	1 = UARTx is 0 = UARTx is minimal	NRTx Enable bit s enabled; all U/ s disabled; all U	ARTx pins are ARTx pins ar							
bit 14	-	ted: Read as '0	3							
bit 13		USIDL: Stop in Idle Mode bit 1 = Discontinue module operation when device enters Idle mode.								
		module operati			ale mode.					
pit 12		Encoder and De								
	1 = IrDA ence	oder and decod	er enabled							
bit 11		le Selection for		it						
		in in Simplex m in in Flow Conti								
oit 10	•	ted: Read as '0								
oit 9-8	UEN<1:0>: U	ARTx Enable b	its							
	10 = UxTX, U 01 = UxTX, U	UxRX and BCL UxRX, UxCTS a UxRX and UxR and UxRX pins a	and UxRTS p TS pins are e	ins are enable nabled and us	d an <u>d used</u> ed; UxCTS pin	controlled by p	ort latches			
oit 7		e-up on Start bit								
		vill continue to s are on the follov -up enabled			upt generated o	n the falling ed	ge; bit cleared			
oit 6		RTx Loopback	Mode Select	bit						
		oopback mode k mode is disab	led							
oit 5	ABAUD: Auto	o-Baud Enable I	oit							
	before ot	aud rate measu her data; cleare e measurement	d in hardwar	e upon comple		ception of a Sy	nc field (0x55)			
	efer to Section	a 17. "UART" abling the UAR	(DS70188) i	n the <i>"dsPIC</i> 3		mily Referenc	e <i>Manual"</i> for			

2: This feature is only available for the 16x BRG mode (BRGH = 0).

REGISTER 2	0-1: UxMODE: UARTx MODE REGISTER (CONTINUED)
bit 4	URXINV: Receive Polarity Inversion bit 1 = UxRX Idle state is '0' 0 = UxPX Idle state is (1'
bit 3	0 = UxRX Idle state is '1' BRGH: High Baud Rate Enable bit
	 1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode) 0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)
bit 2-1	PDSEL<1:0>: Parity and Data Selection bits
	11 = 9-bit data, no parity 10 = 8-bit data, odd parity
	01 = 8-bit data, even parity
	00 = 8-bit data, no parity
bit 0	STSEL: Stop Bit Selection bit
	1 = Two Stop bits
	0 = One Stop bit

- Note 1: Refer to Section 17. "UART" (DS70188) in the "dsPIC33F/PIC24H Family Reference Manual" for information on enabling the UART module for receive or transmit operation.
 - 2: This feature is only available for the 16x BRG mode (BRGH = 0).



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REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0 HC	R/W-0	R-0
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN ⁽¹⁾	UTXBF
bit 15						Ľ

							扫一扫上面的二维码图案,	加我为朋
R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0	1
URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	
bit 7							bit 0	

Legend:	HC = Hardware Clearable bit		= Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15,13 UTXISEL<1:0>: Transmission Interrupt Mode Selection bits

- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR), and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)
- bit 14 UTXINV: Transmit Polarity Inversion bit If IREN = 0: 1 = UXTX Idle state is '0'

0 = UxTX Idle state is '1'

- If IREN = 1: 1 = IrDA[®] encoded UxTX Idle state is '1' 0 = IrDA encoded UxTX Idle state is '0' bit 12 Unimplemented: Read as '0' bit 11 UTXBRK: Transmit Break bit 1 = Send Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion 0 = Sync Break transmission disabled or completed bit 10 UTXEN: Transmit Enable bit⁽¹⁾ 1 = Transmit enabled, UxTX pin controlled by UARTx 0 = Transmit disabled, any pending transmission is aborted and the buffer is reset. UxTX pin controlled by port. bit 9 **UTXBF:** Transmit Buffer Full Status bit (read-only) 1 = Transmit buffer is full 0 = Transmit buffer is not full, at least one more character can be written
- bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only) 1 = Transmit Shift Register is empty and the transmit buffer is empty (the last transmission has completed)
 - 0 = Transmit Shift Register is not empty, a transmission is in progress or queued
 - **Note 1:** Refer to **Section 17. "UART"** (DS70188) in the *"dsPIC33F/PIC24H Family Reference Manual"* for information on enabling the UART module for transmit operation.



REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 7-6	URXISEL<1:0>: Receive Interrupt Mode Selection bits				
	 11 = Interrupt is set on the UxRSR transfer, making the receive buffer full (i.e., has 4 data the state of the line of the UxRSR transfer, making the receive buffer 3/4 full (i.e., has 3 data the state of the line of the				
bit 5	ADDEN: Address Character Detect bit (bit 8 of received data = 1)				
	 1 = Address Detect mode enabled. If 9-bit mode is not selected, this does not take effect. 0 = Address Detect mode disabled 				
bit 4	RIDLE: Receiver Idle bit (read-only)				
	1 = Receiver is Idle0 = Receiver is active				
bit 3	PERR: Parity Error Status bit (read-only)				
	 1 = Parity error has been detected for the current character (character at the top of the receive FIFO) 0 = Parity error has not been detected 				
bit 2	FERR: Framing Error Status bit (read-only)				
	 1 = Framing error has been detected for the current character (character at the top of the receive FIFO) 				
	0 = Framing error has not been detected				
bit 1	OERR: Receive Buffer Overrun Error Status bit (read/clear only)				
	 1 = Receive buffer has overflowed 0 = Receive buffer has not overflowed. Clearing a previously set OERR bit (1 → 0 transition) will reset the receiver buffer and the UxRSR to the empty state. 				
bit 0	URXDA: Receive Buffer Data Available bit (read-only)				
	 1 = Receive buffer has data, at least one more character can be read 0 = Receive buffer is empty 				

Note 1: Refer to **Section 17. "UART"** (DS70188) in the *"dsPIC33F/PIC24H Family Reference Manual"* for information on enabling the UART module for transmit operation.

21.0 ENHANCED CAN MODULE

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/ X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 15. "Enhanced Controller Area Network (ECAN™)" (DS70185) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

21.1 Overview

The Enhanced Controller Area Network (ECAN™ technology) module is a serial interface, useful for communicating with other CAN modules or microcontroller devices. This interface/protocol was designed to allow communications within noisy environments. The dsPIC33FJXXXMCX06A/X08A/X10A devices contain up to two ECAN modules.

The CAN module is a communication controller implementing the CAN 2.0 A/B protocol, as defined in the BOSCH specification. The module will support CAN 1.2, CAN 2.0A, CAN 2.0B Passive and CAN 2.0B Active versions of the protocol. The module implementation is a full CAN system. The CAN specification is not covered within this data sheet. The reader may refer to the BOSCH CAN specification for further details.

The module features are as follows:

- Implementation of the CAN protocol, CAN 1.2, CAN 2.0A and CAN 2.0B
- Standard and extended data frames
- 0-8 bytes data length
- Programmable bit rate up to 1 Mbit/sec
- Automatic response to remote transmission requests
- Up to eight transmit buffers with application specified prioritization and abort capability (each buffer may contain up to 8 bytes of data)
- Up to 32 receive buffers (each buffer may contain up to 8 bytes of data)
- Up to 16 full (standard/extended identifier)
 acceptance filters
- Three full acceptance filter masks
- DeviceNet[™] addressing support
- Programmable wake-up functionality with integrated low-pass filter
- Programmable Loopback mode supports self-test operation

- Signaling via interrupt capabilities
 receiver and transmitter error state
- Programmable clock source
- Programmable link to input captur for both CAN1 and CAN2) for time network synchronization
- Low-power Sleep and Idle mode

The CAN bus module consists of a protocol engine and message buffering/control. The CAN protocol engine handles all functions for receiving and transmitting messages on the CAN bus. Messages are transmitted by first loading the appropriate data registers. Status and errors can be checked by reading the appropriate registers. Any message detected on the CAN bus is checked for errors and then matched against filters to see if it should be received and stored in one of the receive registers.

21.2 Frame Types

The CAN module transmits various types of frames which include data messages, or remote transmission requests initiated by the user, as other frames that are automatically generated for control purposes. The following frame types are supported:

Standard Data Frame:

A standard data frame is generated by a node when the node wishes to transmit data. It includes an 11-bit Standard Identifier (SID), but not an 18-bit Extended Identifier (EID).

· Extended Data Frame:

An extended data frame is similar to a standard data frame, but includes an extended identifier as well.

Remote Frame:

It is possible for a destination node to request the data from the source. For this purpose, the destination node sends a remote frame with an identifier that matches the identifier of the required data frame. The appropriate data source node will then send a data frame as a response to this remote request.

· Error Frame:

An error frame is generated by any node that detects a bus error. An error frame consists of two fields: an error flag field and an error delimiter field.

Overload Frame:

An overload frame can be generated by a node as a result of two conditions. First, the node detects a dominant bit during interframe space which is an illegal condition. Second, due to internal conditions, the node is not yet able to start reception of the next message. A node may generate a maximum of 2 sequential overload frames to delay the start of the next message.

Interframe Space:

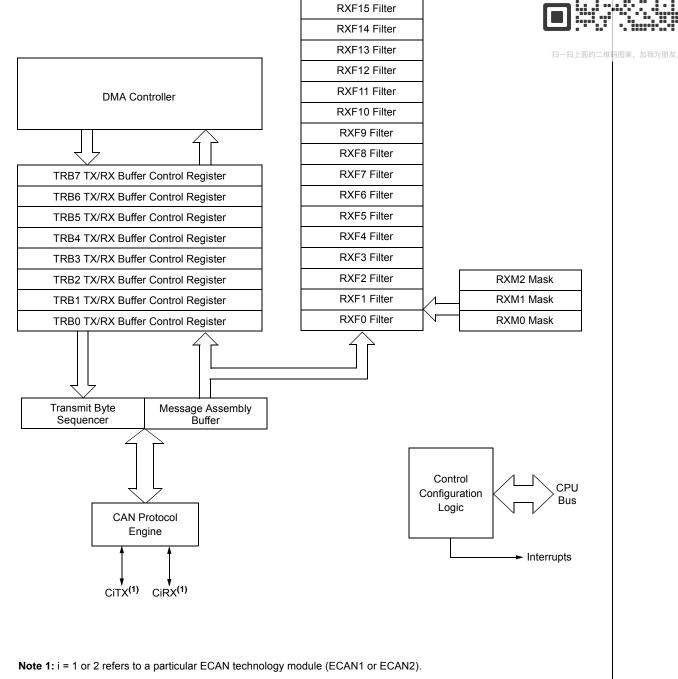
Interframe space separates a proceeding frame (of whatever type) from a following data or remote frame.



-扫上面的二维码图案

FIGURE 21-1: ECAN™ TECHNOLOGY MODULE BLOCK DIAGRAM





21.3 Modes of Operation

The CAN module can operate in one of several operation modes selected by the user. These modes include:

- Initialization Mode
- Disable Mode
- Normal Operation Mode
- Listen Only Mode
- Listen All Messages Mode
- · Loopback Mode

Modes are requested by setting the REQOP<2:0> bits (CiCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CiCTRL1<7:5>). The module will not change the mode and the OPMODE bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

21.3.1 INITIALIZATION MODE

In the Initialization mode, the module will not transmit or receive. The error counters are cleared and the interrupt flags remain unchanged. The programmer will have access to Configuration registers that are access restricted in other modes. The module will protect the user from accidentally violating the CAN protocol through programming errors. All registers which control the configuration of the module cannot be modified while the module is on-line. The CAN module will not be allowed to enter the Configuration mode while a transmission is taking place. The Configuration mode serves as a lock to protect the following registers:

- All Module Control Registers
- · Baud Rate and Interrupt Configuration Registers
- Bus Timing Registers
- Identifier Acceptance Filter Registers
- Identifier Acceptance Mask Registers

21.3.2 DISABLE MODE

In Disable mode, the module will not transmit or receive. The module has the ability to set the WAKIF bit due to bus activity, however, any pending interrupts will remain and the error counters will retain their value.

If the REQOP<2:0> bits (CiCTRL1<10:8>) = 001, the module will enter the Module Disable mode. If the module is active, the module will wait for 11 recessive bits on the CAN bus, detect that condition as an Idle bus, then accept the module disable command. When the OPMODE<2:0> bits (CiCTRL1<7:5>) = 001, that indicates whether the module successfully went into Module Disable mode. The I/O pins will revert to normal I/O function when the module is in the Module Disable mode.

The module can be programmed to filter function to the CiRX input line w the CPU is in Sleep mode. (CiCFG2<14>) enables or disables t



Note: Typically, if the CAN module is allowed to transmit in a particular mode of operation and a transmission is requested immediately after the CAN module has been placed in that mode of operation, the module waits for 11 consecutive recessive bits on the bus before starting transmission. If the user switches to Disable mode within this 11-bit period, then this transmission is aborted and the corresponding TXABT bit is set, and the TXREQ bit is cleared.

21.3.3 NORMAL OPERATION MODE

Normal Operation mode is selected when REQOP<2:0> = 000. In this mode, the module is activated and the I/O pins will assume the CAN bus functions. The module will transmit and receive CAN bus messages via the CiTX and CiRX pins.

21.3.4 LISTEN ONLY MODE

If the Listen Only mode is activated, the module on the CAN bus is passive. The transmitter buffers revert to the port I/O function. The receive pins remain inputs. For the receiver, no error flags or Acknowledge signals are sent. The error counters are deactivated in this state. The Listen Only mode can be used for detecting the baud rate on the CAN bus. To use this, it is necessary that there are at least two further nodes that communicate with each other.

21.3.5 LISTEN ALL MESSAGES MODE

The module can be set to ignore all errors and receive any message. The Listen All Messages mode is activated by setting REQOP<2:0> = 111. In this mode, the data which is in the message assembly buffer until the time an error occurred, is copied in the receive buffer and can be read via the CPU interface.

21.3.6 LOOPBACK MODE

If the Loopback mode is activated, the module will connect the internal transmit signal to the internal receive signal at the module boundary. The transmit and receive pins revert to their port I/O function.



REGISTER	21-1: CiCT	RL1: ECAN™	CONTROL	REGISTER 1			
U-0	U-0	R/W-0	R/W-0	r-0	R/W-1	R/W-0	
—	—	CSIDL	ABAT	—		REQOP<2:0>	
oit 15							bit -8
							<u>扫一扫上面的二维码</u> 图案,加我为
R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
-:+ 7	OPMODE<2:	0>		CANCAP	—	—	WIN
pit 7							bit 0
_egend:		r = Reserved	bit				
R = Readable	e bit	W = Writable	bit	U = Unimpler	nented bit, re	ad as '0'	
n = Value at	POR	'1' = Bit is se	t	'0' = Bit is cle		x = Bit is unkr	nown
oit 15-14	Unimpleme	ented: Read as	ʻ0'				
oit 13	CSIDL: Sto	op in Idle Mode b	bit				
		inue module ope			le mode		
		e module opera					
bit 12		rt All Pending Tr					
		all transmit buffe will clear this bit			borted		
bit 11	Reserved:	Do no use					
oit 10-8	REQOP<2:	0>: Request Op	peration Mode	e bits			
		isten All Messag					
		erved – do not us erved – do not us	-				
		Configuration mo					
		isten Only Mode	e				
		oopback mode. Disable mode					
		Normal Operation	n mode				
oit 7-5		2:0>: Operation					
		ule is in Listen A		node			
	110 = Rese		-				
	101 = Rese		ation mode				
		ule is in Configui ule is in Listen O					
		ule is in Loopbac	•				
		ule is in Disable					
		ule is in Normal		de			
bit 4	-	ented: Read as					
bit 3		CAN Message F		-			
		input capture ba CAN capture	ised on CAN	message receiv	e		
bit 2-1	Unimpleme	ented: Read as	0'				
oit O	WIN: SFR	Map Window Se	elect bit				
	1 = Use filte						
	0 = Use buf	fer window					



CiCTRL2: ECAN™ CONTROL REGISTER 2 **REGISTER 21-2:** U-0 U-0 U-0 U-0 U-0 U-0

bit 15							bit•8	
U-0	U-0	U-0	R-0	R-0	R-0	R-0	扫一扫上面的二维码图案, R-0	加我为朋友。
_	_	—			DNCNT<4:0>			
bit 7							bit 0	

U-0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

DNCNT<4:0>: DeviceNet[™] Filter Bit Number bits

10010-11111 = Invalid selection

10001 = Compare up to data byte 3, bit 6 with EID<17>

bit 4-0

00001 = Compare up to data byte 1, bit 7 with EID<0> 00000 = Do not compare data bytes

REGISTER 21-3: CiVEC: ECAN[™] INTERRUPT CODE REGISTER



CEGISTER .	21-3. Civi		ILENNUFI	CODE REGI	SIER		
U-0	U-0	U-0	R-0	R-0	R-0	R-0	R.O.
—	—	—			FILHIT<4:0>		
it 15							bit 8
							扫一扫上面的二约
U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
				ICODE<6:0	>		
pit 7							bit (
Legend:							
R = Readable	e bit	W = Writable		U = Unimple	emented bit, read	d as '0'	
n = Value at	POR	'1' = Bit is se	t	'0' = Bit is cl	eared	x = Bit is unl	known
oit 15-13	Unimplem	ented: Read as	ʻ0'				
oit 12-8	FILHIT<4:(D>: Filter Hit Num	ber bits				
	10000-11 01111 = F i	111 = Reserved					
	•						
	•						
	•						
	00001 = Fi 00000 = Fi						
oit 7	Unimplem	ented: Read as	ʻ0'				
oit 6-0	ICODE<6:0	0>: Interrupt Flag	Code bits				
	1000100 = 1000011 = 1000010 = 1000001 =	1111111 = Rese FIFO almost ful Receiver overfile Wake-up interru Error interrupt No interrupt	l interrupt ow interrupt				
		0111111 = Rese RB15 buffer Inte					
	•						
	•						
	0001000 = 0000111 = 0000110 = 0000100 = 0000100 = 0000011 =	RB9 buffer inter RB8 buffer inter TRB7 buffer inter TRB6 buffer inter TRB5 buffer inter TRB5 buffer inter TRB4 buffer inter TRB3 buffer inter TRB2 buffer inter	rrupt errupt errupt errupt errupt errupt errupt errupt				

REGISTER 21-4: CIFCTRL: ECAN™ FIFO CONTROL REGISTER



R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0			
	DMABS<2:0>		—	—	—	—			
it 15							bit-8		
							扫一扫上面的二维码图案		
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	—	—			FSA<4:0>				
pit 7							bit 0		
₋egend: R = Readabl	e hit	W = Writable b	hit	II = I Inimplei	mented bit, rea	d as '0'			
n = Value at		'1' = Bit is set		'0' = Bit is cle		x = Bit is u	nknown		
oit 15-13	DMABS<2:0	>: DMA Buffer S	Size bits						
	111 = Reser								
		ffers in DMA RA							
		ffers in DMA RAI ffers in DMA RAI							
		ffers in DMA RA							
		ers in DMA RAM							
		ers in DMA RAM							
		ers in DMA RAM							
oit 12-5	-	nted: Read as '0							
oit 4-0		FIFO Area Starts	with Buffer b	oits					
	11111 = RB31 buffer 11110 = RB30 buffer								
		30 buffer							
	•								
	•								
	00001 = T R	B1 buffer							
	00000 = TR								



REGISTER	21-5: CiFI	IFO: ECAN™ FIFO) STATU	IS REGISTER			
U-0	U-0	R-0	R-0	R-0	R-0	R-0	
_	_			FBF	°<5:0>		
bit 15							bi t -8
							扫一扫上面的二维
U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	_			FNR	B<5:0>		L:1.0
bit 7							bit 0
Legend:							
R = Readabl		W = Writable bit		U = Unimpler		ad as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
	011110 = • •	RB31 buffer RB30 buffer					
		TRB1 buffer TRB0 buffer					
bit 7-6		nented: Read as '0'					
bit 5-0	-	>: FIFO Next Read I	Buffer Poi	inter bits			
		RB31 buffer RB30 buffer					
	•						
		TRB1 buffer TRB0 buffer					



it 15 R/C-0 IVRIF	_	ТХВО	T)/D D		-		
R/C-0			TXBP	RXBP	TXWAR	RXWAR	EWARN
						L	bit 8
IVRIF	R/C-0	R/C-0	U-0	R/C-0	R/C-0	R/C-0	扫一扫上京的C细码图案,
	WAKIF	ERRIF	_	FIFOIF	RBOVIF	RBIF	TBIF
it 7							bit 0
egend:				C = Cle	earable bit		
R = Readable	bit	W = Writable I	bit	U = Unimple	mented bit, read	as '0'	
n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unl	known
it 15-14	Unimplemen	ted: Read as 'd)'				
it 13		mitter in Error S		bit			
		er is in Bus Off					
it 12		er is not in Bus mitter in Error S		ssiva hit			
11 12		er is in Bus Pas		SSIVE DIL			
	0 = Transmitte	er is not in Bus	Passive stat	e			
it 11		iver in Error Sta		ive bit			
		is in Bus Passiv					
:+ 40		is not in Bus Pa		ine hit			
it 10		nsmitter in Error er is in Error Wa		ing bit			
		er is not in Erro	•	ate			
it 9		eiver in Error S	-				
		is in Error Warr	•				
		is not in Error V	-				
it 8		nsmitter or Rec		-	g bit		
		er or receiver is er or receiver is					
it 7		Message Rece		•			
		request has occ		er eg er			
	•	request has not					
it 6		Wake-up Activit		lag bit			
		request has occ request has not					
it 5	-	-		ources in CilN	TF<13:8> regist	≏r)	
		request has occ			The region		
		request has not					
it 4	Unimplemen	ted: Read as 'o)'				
it 3	FIFOIF: FIFO	Almost Full Int	errupt Flag b	bit			
		request has occ					
		request has not		: h 14			
it 2		Buffer Overflow request has occ	•	ag bit			
	•	request has occ					
it 1	-	ffer Interrupt Fla					
		request has occ	•				
		request has not					
it O		fer Interrupt Fla					
		request has occ request has not					

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,加我为朋友。

REGISTER 21-7: CIINTE: ECAN™ INTERRUPT ENABLE REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	_	—	—	—
bit 15						

							扫一扫上面的二维码图
R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE
bit 7							bit 0

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is uni bit 15-8 Unimplemented: Read as '0' bit 7 IVRIE: Invalid Message Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request enabled 0 = Interrupt request enabled 0 = Interrupt request enabled bit 6 WAKIE: Bus Wake-up Activity Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request enabled 0 = Interrupt request enabled 0 = Interrupt request enabled bit 5 ERRIE: Error Interrupt Enable bit 1 = Interrupt request not enabled 0 = Interrupt request not enabled bit 4 Unimplemented: Read as '0' bit 3 FIFOIE: FIFO Almost Full Interrupt Enable bit 1 = Interrupt request not enabled 0 = Interrupt request not enabled bit 2 RBOVIE: RX Buffer Overflow Interrupt Enable bit 1 = Interrupt request not enabled 0 = Interrupt request not enabled bit 1 RBIE: RX Buffer Interrupt Enable bit 1 = Interrupt request not enabled 0 = Interrupt request not enabled bit 1 RBIE: RX Buffer Interrupt Enable bit	Legend:								
bit 15-8 Unimplemented: Read as '0' bit 7 IVRIE: Invalid Message Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request enabled bit 6 WAKIE: Bus Wake-up Activity Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request enabled 0 = Interrupt request enabled 0 = Interrupt request enabled bit 5 ERRIE: Error Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request enabled 0 = Interrupt request enabled 0 = Interrupt request enabled bit 5 ERRIE: Error Interrupt Enable bit 1 = Interrupt request not enabled 0 = Interrupt request enabled 0 = Interrupt request not enabled 0 = Interrupt request not enabled bit 4 Unimplemented: Read as '0' bit 3 FIFOIE: FIFO Almost Full Interrupt Enable bit 1 = Interrupt request not enabled 0 = Interrupt request not enabled bit 2 RBOVIE: RX Buffer Overflow Interrupt Enable bit 1 = Interrupt request not enabled 0 = Interrupt request not enabled bit 1 RBIE: RX Buffer Interrupt Enable bit 1 = Interrupt request not enabled 0 = Interrupt request enabled	R = Readab	le bit	W = Writable bit	U = Unimplemented bit	, read as '0'				
bit 7 IVRIE: Invalid Message Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request not enabled bit 6 WAKIE: Bus Wake-up Activity Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request enabled 0 = Interrupt request not enabled 0 = Interrupt request not enabled bit 5 ERRIE: Error Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request enabled 0 = Interrupt request enabled 0 = Interrupt request enabled bit 4 Unimplemented: Read as '0' bit 3 FIFOIE: FIFO Almost Full Interrupt Enable bit 1 = Interrupt request not enabled 0 = Interrupt request not enabled bit 4 Unimplemented: Read as '0' bit 5 EIFFOIE: FIFO Almost Full Interrupt Enable bit 1 = Interrupt request not enabled 0 = Interrupt request not enabled bit 2 RBOVIE: RX Buffer Overflow Interrupt Enable bit 1 = Interrupt request not enabled 0 = Interrupt request not enabled bit 1 RBIE: RX Buffer Interrupt Enable bit 1 = Interrupt request not enabled 0 = Interrupt request enabled	-n = Value a	t POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				
1 = Interrupt request enabled 0 = Interrupt request not enabled bit 6 WAKIE: Bus Wake-up Activity Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request not enabled bit 5 ERRIE: Error Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request not enabled bit 4 Unimplemented: Read as '0' bit 3 FIFOIE: FIFO Almost Full Interrupt Enable bit 1 = Interrupt request not enabled 0 bit 4 Unimplemented: Read as '0' bit 5 RBOVIE: FIFO Almost Full Interrupt Enable bit 1 = Interrupt request not enabled 0 bit 2 RBOVIE: RX Buffer Overflow Interrupt Enable bit 1 = Interrupt request not enabled 0 0 = Interrupt request not enabled 1	bit 15-8	Unimple	Unimplemented: Read as '0'						
1 = Interrupt request enabled 0 = Interrupt request not enabled bit 5 ERRIE: Error Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request enabled 0 = Interrupt request ont enabled bit 4 Unimplemented: Read as '0' bit 3 FIFOIE: FIFO Almost Full Interrupt Enable bit 1 = Interrupt request enabled 0 0 = Interrupt request not enabled bit 3 FIFOIE: FIFO Almost Full Interrupt Enable bit 1 = Interrupt request enabled 0 0 = Interrupt request not enabled 0 bit 2 RBOVIE: RX Buffer Overflow Interrupt Enable bit 1 = Interrupt request enabled 0 0 = Interrupt request not enabled 0 bit 1 RBIE: RX Buffer Interrupt Enable bit 1 = Interrupt request not enabled 1 bit 1 RBIE: RX Buffer Interrupt Enable bit 1 = Interrupt request enabled 1	bit 7	1 = Interr	upt request enabled	ble bit					
1 = Interrupt request enabled 0 = Interrupt request not enabled bit 4 Unimplemented: Read as '0' bit 3 FIFOIE: FIFO Almost Full Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request enabled bit 2 RBOVIE: RX Buffer Overflow Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request enabled bit 1 RBIE: RX Buffer Interrupt Enable bit 1 = Interrupt request not enabled 0 = Interrupt request not enabled bit 1 RBIE: RX Buffer Interrupt Enable bit 1 = Interrupt request not enabled 0 = Interrupt request not enabled	bit 6	1 = Interr	upt request enabled	pt Enable bit					
bit 3 FIFOIE: FIFO Almost Full Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request not enabled bit 2 RBOVIE: RX Buffer Overflow Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request enabled 0 = Interrupt request not enabled bit 1 RBIE: RX Buffer Interrupt Enable bit 1 = Interrupt request not enabled bit 1 RBIE: RX Buffer Interrupt Enable bit 1 = Interrupt request enabled	bit 5	1 = Interr	upt request enabled						
1 = Interrupt request enabled 0 = Interrupt request not enabled bit 2 RBOVIE: RX Buffer Overflow Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request not enabled 0 = Interrupt request not enabled bit 1 RBIE: RX Buffer Interrupt Enable bit 1 = Interrupt request not enabled bit 1 RBIE: RX Buffer Interrupt Enable bit 1 = Interrupt request enabled	bit 4	Unimple	mented: Read as '0'						
1 = Interrupt request enabled 0 = Interrupt request not enabled bit 1 RBIE: RX Buffer Interrupt Enable bit 1 = Interrupt request enabled	bit 3	1 = Interr	upt request enabled	nable bit					
1 = Interrupt request enabled	bit 2	1 = Interr	upt request enabled	ot Enable bit					
	bit 1	1 = Interr	upt request enabled						
bit 0 TBIE: TX Buffer Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request not enabled	bit 0	1 = Interr	upt request enabled						



REGISTER 21-8: CIEC: ECAN™ TRANSMIT/RECEIVE ERROR COUNT REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	
110			-	CNT<7:0>			
bit 15							bit-8
							<u> 扫一扫上面的二维码图案,</u> 加我为周
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			RERR	CNT<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit		t	U = Unimplemented bit, read as '0'				
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is u	nknown

bit 15-8 TERRCNT<7:0>: Transmit Error Count bits

bit 7-0 RERRCNT<7:0>: Receive Error Count bits



REGISTER 21-9: CiCFG1: ECAN™ BAUD RATE CONFIGURATION REGISTER 1

							10° 1
U-0	U-0	U-0	U-0	U-0	U-0	U-0	
—	—	—	—	—	—	_	
bit 15	-						
							担一担上
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W

<u>面的二维码</u> 图案,加我为J								
0		R/W-0						
	SJW<1:0> BRP<5:0>			SJW<				
bit 0						•		bit 7
bit 0								bit 7

Legend:								
R = Readat	ole bit	W = Writable bit	U = Unimplemented bit	, read as '0'				
-n = Value a	at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				
bit 15-8 Unimpler		mented: Read as '0'	nented: Read as '0'					
bit 7-6	SJW<1:0>: Synchronization Jump Width bits							
10 = L 01 = L		ngth is 4 x TQ ngth is 3 x TQ ngth is 2 x TQ ngth is 1 x TQ						
bit 5-0	BRP<5:0>: Baud Rate Prescaler bits							
	11 1111 = TQ = 2 x 64 x 1/FCAN							
	•							
	•							
	•							
	00 000	0 = TQ = 2 x 3 x 1/FCAN 1 = TQ = 2 x 2 x 1/FCAN 0 = TQ = 2 x 1 x 1/FCAN						



REGISTER 21-10: CiCFG2: ECAN[™] BAUD RATE CONFIGURATION REGISTER 2

U-0	R/W-x	U-0	U-0	U-0	R/W-x	R/W-x
—	WAKFIL	—	—	—		SEG2PH<2:0>
bit 15						

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	——扫上面的维码图案, R/W-x	7032
SEG2PHTS	SAM	:	SEG1PH<2:0>			PRSEG<2:0>		1
bit 7							bit 0	

Legend:							
R = Readabl	e bit	W = Writable bit	U = Unimplemented bit,	read as '0'			
-n = Value at	POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			
bit 15	Unimplem	ented: Read as '0'					
bit 14	WAKFIL: S	Select CAN bus Line Filter	for Wake-up bit				
		N bus line filter for wake-u	•				
	0 = CAN b ı	us line filter is not used for v	wake-up				
bit 13-11	Unimplem	ented: Read as '0'					
bit 10-8 SEG2PH<2:0>: Phase Buffer Segment 2 bits							
	111 = Len g	gth is 8 x TQ					
	000 = Len g	gth is 1 x TQ					
bit 7	SEG2PHTS	S: Phase Segment 2 Time	Select bit				
		programmable					
			mation Processing Time (IPT), whichever is greater			
bit 6	SAM: Sam	ple of the CAN bus Line bi	t				
		e is sampled three times at					
		e is sampled once at the sa					
bit 5-3		2:0>: Phase Buffer Segme	nt 1 bits				
		oth is 8 x TQ					
	-	pth is 1 x TQ					
bit 2-0		0>: Propagation Time Seg	iment bits				
		oth is 8 x TQ					
	000 = Leng	gth is 1 x TQ					

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REGISTER 21-11: CIFEN1: ECAN[™] ACCEPTANCE FILTER ENABLE REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	
FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	
bit 15							Ľ

							扫一扫上面的二维码	冯图案,
R/W-1								
FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0	
bit 7							bit 0	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **FLTENn:** Enable Filter n to Accept Messages bits

1 = Enable Filter n

0 = Disable Filter n



REGISTER 21-12: CIBUFPNT1: ECAN™ FILTER 0-3 BUFFER POINTER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	F3BP<	<3:0>			F2BP	<3:0>
bit 15						

_								扫一扫上面的二维码图案,	_ 加我为月
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
		F1BP<	<3:0>		F0BP<3:0>				
b	pit 7							bit 0]

Legend:				
R = Readabl	e bit	W = Writable bit	U = Unimplemented bit,	, read as '0'
-n = Value at	POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 15-12	1111 = F 1110 = F •	:0>: RX Buffer Written when Filter hits received in RX FIF Filter hits received in RX Buff	O buffer fer 14	
		Filter hits received in RX Buff		
bit 11-8	1111 = F 1110 = F	:0>: RX Buffer Written when Filter hits received in RX FIF Filter hits received in RX Buff Filter hits received in RX Buff	O buffer fer 14	
bit 7-4	F1BP<3	:0>: RX Buffer Written when Filter hits received in RX FIF Filter hits received in RX Buff	Filter 1 Hits bits O buffer	
	•			
		Filter hits received in RX Buff Filter hits received in RX Buff		
bit 3-0	1111 = F 1110 = F • • • •	:0>: RX Buffer Written when Filter hits received in RX FIF Filter hits received in RX Buff Filter hits received in RX Buff Filter hits received in RX Buff	O buffer Fer 14	



REGISTER 21-13: CIBUFPNT2: ECAN™ FILTER 4-7 BUFFER POINTER REGISTER

F7BP<3:0> F6BP<3:0> bit 15 Im-Image R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 F5BP<3:0> F4BP<3:0>	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
bit 15 Image: State of the second of the	N/W-0		-	N/W-U	N/W-0		-	
RW-0	15	1101	0.0			1021	0.0	- LEJ :: _{bit} .8
RW-0								
bit 7	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15-12 F7BP<3:0>: RX Buffer Written when Filter 7 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 6 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14		F5BP<	3:0>			F4BF	P<3:0>	
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15-12 F7BP<3:0>: RX Buffer Written when Filter 7 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 0 bit 7-4 F5BP-3:0>: RX Buffer Written when Filter 5 Hits bits 1111 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 0 bit 3-0 F4BP-3:0>: RX Buffer Written when Filter 4 Hits bits 1111 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 14 . . <td>7</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>bit 0</td>	7							bit 0
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' .n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15-12 F7BP<3:0>: RX Buffer Written when Filter 7 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 14 </td <td>nend:</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>	nend:							
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15-12 F7BP-3:00: RX Buffer Written when Filter 7 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 0 bit 11-8 F6BP-3:00: RX Buffer Written when Filter 6 Hits bits 1111 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 0 bit 3-0 F4BP-3:00: RX Buffer Written when Filter 4 Hits bits 1111 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1<	-		W = Writable	bit	U = Unimpler	nented bit, read	d as '0'	
bit 15-12 F7BP<3:0>: RX Buffer Written when Filter 7 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 0 F6BP<3:0>: RX Buffer Written when Filter 6 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 0 bit 7-4 F5BP<3:0>: RX Buffer Written when Filter 5 Hits bits 1111 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 1110 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14					-			known
<pre>1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14 </pre>								
 bit 11-8 F6BP<3:0>: RX Buffer Written when Filter 6 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14 0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 0 bit 7-4 F5BP<3:0>: RX Buffer Written when Filter 5 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 14 Bit 3-0 F4BP<3:0>: RX Buffer Written when Filter 4 Hits bits 1111 = Filter hits received in RX Buffer 14 	1	111 = Filter h	nits received in	RX FIFO bu	uffer			
 bit 11-8 F6BP<3:0>: RX Buffer Written when Filter 6 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14 0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 0 bit 7-4 F5BP<3:0>: RX Buffer Written when Filter 5 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14 0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 14 Bit 3-0 F4BP<3:0>: RX Buffer Written when Filter 4 Hits bits 1111 = Filter hits received in RX Buffer 14 	•							
 bit 11-8 F6BP<3:0>: RX Buffer Written when Filter 6 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14 0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 0 bit 7-4 F5BP<3:0>: RX Buffer Written when Filter 5 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0001 = Filter hits received in RX Buffer 1 0011 = Filter hits received in RX Buffer 1 	•							
<pre>1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14 bit 7-4 F5BP<3:0>: RX Buffer Viriten when Filter 5 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14</pre>	-							
 bit 7-4 F5BP<3:0>: RX Buffer Written when Filter 5 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14 . . 0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 0 bit 3-0 F4BP<3:0>: RX Buffer Written when Filter 4 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14 . 	1	111 = Filter h	nits received in	RX FIFO bu	uffer			
 bit 7-4 F5BP<3:0>: RX Buffer Written when Filter 5 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14 . . 0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 0 bit 3-0 F4BP<3:0>: RX Buffer Written when Filter 4 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14 	•							
<pre>1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14</pre>								
<pre>0000 = Filter hits received in RX Buffer 0 bit 3-0 F4BP<3:0>: RX Buffer Written when Filter 4 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14</pre>	1	111 = Filter h	nits received in	RX FIFO bu	uffer			
<pre>0000 = Filter hits received in RX Buffer 0 bit 3-0 F4BP<3:0>: RX Buffer Written when Filter 4 Hits bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14</pre>	•							
 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14 . 								
• • •	1	111 = Filter ł	nits received in	RX FIFO bu	uffer			
• 0001 = Filter hits received in RX Buffer 1	•		ins received in	I KA DUIIEF 1	4			
	•		aite received in					
0000 = Filter hits received in RX Buffer 0	-							



REGISTER 21-14: CIBUFPNT3: ECAN™ FILTER 8-11 BUFFER POINTER REGISTER

							0_0_000
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W- 0
		F11BP	<3:0>			F10BF	P<3:0>
ſ	bit 15						

							扫一扫上面的二维码图案,	,加我为
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	F9BP<	<3:0>		F8BP<3:0>				
bit 7							bit 0	

Legend:				
R = Readab	le bit	W = Writable bit	U = Unimplemented bit,	, read as '0'
-n = Value a	t POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 15-12	1111 = F	3:0>: RX Buffer Written wher Filter hits received in RX FIF(Filter hits received in RX Buff	O buffer	
		Filter hits received in RX Buff		
bit 11-8	F10BP<: 1111 = F	3:0>: RX Buffer Written when Filter hits received in RX FIF(Filter hits received in RX Buff	n Filter 10 Hits bits D buffer	
		Filter hits received in RX Buff		
bit 7-4	1111 = F	:0>: RX Buffer Written when Filter hits received in RX FIFC Filter hits received in RX Buff	O buffer	
		Filter hits received in RX Buff		
bit 3-0	1111 = F	:0>: RX Buffer Written when Filter hits received in RX FIF(Filter hits received in RX Buff	O buffer	
		Filter hits received in RX Buff Filter hits received in RX Buff		



REGISTER 21-15: CIBUFPNT4: ECAN™ FILTER 12-15 BUFFER POINTER REGISTER

		UFPNT4: ECAN					
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
bit 15	F15	BP<3:0>			F14B	P<3:0>	
							Dit o
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	<u>— 扫一扫上面的二维码</u> 图 R/W-0
1011 0	-	BP<3:0>	1011 0		-	P<3:0>	
bit 7							bit 0
Legend:							
R = Readabl	e bit	W = Writable	bit	U = Unimpler	mented bit, rea	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown
bit 15-12		0>: RX Buffer Wri ter hits received in					
		ter hits received in					
	•						
	•						
	•						
		ter hits received in ter hits received in					
bit 11-8		0>: RX Buffer Wri					
		ter hits received in					
	1110 = Fil	ter hits received in	n RX Buffer 1	4			
	•						
	•						
	0001 = Fi l	ter hits received in	n RX Buffer 1				
		ter hits received in					
bit 7-4		0>: RX Buffer Wri					
		ter hits received in ter hits received in					
	•			4			
	•						
	•						
		ter hits received in					
		ter hits received in					
bit 3-0		0>: RX Buffer Wri					
		ter hits received in ter hits received in					
	• •			т			
	•						
	•						
		ter hits received in					
	0000 = Fil	ter hits received in	n RX Buffer 0)			



REGISTER 21-16: CIRXFnSID: ECAN™ ACCEPTANCE FILTER n STANDARD IDENTIFIER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-X	R/04-x					
			SID<	:10:3>		ſ						
bit 15	SID<10:3> 15 R/W-x SID<10:0	bit 8										
						2-	一扫上面的二维码图案					
R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x					
	SID<2:0>			EXIDE	—	EID<'	17:16>					
bit 7							bit 0					
Legend:												
				•								
-n = Value a	t POR	'1' = Bit is set	et '0' = Bit is cleared			x = Bit is unkı	nown					
bit 15-5	SID<10:0>: S	standard Identif	ier bits									
	-			of to match filte	r							
bit 4	Unimplemented: Read as '0'											
bit 3												
			ith standard io	lentifier addres	ses							
	/											
	0											
bit 2	-											
bit 1-0												
	1 = Message address bit, EIDx, must be '1' to match filter											
	o N/			al 1 1. I. C.								

REGISTER 21-17: CIRXFnEID: ECAN™ ACCEPTANCE FILTER n EXTENDED IDENTIFIER (n = 0, 1, ..., 15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			EID	<15:8>			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			EID)<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable	bit	U = Unimplen	nented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 EID<15:0>: Extended Identifier bits

1 = Message address bit, EIDx, must be '1' to match filter

0 = Message address bit, EIDx, must be '0' to match filter



REGISTER 21-18: CiFMSKSEL1: ECAN™ FILTER 7-0 MASK SELECTION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	EW D
	SK<1:0>	F6MS	K<1:0>	F5M	SK<1:0>	F4MS	K<10>
bit 15							• bit 8
						DAMO	日一扫上面的二维
R/W-0	R/W-0 SK<1:0>	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SK<1:0>	F21015	K<1:0>	F IM	SK<1:0>	FUMS	K<1:0>
bit 7							bit C
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimple	mented bit, rea	d as '0'	
-n = Value at	POR	'1' = Bit is se	t	'0' = Bit is cle		x = Bit is unk	nown
bit 15-14	11 = Reserv 10 = Accept 01 = Accept	>: Mask Sourc ed; do not use ance Mask 2 re ance Mask 1 re	gisters contai gisters contai	in mask in mask			
bit 13-12	F6MSK<1:0 11 = Reserv 10 = Accept 01 = Accept	ance Mask 0 re >: Mask Sourc ed; do not use ance Mask 2 re ance Mask 1 re ance Mask 0 re	e for Filter 6 t gisters contai gisters contai	bit in mask in mask			
bit 11-10	11 = Reserv 10 = Accept 01 = Accept	>: Mask Sourc ed; do not use ance Mask 2 re ance Mask 1 re ance Mask 0 re	gisters contai gisters contai	in mask in mask			
bit 9-8	F4MSK<1:0 11 = Reserv 10 = Accept 01 = Accept	>: Mask Sourc ed; do not use ance Mask 2 re ance Mask 1 re ance Mask 0 re	e for Filter 4 t gisters contai gisters contai	bit in mask in mask			
bit 7-6	F3MSK<1:0 11 = Reserv 10 = Accept 01 = Accept	>: Mask Sourc ed; do not use ance Mask 2 re ance Mask 1 re ance Mask 0 re	e for Filter 3 b gisters contai gisters contai	bit in mask in mask			
bit 5-4	F2MSK<1:0 11 = Reserv 10 = Accept 01 = Accept	>: Mask Sourc ed; do not use ance Mask 2 re ance Mask 1 re ance Mask 0 re	e for Filter 2 b gisters contai gisters contai	bit in mask in mask			
bit 3-2	F1MSK<1:0 11 = Reserv 10 = Accept 01 = Accept	>: Mask Sourc ed; do not use ance Mask 2 re ance Mask 1 re ance Mask 0 re	e for Filter 1 t gisters contai gisters contai	bit in mask in mask			
bit 1-0	F0MSK<1:0 11 = Reserv 10 = Accept 01 = Accept	>: Mask Sourc ed; do not use ance Mask 2 re ance Mask 1 re ance Mask 0 re	e for Filter 0 t gisters contai gisters contai	bit in mask in mask			



REGISTER 21-19: CiFMSKSEL2: ECAN™ FILTER 15-8 MASK SELECTION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0 R/W-0
F15MSK<1	:0>	F14MS	K<1:0>	F13MS	SK<1:0>	F12 //SM < 0>
bit 15						bit S

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	扫一扫上南的环维码图案,	加我为朋友
F11MSK<1:0>		F10MSK<1:0>		F9MSK<1:0>		F81	/ISK<1:0>	
bit 7							bit 0	

Legend:	h:t	M = M/ritable bit	II — I loineal an an tait bit	read as '0'				
R = Readable		W = Writable bit	U = Unimplemented bit,					
-n = Value at P	UK	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				
bit 15-14	F15MSK-1.0	>: Mask Source for Filte	r 15 hit					
	11 = Reserve							
		nce Mask 2 registers co	ntain mask					
		nce Mask 1 registers co						
		nce Mask 0 registers co						
bit 13-12		>: Mask Source for Filte						
511 15-12	11 = Reserve							
		nce Mask 2 registers co	ntain mask					
		nce Mask 1 registers co						
		nce Mask 0 registers co						
bit 11-10	-	>: Mask Source for Filte						
	11 = Reserve							
	10 = Acceptance Mask 2 registers contain mask							
		nce Mask 1 registers co						
		nce Mask 0 registers co						
bit 9-8	-	>: Mask Source for Filte						
	11 = Reserve							
		nce Mask 2 registers co	ntain mask					
		nce Mask 1 registers co						
		nce Mask 0 registers co						
bit 7-6	F11MSK<1:0	>: Mask Source for Filte	r 11 bit					
	11 = Reserve	d; do not use						
	10 = Accepta	nce Mask 2 registers co	ntain mask					
	01 = Accepta	nce Mask 1 registers co	ntain mask					
	00 = Accepta	nce Mask 0 registers co	ntain mask					
bit 5-4	F10MSK<1:0	>: Mask Source for Filte	r 10 bit					
	11 = Reserve	d; do not use						
	10 = Accepta	nce Mask 2 registers co	ntain mask					
		nce Mask 1 registers co						
	00 = Accepta	nce Mask 0 registers co	ntain mask					
bit 3-2	F9MSK<1:0>	: Mask Source for Filter	9 bit					
	11 = Reserve	-						
	-	nce Mask 2 registers co						
		nce Mask 1 registers co						
		nce Mask 0 registers co						
bit 1-0		: Mask Source for Filter	8 bit					
	11 = Reserve	,						
		nce Mask 2 registers co						
		nce Mask 1 registers co						
	00 = Accepta	nce Mask 0 registers co	ntain mask					



REGISTER 21-20: CIRXMnSID: ECAN™ ACCEPTANCE FILTER MASK n STANDARD IDE

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	E74-X
			SID	<10:3>			
bit 15							bit 8
							扫一扫上面的二
R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
	SID<2:0>			MIDE		EID<	:17:16>
bit 7							bit (
Legend:							
R = Readab	le bit	W = Writable b	it	U = Unimpler	nented bit, read	d as '0'	
-n = Value a	n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is ur						nown
bit 15-5		Standard Identifi					
		oit, SIDx, in filter	•				
1.11 A		, is a don't care i		barison			
bit 4	•	nted: Read as '0					
bit 3		ifier Receive Mo					
		nly message type ither standard or					XIDE bit in filte
		Filter SID) = (Mes					
bit 2		nted: Read as '0			, (,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	
bit 1-0	•	Extended Identi					
		bit, EIDx, in filter					
		k, is a don't care					
			-				

REGISTER 21-21: CIRXMnEID: ECAN™ ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			EID	<15:8>			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			EID	<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit		bit	U = Unimplemented bit, read as '0'				
-n = Value at P	OR	'1' = Bit is set	it is set '0' = Bit is cleared x = Bit is u		x = Bit is unkr	nown	

bit 15-0 EID<15:0>: Extended Identifier bits

1 = Include bit, EIDx, in filter comparison

0 = Bit, EIDx, is a don't care in filter comparison



REGISTER 21-22: CIRXFUL1: ECAN™ RECEIVE BUFFER FULL REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL
bit 15						

								加我为周
R/C-0								
RXFUL7	RXFUL6	RXFUL5	RXFUL4	RXFUL3	RXFUL2	RXFUL1	RXFUL0	
bit 7							bit 0	

Legend:	C= Clearable bit				
R = Readable bit	W = Writable bit	W = Writable bit U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-0

RXFUL15:RXFUL0: Receive Buffer n Full bits

1 = Buffer is full (set by module)

0 = Buffer is empty (clear by application software)

REGISTER 21-23: CIRXFUL2: ECAN[™] RECEIVE BUFFER FULL REGISTER 2

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXFUL31 | RXFUL30 | RXFUL29 | RXFUL28 | RXFUL27 | RXFUL26 | RXFUL25 | RXFUL24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXFUL23 | RXFUL22 | RXFUL21 | RXFUL20 | RXFUL19 | RXFUL18 | RXFUL17 | RXFUL16 |
| bit 7 | | | | | | | bit 0 |

Legend:		C= Clearable bit				
R = Readable bit	W = Writable bit	W = Writable bit U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 15-0 **RXFUL31:RXFUL16:** Receive Buffer n Full bits

1 = Buffer is full (set by module)

0 = Buffer is empty (clear by application software)



REGISTER 21-24: CIRXOVF1: ECAN™ RECEIVE BUFFER OVERFLOW REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	
RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	F
bit 15							

							扫一扫上面的二维码	图案
R/C-0								
RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	
bit 7							bit 0	

Legend: C= Clearable bit					
R = Readable bit	W = Writable bit	W = Writable bit U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-0 RXOVF15:RXOVF0: Receive Buffer n Overflow bits

1 = Module pointed a write to a full buffer (set by module)

0 = Overflow is cleared (clear by application software)

REGISTER 21-25: CIRXOVF2: ECAN™ RECEIVE BUFFER OVERFLOW REGISTER 2

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 |
| bit 7 | | | | | | | bit 0 |

Legend:		C= Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit	t, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 RXOVF31:RXOVF16: Receive Buffer n Overflow bits

1 = Module pointed a write to a full buffer (set by module)

0 = Overflow is cleared (clear by application software)



REGISTER 21-26: CiTRmnCON: ECAN™ TX/RX BUFFER mn CONTROL REGISTER (m = 0,2

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0
TXENn	TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnFF
bit 15						Ľ

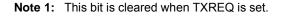
R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	<u>3一扫上面的二维码图案,</u> R/W-0
TXENm	TXABTm ⁽¹⁾	TXLARBm ⁽¹⁾	TXERRm ⁽¹⁾	TXREQm	RTRENm	TXmP	RI<1:0>
bit 7			L				bit 0

Legend:				
R = Readal	ole bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR		'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 15-8	See Defi	nition for Bits 7-0, Controls	Buffer n	
bit 7	TXENm:	TX/RX Buffer Selection bit		
	1 = Buffe	er TRBn is a transmit buffer		
	0 = Buffe	er TRBn is a receive buffer		
bit 6	TXABTn	1: Message Aborted bit ⁽¹⁾		
		age was aborted		
		sage completed transmission		
bit 5	TXLARB	m: Message Lost Arbitration	n bit ⁽¹⁾	
		age lost arbitration while beir	•	
		age did not lose arbitration w	•	
bit 4	TXERRn	 Error Detected During Tra 	nsmission bit ⁽¹⁾	
		s error occurred while the me	U	
	0 = A bu	s error did not occur while the	e message was being sent	
bit 3		n: Message Send Request b		
				natically clear when the message
			o '0' while set will request a m	essage abort.
bit 2	RTRENn	n: Auto-Remote Transmit Ena	able bit	
	1 = Whe	n a remote transmit is receive	ed, TXREQ will be set	

0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0 **TXmPRI<1:0>:** Message Transmission Priority bits 11 = Highest message priority

- 10 = High intermediate message priority
- 01 = Low intermediate message priority
- 00 = Lowest message priority





Note: The buffers, SID, EID, DLC, Data Field and Receive Status registers, are located in DMA RA

REGISTER 21-27: CiTRBnSID: ECAN™ BUFFER n STANDARD IDENTIFIER (n = 0, 1, ...,

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	
_	—	_			SID<10:6>		扫一扫上面的二维码图案,加我为朋友。
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID<5:0>							IDE
bit 7							bit 0

Legend:

Legenu.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13	Unimplemented: Read as '0'
bit 12-2	SID<10:0>: Standard Identifier bits
bit 1	SRR: Substitute Remote Request bit
	1 = Message will request remote transmission0 = Normal message
bit 0	IDE: Extended Identifier bit
	1 = Message will transmit extended identifier0 = Message will transmit standard identifier

REGISTER 21-28: CiTRBnEID: ECAN[™] BUFFER n EXTENDED IDENTIFIER (n = 0, 1, ..., 31)

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
_	_		_		EID<'	17:14>	
bit 15		· · · ·					bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			EID	<13:6>			
bit 7							bit 0
Legend:							
R = Readable b	oit	W = Writable bit	t	U = Unimpler	nented bit, read	l as '0'	

'0' = Bit is cleared

bit 15-12 Unimplemented: Read as '0'

bit 11-0 EID<17:6>: Extended Identifier bits

'1' = Bit is set

-n = Value at POR

x = Bit is unknown



REGISTER 21-29: CITRBnDLC: ECAN™ BUFFER n DATA LENGTH CONTROL (n = 0

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID5	EID4	EID3	EID2	EID1	EID0	RTR
bit 15						

								加我为月
U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
—	—	_	RB0	DLC3	DLC2	DLC1	DLC0	
bit 7							bit 0	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10	EID<5:0>: Extended Identifier bits
bit 9	RTR: Remote Transmission Request bit
	 1 = Message will request remote transmission 0 = Normal message
bit 8	RB1: Reserved Bit 1
	User must set this bit to '0' per CAN protocol.
bit 7-5	Unimplemented: Read as '0'
bit 4	RB0: Reserved Bit 0
	User must set this bit to '0' per CAN protocol.
bit 3-0	DLC<3:0>: Data Length Code bits

REGISTER 21-30: CiTRBnDm: ECAN™ BUFFER n DATA FIELD BYTE m (n = 0, 1, ..., 31; m = 0, 1, ..., 7)⁽¹⁾

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
TRBnDm<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	t, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **TRnDm<7:0>:** Data Field Buffer 'n' Byte 'm' bits

Note 1: The Most Significant Byte contains byte (m + 1) of the buffer.



REGISTER 21-31: CITRBnSTAT: ECAN™ RECEIVE BUFFER n STATUS (n = 0, 1, ..., 31)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
—	—	_	FILHIT<4:0>			
bit 15						

0-0	U-0							
_	_	_		—	_	_		
bit 0				·				bit 7
		_	_	—	-	-	—	bit 7

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 Unimplemented: Read as '0'

bit 12-8 **FILHIT<4:0>:** Filter Hit Code bits (only written by module for receive buffers, unused for transmit buffers) Encodes number of filter that resulted in writing this buffer.

bit 7-0 Unimplemented: Read as '0'

22.0 10-BIT/12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 16. "Analog-to-Digital Converter (ADC)" (DS70183) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33FJXXXMCX06A/X08A/X10A devices have up to 32 ADC input channels. These devices also have up to 2 ADC modules (ADCx, where 'x' = 1 or 2), each with its own set of Special Function Registers.

The AD12B bit (ADxCON1<10>) allows each of the ADC modules to be configured by the user as either a 10-bit, 4-sample/hold ADC (default configuration) or a 12-bit, 1-sample/hold ADC.

Note: The ADC module needs to be disabled before modifying the AD12B bit.

22.1 Key Features

The 10-bit ADC configuration has the following key features:

- Successive Approximation (SAR) conversion
- Conversion speeds of up to 1.1 Msps
- · Up to 32 analog input pins
- External voltage reference input pins
- Simultaneous sampling of up to four analog input pins
- Automatic Channel Scan mode
- Selectable conversion trigger source
- Selectable Buffer Fill modes
- Four result alignment options (signed/unsigned, fractional/integer)
- · Operation during CPU Sleep and Idle modes

The 12-bit ADC configuration supports all the above features, except:

- In the 12-bit configuration, conversion speeds of up to 500 ksps are supported.
- There is only 1 sample/hold amplifier in the 12-bit configuration, so simultaneous sampling of multiple channels is not supported.

Depending on the particular device pine have up to 32 analog input pins, through AN31. In addition, there are pins for external voltage reference voltage reference inputs may be analog input pins. The actual number of an pins and external voltage reference input cor will depend on the specific device.



A block diagram of the ADC is shown in Figure 22-1.

22.2 ADC Initialization

The following configuration steps should be performed.

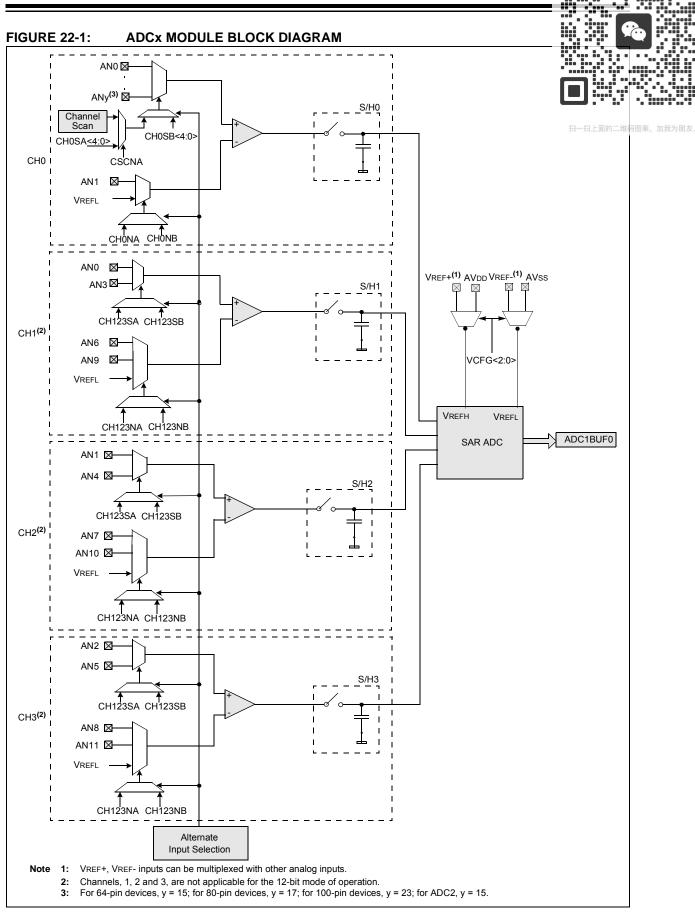
- 1. Configure the ADC module:
 - a) Select port pins as analog inputs (ADxPCFGH<15:0> or ADxPCFGL<15:0>)
 - b) Select voltage reference source to match expected range on analog inputs (ADxCON2<15:13>)
 - c) Select the analog conversion clock to match desired data rate with processor clock (ADxCON3<7:0>)
 - d) Determine how many S/H channels will be used (ADxCON2<9:8> and ADxPCFGH<15:0> or ADxPCFGL<15:0>)
 - e) Select the appropriate sample/conversion sequence (ADxCON1<7:5> and ADxCON3<12:8>)
 - f) Select how conversion results are presented in the buffer (ADxCON1<9:8>)
 - g) Turn on ADC module (ADxCON1<15>)
- 2. Configure ADC interrupt (if required):
 - a) Clear the ADxIF bit
 - b) Select ADC interrupt priority

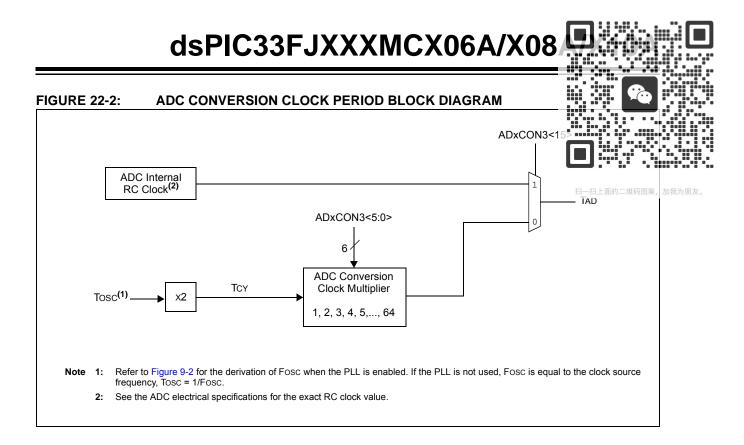
22.3 ADC and DMA

If more than one conversion result needs to be buffered before triggering an interrupt, DMA data transfers can be used. Both ADC1 and ADC2 can trigger a DMA data transfer. If ADC1 or ADC2 is selected as the DMA IRQ source, a DMA transfer occurs when the AD1IF or AD2IF bit gets set as a result of an ADC1 or ADC2 sample conversion sequence.

The SMPI<3:0> bits (ADxCON2<5:2>) are used to select how often the DMA RAM Buffer Pointer is incremented.

The ADDMABM bit (ADxCON1<12>) determines how the conversion results are filled in the DMA RAM buffer area being used for ADC. If this bit is set, DMA buffers are written in the order of conversion. The module will provide an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer. If the ADDMABM bit is cleared, then DMA buffers are written in Scatter/Gather mode. The module will provide a scatter/gather address to the DMA channel, based on the index of the analog input and the size of the DMA buffer.







22.4 ADC Helpful Tips

- 1. The SMPI<3:0> (AD1CON2<5:2>) control bits:
 - a) Determine when the ADC interrupt flag is set and an interrupt is generated if enabled.
 - b) When the CSCNA bit (AD1CON2<10>) is set to '1', determines when the ADC analog scan channel list defined in the AD1CSSL/ AD1CSSH registers starts over from the beginning.
 - c) On devices without a DMA peripheral, determines when ADC result buffer pointer to ADC1BUF0-ADC1BUFF, gets reset back to the beginning at ADC1BUF0.
- On devices without a DMA module, the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF regardless of which analog inputs are being used subject to the SMPI<3:0> bits (AD1CON2<5:2>) and the condition described in 1c above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
- On devices with a DMA module, the ADC module has only 1 ADC result buffer, (i.e., ADC1BUF0), per ADC peripheral and the ADC conversion result must be read either by the CPU or DMA controller before the next ADC conversion is complete to avoid overwriting the previous value.
- 4. The DONE bit (AD1CON1<0>) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in manual sample mode, particularly where the users code is setting the SAMP bit (AD1CON1<1>), the DONE bit should also be cleared by the user application just before setting the SAMP bit.
- 5. On devices with two ADC modules, the ADCxPCFG registers for both ADC modules must be set to a logic '1' to configure a target I/O pin as a digital I/O pin. Failure to do so means that any alternate digital input function will always see only a logic '0' as the digital input buffer is held in Disable mode.

22.5 ADC Resources

Many useful resources related to ADC an the main product page of the Microchip w devices listed in this data sheet. This p which can be accessed using this link, latest updates and additional information.



22.5.1 KEY RESOURCES

- Section 16. "Analog-to-Digital Converter (ADC)" (DS70183)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools



REGISTER 22-1: ADxCON1: ADCx CONTROL REGISTER 1 (where x = 1 or 2)

R/W-0 U-0 R/W-0 R/W-0 U-0 R/W-0 R/W-0			
	R/W-0 R/W-0 U-0 R/W-0	U-0	R/W-0
ADOM — ADOL ADDMABIN — AD12B	ADSIDL ADDMABM — AD12B	_	FORM<###
bit 15			

							<u> 扫上面的维码图案,</u> 加
R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0,	R/C-0,
						HC,HS	HC, HS
	SSRC<2:0>			SIMSAM	ASAM	SAMP	DONE
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	C= Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	ADON: ADC Operating Mode bit 1 = ADC module is operating 0 = ADC is off
bit 14	Unimplemented: Read as '0'
bit 13	ADSIDL: Stop in Idle Mode bit
Sit 10	 1 = Discontinue module operation when device enters Idle mode 0 = Continue module operation in Idle mode
bit 12	ADDMABM: DMA Buffer Build Mode bit
	 1 = DMA buffers are written in the order of conversion. The module will provide an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer 0 = DMA buffers are written in Scatter/Gather mode. The module will provide a scatter/gather address to the DMA channel, based on the index of the analog input and the size of the DMA buffer
bit 11	Unimplemented: Read as '0'
bit 10	AD12B: 10-Bit or 12-Bit Operation Mode bit
	 1 = 12-bit, 1-channel ADC operation 0 = 10-bit, 4-channel ADC operation
bit 9-8	FORM<1:0>: Data Output Format bits
	For 10-Bit Operation: 11 = Signed fractional (Dout = sddd dddd dd00 0000, where s = .NOT.d<9>) 10 = Fractional (Dout = dddd dddd dd00 0000)
	01 = Signed integer (Dout = ssss sssd dddd dddd, where s = .NOT.d<9>) 00 = Integer (Dout = 0000 00dd dddd dddd)
	For 12-Bit Operation: 11 = Signed fractional (Dout = sddd dddd dddd 0000, where s = .NOT.d<11>) 10 = Fractional (Dout = dddd dddd dddd 0000)
	01 = Signed Integer (DOUT = ssss sddd dddd dddd, where s = .NOT.d<11>) 00 = Integer (DOUT = 0000 dddd dddd dddd)
bit 7-5	SSRC<2:0>: Sample Clock Source Select bits
	 111 = Internal counter ends sampling and starts conversion (auto-convert) 110 = Reserved 101 = Reserved
	 101 = Reserved 100 = GP timer (Timer5 for ADC1, Timer3 for ADC2) compare ends sampling and starts conversion 011 = MPWM interval ends sampling and starts conversion 010 = GP timer (Timer3 for ADC1, Timer5 for ADC2) compare ends sampling and starts conversion 001 = Active transition on INT0 pin ends sampling and starts conversion 000 = Clearing sample bit ends sampling and starts conversion
bit 4	Unimplemented: Read as '0'



REGISTER 22-1: ADxCON1: ADCx CONTROL REGISTER 1 (where x = 1 or 2) (CONTIN

bit 3	SIMSAM: Simultaneous Sample Select bit (only applicable when CHPS<1:0> = 01 or 1×
	 When AD12B = 1, SIMSAM is: U-0, Unimplemented, Read as '0'. 1 = Samples CH0, CH1, CH2, CH3 simultaneously (when CHPS<1:0> = 1x); or sample channels individually in sequence 0 = Samples multiple channels individually in sequence
bit 2	ASAM: ADC Sample Auto-Start bit
	 1 = Sampling begins immediately after last conversion. SAMP bit is auto-set. 0 = Sampling begins when SAMP bit is set
bit 1	SAMP: ADC Sample Enable bit
	 1 = ADC sample/hold amplifiers are sampling 0 = ADC sample/hold amplifiers are holding If ASAM = 0, software may write '1' to begin sampling. Automatically set by hardware if ASAM = 1. If SSRC = 000, software may write '0' to end sampling and start conversion. If SSRC ≠ 000, automatically cleared by hardware to end sampling and start conversion.
bit 0	DONE: ADC Conversion Status bit
	 1 = ADC conversion cycle is completed 0 = ADC conversion not started or in progress Automatically set by hardware when ADC conversion is complete. Software may write '0' to clear DONE status (software not allowed to write '1'). Clearing this bit will NOT affect any operation in progress. Automatically cleared by hardware at start of a new conversion.



REGISTER 22-2: ADxCON2: ADCx CONTROL REGISTER 2 (where x = 1 or 2)

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W- 0
	VCFG<2:0>		—	-	CSCNA	CHP
bit 15						Ľ
D O	11.0					DAM O

R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	—扫上面的二维码图案, R/W-0	加我为朋友。
BUFS	—	SMPI<3:0>			BUFM	ALTS		
bit 7							bit 0	

= Writable bit U = Unir	mplemented bit, read as	'0'
= Bit is set '0' = Bit	is cleared x =	= Bit is unknown
		·····, ···,

bit 15-13	VCFG<2:0>: Converter Voltage Reference Configuration bits

		Vref+	VREF-				
	000	Avdd	Avss				
	001	External VREF+	Avss				
	010	Avdd	External VREF-				
	011	External VREF+	External VREF-				
	1xx	Avdd	Avss				
bit 12-11	Unimp	lemented: Read as	s '0'				
bit 10	CSCN	A: Scan Input Selec	ctions for CH0+ dur	ing Sample A bit			
	1 = Scan inputs 0 = Do not scan inputs						
bit 9-8	CHPS	<1:0>: Selects Cha	nnels Utilized bits				
	When AD12B = 1, CHPS<1:0> is: U-0, Unimplemented, Read as '0'. 1x = Converts CH0, CH1, CH2 and CH3 01 = Converts CH0 and CH1 00 = Converts CH0						
bit 7	BUFS:	Buffer Fill Status b	it (only valid when l	BUFM = 1)			
	 1 = ADC is currently filling second half of buffer, user should access data in the first half 0 = ADC is currently filling first half of buffer, user should access data in the second half 						
bit 6	Unimplemented: Read as '0'						
bit 5-2	SMPI<3:0>: Selects Increment Rate for DMA Address Bits or Number of Sample/Conversion Operations per Interrupt bits						
	 1111 = Increments the DMA address or generates interrupt after completion of every 16th sample/ conversion operation 1110 = Increments the DMA address or generates interrupt after completion of every 15th sample/ conversion operation 						
	 0001 = Increments the DMA address or generates interrupt after completion of every 2nd sample/ version operation 						
	0000 =	 Increments the DI sion operation 	MA address or gene	erates interrupt after completion of every sample/conver-			
bit 1	BUFM	: Buffer Fill Mode S	elect bit				
		arts filling first half o wavs starts filling bu		errupt and the second half of buffer on next interrupt			

REGISTER 22-2: ADxCON2: ADCx CONTROL REGISTER 2 (CONTINUED) (where x = 1

- bit 0 ALTS: Alternate Input Sample Mode Select bit
 - 1 = Uses channel input selects for Sample A on first sample and Sample B on next sample
 - 0 = Always uses channel input selects for Sample A



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R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	P 4744_0
ADRC		0-0	N/W-0	N/W-U	SAMC<4:0> ⁽¹⁾		
pit 15					5AMC \$4.02		bit
							扫一扫上面的二维码图题
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			ADCS	<7:0> ⁽²⁾			
bit 7							bit
Legend:							
R = Readab	le bit	W = Writable bi	t	U = Unimple	mented bit, read	as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cl		x = Bit is u	nknown
bit 14-13 bit 12-8	SAMC<4:0> 11111 = 31	AD AD					
bit 7-0	11111111 = • • • • • •	Reserved					
	• • 00000010 = 0000001 =	Tcy · (ADCS<7: Tcy · (ADCS<7: Tcy · (ADCS<7:	0> + 1) = 3 0> + 1) = 2	• Tcy = Tad			

2: This bit is not used if ADxCON3<15> (ADRC) = 1.



REGISTER 22-4: ADxCON4: ADCx CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	_
bit 15						

							扫一扫上面的二维码	冯图案,加
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
—	—	—	—	_		DMABL<2:0>		
bit 7							bit 0	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3 Unimplemented: Read as '0'

bit 2-0

DMABL<2:0>: Selects Number of DMA Buffer Locations per Analog Input bits

111 = Allocates 128 words of buffer to each analog input

110 = Allocates 64 words of buffer to each analog input

101 = Allocates 32 words of buffer to each analog input

100 = Allocates 16 words of buffer to each analog input

011 = Allocates 8 words of buffer to each analog input

010 = Allocates 4 words of buffer to each analog input

001 = Allocates 2 words of buffer to each analog input

000 = Allocates 1 word of buffer to each analog input



REGISTER 22-5: ADxCHS123: ADCx INPUT CHANNEL 1, 2, 3 SELECT REGISTER

-							
	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W- 0 R/
	_		_	_	—	CH123N	NB<1:0>
I	bit 15						

							扫一扫上面的二维码图案,	加我为朋友
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
	—	—	_	_	CH123NA<1:0>		CH123SA	
bit 7		•			-		bit 0	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11	Unimplemented: Read as '0'
bit 10-9	CH123NB<1:0>: Channel 1, 2, 3 Negative Input Select for Sample B bits
	When AD12B = 1, CHxNB is: U-0, Unimplemented, Read as '0'. 11 = CH1 negative input is AN9; CH2 negative input is AN10; CH3 negative input is AN11 10 = CH1 negative input is AN6; CH2 negative input is AN7; CH3 negative input is AN8 0x = CH1, CH2, CH3 negative input is VREF-
bit 8	CH123SB: Channel 1, 2, 3 Positive Input Select for Sample B bit
	When AD12B = 1, CHxSB is: U-0, Unimplemented, Read as '0'. 1 = CH1 positive input is AN3; CH2 positive input is AN4; CH3 positive input is AN5 0 = CH1 positive input is AN0; CH2 positive input is AN1; CH3 positive input is AN2
bit 7-3	Unimplemented: Read as '0'
bit 2-1	CH123NA<1:0>: Channel 1, 2, 3 Negative Input Select for Sample A bits
	When AD12B = 1, CHxNA is: U-0, Unimplemented, Read as '0'. 11 = CH1 negative input is AN9; CH2 negative input is AN10; CH3 negative input is AN11 10 = CH1 negative input is AN6; CH2 negative input is AN7; CH3 negative input is AN8 0x = CH1, CH2, CH3 negative input is VREF-
bit 0	CH123SA: Channel 1, 2, 3 Positive Input Select for Sample A bit
	When AD12B = 1, CHxSA is: U-0, Unimplemented, Read as '0'. 1 = CH1 positive input is AN3; CH2 positive input is AN4; CH3 positive input is AN5 0 = CH1 positive input is AN0; CH2 positive input is AN1; CH3 positive input is AN2



REGISTER 22-6: ADxCHS0: ADCx INPUT CHANNEL 0 SELECT REGISTER

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB	—	—			CH0SB<4:0>	
bit 15						

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	——扫上面的三/ R/W-0				
CH0NA		_			CH0SA<4:0>	(1)					
bit 7							bit (
Legend:											
R = Readab	le bit	W = Writable bi	t	U = Unimple	mented bit, rea	ad as '0'					
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unk	nown				
bit 15	CHONB: Ch	annel 0 Negative	Innut Select	for Sample B h	hit						
	CH0NB: Channel 0 Negative Input Select for Sample B bit Same definition as bit 7.										
bit 14-13	Unimpleme	Unimplemented: Read as '0'									
bit 12-8	CH0SB<4:0>: Channel 0 Positive Input Select for Sample B bits										
	Same defini	ition as bit<4:0>.									
bit 7	CH0NA: Channel 0 Negative Input Select for Sample A bit										
	1 = Channel 0 negative input is AN1										
	0 = Channel 0 negative input is VREF-										
bit 6-5	Unimpleme	ented: Read as '0'									
bit 4-0	CH0SA<4:0>: Channel 0 Positive Input Select for Sample A bits ⁽¹⁾										
		nannel 0 positive ir									
	11110 = Channel 0 positive input is AN30										
	:										
	• 00010 - Ch	nannel 0 positive ir	put is AN2								
		nannel 0 positive ir	•								
	00001 - 01		10/11/1								

Note 1: ADC2 can only select AN0-AN15 as positive inputs.



REGISTER 22-7: ADxCSSH: ADCx INPUT SCAN SELECT REGISTER HIGH^(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W- 0
CSS31	CSS30	CSS29	CSS28	CSS27	CSS26	CSS25
bit 15						···

							扫一扫上面的二维码图案,	加我为朋
R/W-0								
CSS23	CSS22	CSS21	CSS20	CSS19	CSS18	CSS17	CSS16	
bit 7	•	•					bit 0	

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0

CSS<31:16>: ADC Input Scan Selection bits

- 1 = Select ANx for input scan
- 0 = Skip ANx for input scan
- **Note 1:** On devices without 32 analog inputs, all ADxCSSH bits may be selected by user. However, inputs selected for scan without a corresponding input on the device will convert VREFL.
 - **2:** CSSx = ANx, where x = 16 through 31.

REGISTER 22-8: ADxCSSL: ADCx INPUT SCAN SELECT REGISTER LOW^(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8
bit 15						·	bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			oit	U = Unimple	mented bit, read	d as '0'	
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown

bit 15-0

CSS<15:0>: ADC Input Scan Selection bits

1 =Select ANx for input scan

0 = Skip ANx for input scan

- **Note 1:** On devices without 16 analog inputs, all ADxCSSL bits may be selected by user. However, inputs selected for scan without a corresponding input on the device will convert VREF-.
 - **2:** CSSx = ANx, where x = 0 through 15.



REGISTER 22-9: ADxPCFGH: ADCx PORT CONFIGURATION REGISTER HIGH^(1,2,3,4)

R/W-0							
PCFG31	PCFG30	PCFG29	PCFG28	PCFG27	PCFG26	PCFG25	
bit 15							Ľ

							扫一扫上面的二维码	冯图案
R/W-0								
PCFG23	PCFG22	PCFG21	PCFG20	PCFG19	PCFG18	PCFG17	PCFG16	
bit 7							bit 0	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0

Γ.

PCFG<31:16>: ADC Port Configuration Control bits

1 = Port pin in Digital mode; port read input enabled; ADC input multiplexer connected to AVss
 0 = Port pin in Analog mode; port read input disabled; ADC samples pin voltage

- **Note 1:** On devices without 32 analog inputs, all PCFG bits are R/W by user. However, PCFG bits are ignored on ports without a corresponding input on the device.
 - 2: ADC2 only supports analog inputs, AN0-AN15; therefore, no ADC2 port Configuration register exists.
 - **3:** PCFGx = ANx, where x = 16 through 31.
 - **4:** The PCFGx bits have no effect if the ADC module is disabled by setting the ADxMD bit in the PMDx register. In this case, all port pins multiplexed with ANx will be in Digital mode.

REGISTER 22-10: ADxPCFGL: ADCx PORT CONFIGURATION REGISTER LOW^(1,2,3,4)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCFG15	PCFG14	PCFG13	PCFG12	PCFG11	PCFG10	PCFG9	PCFG8
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 PCFG<15:0>: ADC Port Configuration Control bits

- 1 = Port pin in Digital mode; port read input enabled; ADC input multiplexer connected to AVss
- 0 = Port pin in Analog mode; port read input disabled; ADC samples pin voltage
- **Note 1:** On devices without 16 analog inputs, all PCFG bits are R/W by user. However, PCFG bits are ignored on ports without a corresponding input on the device.
 - **2:** On devices with two analog-to-digital modules, both AD1PCFGL and AD2PCFGL will affect the configuration of port pins multiplexed with AN0-AN15.
 - **3:** PCFGx = ANx, where x = 0 through 15.
 - **4:** The PCFGx bits have no effect if the ADC module is disabled by setting the ADxMD bit in the PMDx register. In this case, all port pins multiplexed with ANx will be in Digital mode.

23.0 SPECIAL FEATURES

- **Note 1:** This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/X08A/ X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section "CodeGuard™ Security" 23. (DS70199), Section 24. "Programming and Diagnostics" (DS70207) and Section 25. "Device Configuration" (DS70194) in the "dsPIC33F/PIC24H Family Reference Manual", which are available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

dsPIC33FJXXXMCX06A/X08A/X10A devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- · Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard[™] Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming[™] (ICSP[™])
- In-Circuit Emulation

23.1 Configuration Bits

dsPIC33FJXXXMCX06A/X08A/X10/ nonvolatile memory implemental configuration bits. Refer to **Section figuration**" (DS70194) of the " Comity Deferrance Menual" for merce



Family Reference Manual", for more information on this implementation.

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped starting at program memory location 0xF80000.

The device Configuration register map is shown in Table 23-1.

The individual Configuration bit descriptions for the Configuration registers are shown in Table 23-2.

Note that address, 0xF80000, is beyond the user program memory space. In fact, it belongs to the configuration memory space (0x800000-0xFFFFF) which can only be accessed using table reads and table writes.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xF80000	FBS	RBS	<1:0>		_		BSS<2:0>		BWRP
0xF80002	FSS	RSS	<1:0>	—	—		SSS<2:0>		SWRP
0xF80004	FGS	_	_	_	—		GSS1	GSS0	GWRP
0xF80006	FOSCSEL	IESO	Reserved ⁽²⁾	—	—	—	FNC	SC<2:0>	
0xF80008	FOSC	FCKS	M<1:0>	—	—	—	OSCIOFNC POSCMD<1:0		ID<1:0>
0xF8000A	FWDT	FWDTEN	WINDIS	PLLKEN ⁽³⁾	WDTPRE		WDTPOST<3:0>		
0xF8000C	FPOR	PWMPIN	HPOL	LPOL	_	_	FPW	/RT<2:0>	
0xF8000E	FICD	Rese	rved ⁽¹⁾	JTAGEN	—	—	—	ICS<	:1:0>
0xF80010	FUID0			l	Jser Unit ID	Byte 0			
0xF80012	FUID1		User Unit ID Byte 1						
0xF80014	FUID2		User Unit ID Byte 2						
0xF80016	FUID3			L	Jser Unit ID	Byte 3			

TABLE 23-1: DEVICE CONFIGURATION REGISTER MAP

Legend: — = unimplemented bit, reads as '0'.

Note 1: These bits are reserved for use by development tools and must be programmed as '1'.

- 2: When read, this bit returns the current programmed value.
- **3:** This bit is unimplemented on dsPIC33FJ64MCX06A/X08A/X10A and dsPIC33FJ128MCX06A/X08A/X10A devices and reads as '0'.

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TABLE 23-2: CONFIGURATION BITS DESCRIPTION Г Ť

Bit Field	Register	RTSP Effect	Description	
BWRP	FBS	Immediate	1 = Boot segment may be written	羽 图案,加我为朋友。
BSS<2:0>	FBS	Immediate	Boot Segment Program Flash Code Protection Size bits x11 = No boot program Flash segment Boot space is 1K IW less VS: 110 = Standard security; boot program Flash segment starts at end of VS, ends at 0007FEh 010 = High security; boot program Flash segment starts at end of VS, ends at 0007FEh Boot space is 4K IW less VS: 101 = Standard security; boot program Flash segment starts at end of VS, ends at 001FFEh 001 = High security; boot program Flash segment starts at end of VS, ends at 001FFEh 001 = High security; boot program Flash segment starts at end of VS, ends at 001FFEh Boot space is 8K IW less VS: 100 = Standard security; boot program Flash segment starts at end of VS, ends at 003FFEh 000 = High security; boot program Flash segment starts at end of VS, ends at 003FFEh 000 = High security; boot program Flash segment starts at end of VS, ends at 003FFEh	
RBS<1:0>	FBS	Immediate	Boot Segment RAM Code Protection bits 11 = No boot RAM defined 10 = Boot RAM is 128 bytes 01 = Boot RAM is 256 bytes 00 = Boot RAM is 1024 bytes	
SWRP	FSS	Immediate	Secure Segment Program Flash Write Protection bit 1 = Secure segment may be written 0 = Secure segment is write-protected	



Bit Field	Register	RTSP Effect	Description	
SSS<2:0>	FSS	Immediate	Secure Segment Program Flash Code Protection Size bits	
			(FOR 128K and 256K DEVICES) x11 = No secure program Flash segment	加我为朋友。
			 Secure space is 8K IW less BS: 110 = Standard security; secure program Flash segment starts at end of BS, ends at 0x003FFE 010 = High security; secure program Flash segment starts at end of BS, ends at 0x003FFE 	
			 <u>Secure space is 16K IW less BS:</u> 101 = Standard security; secure program Flash segment starts at end of BS, ends at 0x007FFE 001 = High security; secure program Flash segment starts at end of BS, ends at 0x007FFE 	
			 Secure space is 32K IW less BS: 100 = Standard security; secure program Flash segment starts at end of BS, ends at 0x00FFFE 000 = High security; secure program Flash segment starts at end of BS, ends at 0x00FFFE 	
			(FOR 64K DEVICES) x11 = No Secure program Flash segment	
			 Secure space is 4K IW less BS: 110 = Standard security; secure program Flash segment starts at end of BS, ends at 0x001FFE 010 = High security; secure program Flash segment starts at end of BS, ends at 0x001FFE 	
			 Secure space is 8K IW less BS: 101 = Standard security; secure program Flash segment starts at end of BS, ends at 0x003FFE 001 = High security; secure program Flash segment starts at end of BS, ends at 0x003FFE 	
			<u>Secure space is 16K IW less BS:</u> 100 = Standard security; secure program Flash segment starts at end of BS, ends at 007FFEh 000 = High security; secure program Flash segment starts at end of BS, ends at 0x007FFE	
RSS<1:0>	FSS	Immediate	Secure Segment RAM Code Protection bits 11 = No secure RAM defined 10 = Secure RAM is 256 bytes less BS RAM 01 = Secure RAM is 2048 bytes less BS RAM 00 = Secure RAM is 4096 bytes less BS RAM	
GSS<1:0>	FGS	Immediate	 General Segment Code-Protect bits 11 = User program memory is not code-protected 10 = Standard security; general program Flash segment starts at end of SS, ends at EOM 0x = High security; general program Flash segment starts at end of SS, ends at EOM 	

TABLE 23-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)



TABLE 23-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Register	RTSP Effect	Description	
GWRP	FGS	Immediate	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected H=1Lmn=#	码图案,加我为朋
IESO	FOSCSEL	Immediate	 Two-Speed Oscillator Start-up Enable bit 1 = Start-up device with FRC, then automatically switch to the user-selected oscillator source when ready 0 = Start-up device with user-selected oscillator source 	
FNOSC<2:0>	FOSCSEL	If clock switch is enabled, RTSP effect is on any device Reset; otherwise, Immediate	Initial Oscillator Source Selection bits 111 = Internal Fast RC (FRC) oscillator with postscaler 110 = Internal Fast RC (FRC) oscillator with divide-by-16 101 = LPRC oscillator 100 = Secondary (LP) oscillator 011 = Primary (XT, HS, EC) oscillator with PLL 010 = Primary (XT, HS, EC) oscillator 001 = Internal Fast RC (FRC) oscillator with PLL 000 = FRC oscillator	
FCKSM<1:0>	FOSC	Immediate	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled	
OSCIOFNC	FOSC	Immediate	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is clock output 0 = OSC2 is general purpose digital I/O pin	-
POSCMD<1:0>	FOSC	Immediate	Primary Oscillator Mode Select bits 11 = Primary oscillator disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode	
FWDTEN	FWDT	Immediate	 Watchdog Timer Enable bit 1 = Watchdog Timer always enabled (LPRC oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register will have no effect.) 0 = Watchdog Timer enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register.) 	
WINDIS	FWDT	Immediate	Watchdog Timer Window Enable bit 1 = Watchdog Timer in Non-Window mode 0 = Watchdog Timer in Window mode	
PLLKEN	FWDT	Immediate	PLL Lock Enable bit 1 = Clock switch to PLL source will wait until the PLL lock signal is valid 0 = Clock switch will not wait for the PLL lock signal	
WDTPRE	FWDT	Immediate	Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32	
WDT- POST<3:0>	FWDT	Immediate	Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384 • • • • • • • • • • • • •	



TABLE 23-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Register	RTSP Effect	Description	
PWMPIN	FPOR	Immediate	1 = PWM module pins controlled by PORT register at device Reset	加我为朋友。
HPOL	FPOR	Immediate	Motor Control PWM High Side Polarity bit 1 = PWM module high side output pins have active-high output polarity 0 = PWM module high side output pins have active-low output polarity	
LPOL	FPOR	Immediate	Motor Control PWM Low Side Polarity bit 1 = PWM module low side output pins have active-high output polarity 0 = PWM module low side output pins have active-low output polarity	
FPWRT<2:0>	FPOR	Immediate	Power-on Reset Timer Value Select bits 111 = PWRT = 128 ms 110 = PWRT = 64 ms 101 = PWRT = 32 ms 100 = PWRT = 16 ms 011 = PWRT = 8 ms 010 = PWRT = 4 ms 001 = PWRT = 2 ms 000 = PWRT = Disabled	
JTAGEN	FICD	Immediate	JTAG Enable bit 1 = JTAG enabled 0 = JTAG disabled	
ICS<1:0>	FICD	Immediate	ICD Communication Channel Select bits 11 = Communicate on PGEC1 and PGED1 10 = Communicate on PGEC2 and PGED2 01 = Communicate on PGEC3 and PGED3 00 = Reserved	



23.2 On-Chip Voltage Regulator

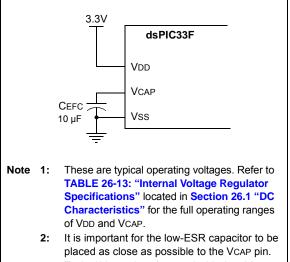
All of the dsPIC33FJXXXMCX06A/X08A/X10A devices power their core digital logic at a nominal 2.5V. This may create an issue for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33FJXXXMCX06A/X08A/X10A family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. The regulator requires that a low-ESR (less than 5 ohms) capacitor (such as tantalum or ceramic) be connected to the VCAP pin (Figure 23-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 26-13 of Section 26.1 "DC Characteristics".

Note: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

On a POR, it takes approximately 20 μ s for the on-chip voltage regulator to generate an output voltage. During this time, designated as TSTARTUP, code execution is disabled. TSTARTUP is applied every time the device resumes operation after any power-down.

FIGURE 23-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR^(1,2,3)



3: Typical VCAP pin voltage = 2.5V when $VDD \ge VDDMIN$.

23.3 BOR: Brown-out Reset

The BOR (Brown-out Reset) module is internal voltage reference circuit that regulated supply voltage, VCAP. The mathematical supply voltage is to generate a device reset where brown-out condition occurs. Brown-out conditions

generally caused by glitches on the AC mains (i.e., missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR will generate a Reset pulse which will reset the device. The BOR will select the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>). Furthermore, if an oscillator mode is selected, the BOR will activate the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, then the clock will be held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT time-out (TPWRT) will be applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM = 100 is applied. The total delay in this case is TFSCM.

The BOR Status bit (RCON<1>) will be set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and will reset the device should VDD fall below the BOR threshold voltage.

23.4 Watchdog Timer (WDT)

For dsPIC33FJXXXMCX06A/X08A/X10A devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler than can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a nominal WDT time-out period (TWDT) of 1 ms in 5-bit mode, or 4 ms in 7-bit mode.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>) which allow the selection of a total of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- · On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSC bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

If the WDT is enabled, it will continue t or Idle modes. When the WDT time device will wake the device and code tinue from where the PWRSAV instruct The corresponding SLEEP or IDLE bits need to be cleared in software after the device



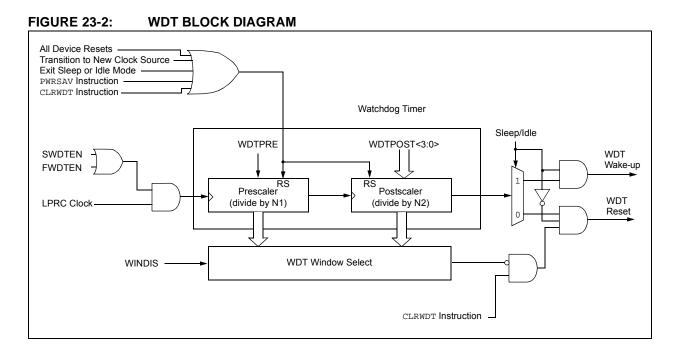
The WDT flag bit, WDTO (RCON<4>), is not automatically 加我为朋友. cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

Note:	The	CLRWDT	and	PWRSAV	instructions				
clear the prescaler and postscaler counts									
	wher	n execute	d.						

The WDT is enabled or disabled by the FWDTEN Configuration bit in the FWDT Configuration register. When the FWDTEN Configuration bit is set, the WDT is always enabled.

The WDT can be optionally controlled in software when the FWDTEN Configuration bit has been programmed to '0'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

Note: If the WINDIS bit (FWDT<6>) is cleared, the CLRWDT instruction should be executed by the application software only during the last 1/4 of the WDT period. This CLRWDT window can be determined by using a timer. If a CLRWDT instruction is executed before this window, a WDT Reset occurs.





23.5 JTAG Interface

dsPIC33FJXXXMCX06A/X08A/X10A devices implement a JTAG interface, which supports boundary scan device testing, as well as in-circuit programming. Detailed information on the interface will be provided in future revisions of the document.

23.6 Code Protection and CodeGuard[™] Security

The dsPIC33FJXXXMCX06A/X08A/X10A devices offer the advanced implementation of CodeGuard[™] Security. CodeGuard Security enables multiple parties to securely share resources (memory, interrupts and peripherals) on a single chip. This feature helps protect individual Intellectual Property (IP) in collaborative system designs.

When coupled with software encryption libraries, CodeGuard[™] Security can be used to securely update Flash even when multiple IPs are resident on the single chip. The code protection features vary depending on the actual device implemented. The following sections provide an overview of these features.

The code protection features are controlled by the Configuration registers: FBS, FSS and FGS.

Note: Refer to Section 23. "CodeGuard™ Security" (DS70199) in the "dsPIC33F/ PIC24H Family Reference Manual" for further information on usage, configuration and operation of CodeGuard Security.

23.7 In-Circuit Serial Progra

dsPIC33FJXXXMCX06A/X08A/X10A father is signal controllers can be serially programming the end application circuit. This is simply for power ground and the programming sequence. This allow

customers to manufacture boards with unprogrammed devices and then program the digital signal controller just before shipping the product. This also allows the most recent firmware, or a custom firmware, to be programmed. Please refer to the "*dsPIC33F/PIC24H Flash Programming Specification*" (DS70152) document for details about ICSP.

Any one out of three pairs of programming clock/data pins may be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- · PGEC3 and PGED3

23.8 In-Circuit Debugger

When MPLAB[®] ICD 2 is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pin functions.

Any one out of three pairs of debugging clock/data pins may be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- · PGEC3 and PGED3

To use the in-circuit debugger function of the device, the design must implement ICSP connections to $\overline{\text{MCLR}}$, VDD, VSS and the PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins.

24.0 INSTRUCTION SET SUMMARY

Note: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/X08A/ X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

The dsPIC33F instruction set is identical to that of the dsPIC30F.

Most instructions are a single program memory word (24 bits). Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word, divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into five basic categories:

- · Word or byte-oriented operations
- · Bit-oriented operations
- · Literal operations
- · DSP operations
- · Control operations

Table 24-1 shows the general symbols used in describing the instructions.

The dsPIC33F instruction set summary in Table 24-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand which is typically a register 'Wb' without any address modifier
- The second source operand which is typically a register 'Ws' with or without an address modifier
- The destination of the result which is typically a register 'Wd' with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- The file register specified by the value 'f'
- The destination, which could either be the file register 'f' or the W0 register, which is denoted as 'WREG'

Most bit-oriented instructions (includ shift instructions) have two operands



- The W register (with or without an modifier) or file register (specified 'Ws' or 'f')
- The bit in the W register or file register (specified by a literal value or indirectly by the #码图案, 加我为朋友 contents of register 'Wb')

The literal instructions that involve data movement may use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by the value of 'k')
- The W register or file register where the literal value is to be loaded (specified by 'Wb' or 'f')

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand which is a register 'Wb' without any address modifier
- The second source operand which is a literal value
- The destination of the result (only if not the same as the first source operand) which is typically a register 'Wd' with or without an address modifier

The MAC class of DSP instructions may use some of the following operands:

- The accumulator (A or B) to be used (required operand)
- The W registers to be used as the two operands
- The X and Y address space prefetch operations
- The X and Y address space prefetch destinations
- The accumulator write back destination

The other DSP instructions do not involve any multiplication and may include:

- The accumulator to be used (required)
- The source or destination operand (designated as Wso or Wdo, respectively) with or without an address modifier
- The amount of shift specified by a W register 'Wn' or a literal value

The control instructions may use some of the following operands:

- A program memory address
- The mode of the table read and table write instructions

All instructions are a single word, except for certain double-word instructions, which were made double-word instructions so that all the required information is available in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it will execute as a NOP.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles with the additional instruction cycle(s) executed as a NOP. Notable exceptions are the BRA (unconditional/computed branch), indirect CALL/GOTO, all table reads and writes and RETURN/RETFIE instructions, which are singleword instructions but take two or three cycles instructions that involve skipping over the instruction require either two or three cycles performed, depending on whether the ins skipped is a single-word or two-word Moreover, double-word moves require two cycles



double-word instructions execute in two high the double mage, mathing of the straight mathing the straightmathing the straight mathing

Note: For more details on the instruction set, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157).

Field	Description					
#text	Means literal defined by "text"					
(text)	Means "content of text"					
[text]	Means "the location addressed by text"					
{ }	Optional field or operation					
<n:m></n:m>	Register bit field					
.b	Byte mode selection					
.d	Double-Word mode selection					
.S	Shadow register select					
.W	Word mode selection (default)					
Acc	One of two accumulators {A, B}					
AWB	Accumulator Write-Back Destination Address register ∈ {W13, [W13]+ = 2}					
bit4	4-bit bit selection field (used in word addressed instructions) $\in \{015\}$					
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero					
Expr	Absolute address, label or expression (resolved by the linker)					
f	File register address ∈ {0x00000x1FFF}					
lit1	1-bit unsigned literal $\in \{0,1\}$					
lit4	4-bit unsigned literal ∈ {015}					
lit5	5-bit unsigned literal ∈ {031}					
lit8	8-bit unsigned literal ∈ {0255}					
lit10	10-bit unsigned literal \in {0255} for Byte mode, {0:1023} for Word mode					
lit14	14-bit unsigned literal ∈ {016384}					
lit16	16-bit unsigned literal $\in \{065535\}$					
lit23	23-bit unsigned literal ∈ {08388608}; LSb must be '0'					
None	Field does not require an entry, may be blank					
OA, OB, SA, SB	DSP Status bits: AccA Overflow, AccB Overflow, AccA Saturate, AccB Saturate					
PC	Program Counter					
Slit10	10-bit signed literal ∈ {-512511}					
Slit16	16-bit signed literal ∈ {-3276832767}					
Slit6	6-bit signed literal ∈ {-1616}					
Wb	Base W register ∈ {W0W15}					
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd], [++Wd], [Wd] }					
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd], [++Wnd], [Wnd], [Wnd+Wb] }					
Wm,Wn	Dividend, Divisor working register pair (direct addressing)					

TABLE 24-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

TABLE 24-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)

Field	Description	
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}	
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7} 扫一扫上面的二维码图案,	加我为朋
Wn	One of 16 working registers ∈ {W0W15}	
Wnd	One of 16 destination working registers ∈ {W0W15}	
Wns	One of 16 source working registers ∈ {W0W15}	
WREG	W0 (working register used in file register instructions)	
Ws	Source W register ∈ {Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws]}	
Wso	Source W register ∈ {Wns, [Wns], [Wns++], [Wns], [++Wns], [Wns], [Wns+Wb]}	
Wx	X Data Space Prefetch Address register for DSP instructions ∈ {[W8]+ = 6, [W8]+ = 4, [W8]+ = 2, [W8], [W8]- = 6, [W8]- = 4, [W8]- = 2, [W9]+ = 6, [W9]+ = 4, [W9]+ = 2, [W9], [W9]- = 6, [W9]- = 4, [W9]- = 2, [W9 + W12], none}	
Wxd	X Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}	
Wy	Y Data Space Prefetch Address register for DSP instructions ∈ {[W10]+ = 6, [W10]+ = 4, [W10]+ = 2, [W10], [W10]- = 6, [W10]- = 4, [W10]- = 2, [W11]+ = 6, [W11]+ = 4, [W11]+ = 2, [W11], [W11]- = 6, [W11]- = 4, [W11]- = 2, [W11 + W12], none}	
Wyd	Y Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}	



TABLE 24-2: INSTRUCTION SET OVERVIEW

	E 24-2:	INSTR	UCTION SET OVER					
Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles	fitaus lilags Afrected	
1	ADD	ADD	Acc	Add Accumulators	1	1	OA,OB,6A,SB	
		ADD	f	f = f + WREG	1	1	C,DC,N,OV,Z	
		ADD	f,WREG	WREG = f + WREG	1	1	GDGNAY,Z#	吗图案,加我为朋友。
		ADD	#lit10,Wn	Wd = lit10 + Wd	1	1	C,DC,N,OV,Z	
		ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1	C,DC,N,OV,Z	
		ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1	C,DC,N,OV,Z	
		ADD	Wso,#Slit4,Acc	16-bit Signed Add to Accumulator	1	1	OA,OB,SA,SB	
2	ADDC	ADDC	f	f = f + WREG + (C)	1	1	C,DC,N,OV,Z	
		ADDC	f,WREG	WREG = $f + WREG + (C)$	1	1	C,DC,N,OV,Z	
		ADDC	#lit10,Wn	Wd = Iit10 + Wd + (C)	1	1	C,DC,N,OV,Z	-
		ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1	C,DC,N,OV,Z	
		ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	C,DC,N,OV,Z	
3	AND	AND	f	f = f .AND. WREG	1	1	N,Z	
		AND	f,WREG	WREG = f .AND. WREG	1	1	N,Z	
		AND	#lit10,Wn	Wd = lit10 .AND. Wd	1	1	N,Z	
		AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1	N,Z	
		AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	N,Z	
4	ASR	ASR	f	f = Arithmetic Right Shift f	1	1	C,N,OV,Z	
		ASR	f,WREG	WREG = Arithmetic Right Shift f	1	1	C,N,OV,Z	
		ASR	Ws,Wd	Wd = Arithmetic Right Shift Ws	1	1	C,N,OV,Z	
		ASR	Wb,Wns,Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N,Z	
		ASR	Wb,#lit5,Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N,Z	
5	BCLR	BCLR	f,#bit4	Bit Clear f	1	1	None	
		BCLR	Ws,#bit4	Bit Clear Ws	1	1	None	
6	BRA	BRA	C,Expr	Branch if Carry	1	1 (2)	None	
		BRA	GE,Expr	Branch if greater than or equal	1	1 (2)	None	
		BRA	GEU,Expr	Branch if unsigned greater than or equal	1	1 (2)	None	
		BRA	GT,Expr	Branch if greater than	1	1 (2)	None	
		BRA	GTU,Expr	Branch if unsigned greater than	1	1 (2)	None	
		BRA	LE,Expr	Branch if less than or equal	1	1 (2)	None	
		BRA	LEU,Expr	Branch if unsigned less than or equal	1	1 (2)	None	
		BRA	LT,Expr	Branch if less than	1	1 (2)	None	
		BRA	LTU, Expr	Branch if unsigned less than	1	1 (2)	None	
		BRA	N,Expr	Branch if Negative	1	1 (2)	None	
		BRA	NC,Expr	Branch if Not Carry	1	1 (2)	None	
		BRA	NN,Expr	Branch if Not Negative	1	1 (2)	None	
		BRA	NOV,Expr	Branch if Not Overflow	1	1 (2)	None	
		BRA	NZ,Expr	Branch if Not Zero	1	1 (2)	None	
		BRA	OA,Expr	Branch if Accumulator A overflow	1	1 (2)	None	
		BRA	OB,Expr	Branch if Accumulator B overflow	1	1 (2)	None	
		BRA	OV,Expr	Branch if Overflow	1	1 (2)	None	
		BRA	SA, Expr	Branch if Accumulator A saturated	1	1 (2)	None	
		BRA	SB, Expr	Branch if Accumulator B saturated	1	1 (2)	None	
		BRA	Expr	Branch Unconditionally	1	2	None	
		BRA	Z,Expr	Branch if Zero	1	1 (2)	None	
		BRA	Wn	Computed Branch	1	2	None	
7	BSET	BSET	f,#bit4	Bit Set f	1	1	None	
•		BSET	Ws,#bit4	Bit Set Ws	1	1	None	1
8	BSW	BSW.C	WS,#DIC4 WS,Wb	Write C bit to Ws <wb></wb>	1	1	None	1
5	101	BSW.Z	WS,WD WS,Wb	Write Z bit to Ws <wb></wb>	1	1	None	1
9	BTG	BSW.2 BTG	f,#bit4	Bit Toggle f	1	1	None	1
5	510	BIG	Ws,#bit4	Bit Toggle Ws	1	1	None	1
		DIG	110, #DIUI	Dit loggie wa	1	<u> </u>	NULLE	1
10	BTSC	BTSC	f,#bit4	Bit Test f, Skip if Clear	1	1 (2 or 3)	None	



TABLE 24-2: INSTRUCTION SET OVERVIEW (CONTINUED)

IADL	E 24-2:	INSIRU	JCTION SET OVERVIE			_		
Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# d Cyclee	Status Flags Africted	
11	BTSS	BTSS	f,#bit4	Bit Test f, Skip if Set	1	(2 or 3)	nto e	
		BTSS	Ws,#bit4	Bit Test Ws, Skip if Set	1		None 扫上面的二维码图案,	- 加我为朋友。
12	BTST	BTST	f,#bit4	Bit Test f	1	1	Z	1
		BTST.C	Ws,#bit4	Bit Test Ws to C	1	1	С	
		BTST.Z	Ws,#bit4	Bit Test Ws to Z	1	1	Z	-
		BTST.C	Ws,Wb	Bit Test Ws <wb> to C</wb>	1	1	С	-
		BTST.Z	Ws,Wb	Bit Test Ws <wb> to Z</wb>	1	1	Z	-
13	BTSTS	BTSTS	f,#bit4	Bit Test then Set f	1	1	Z	-
		BTSTS.C	Ws,#bit4	Bit Test Ws to C, then Set	1	1	С	-
		BTSTS.Z	Ws,#bit4	Bit Test Ws to Z, then Set	1	1	Z	-
14	CALL	CALL	lit23	Call Subroutine	2	2	None	-
		CALL	Wn	Call Indirect Subroutine	1	2	None	-
15	CLR	CLR	f	f = 0x0000	1	1	None	-
		CLR	WREG	WREG = 0x0000	1	1	None	1
		CLR	Ws	Ws = 0x0000	1	1	None	-
		CLR	Acc,Wx,Wxd,Wy,Wyd,AWB	Clear Accumulator	1	1	OA,OB,SA,SB	1
16	CLRWDT	CLRWDT		Clear Watchdog Timer	1	1	WDTO,Sleep	-
17	СОМ	СОМ	f	$f = \overline{f}$	1	1	N,Z	1
	0011	COM	f,WREG	WREG = f	1	1	N,Z	-
				$Wd = \overline{Ws}$	1	1	N,Z	-
18	CP	COM	Ws,Wd f	Compare f with WREG	1	1	C,DC,N,OV,Z	-
10	CP	CP		Compare Wb with lit5	1	1	C,DC,N,OV,Z	-
		CP	Wb,#lit5	Compare Wb with Ws (Wb – Ws)	1	1	C,DC,N,OV,Z C,DC,N,OV,Z	-
19	CD0		Wb,Ws f		1	1		-
19	CP0	CP0		Compare f with 0x0000	1	1	C,DC,N,OV,Z	-
20	CPB	CP0	Ws f	Compare Ws with 0x0000 Compare f with WREG, with Borrow	1	1	C,DC,N,OV,Z C,DC,N,OV,Z	-
20	CPB	CPB CPB		Compare Wb with lit5, with Borrow	1	1	C,DC,N,OV,Z C,DC,N,OV,Z	-
		СРВ	Wb,#lit5 Wb,Ws	Compare Wb with HIS, with Borrow (Wb – Ws – \overline{C})	1	1	C,DC,N,OV,Z	-
21	CPSEQ	CPSEQ	Wb, Wn	Compare Wb with Wn, Skip if =	1	1 (2 or 3)	None	-
22	CPSGT	CPSGT	Wb, Wn	Compare Wb with Wn, Skip if >	1	(2 or 3)	None	-
23	CPSLT	CPSLT	Wb, Wn	Compare Wb with Wn, Skip if <	1	(2 or 3)	None	1
24	CPSNE	CPSNE	Wb, Wn	Compare Wb with Wn, Skip if ≠	1	1 (2 or 3)	None	1
25	DAW	DAW	Wn	Wn = Decimal Adjust Wn	1	1	С	
26	DEC	DEC	f	f = f - 1	1	1	C,DC,N,OV,Z]
		DEC	f,WREG	WREG = f – 1	1	1	C,DC,N,OV,Z	
		DEC	Ws,Wd	Wd = Ws - 1	1	1	C,DC,N,OV,Z	
27	DEC2	DEC2	f	f = f - 2	1	1	C,DC,N,OV,Z	
		DEC2	f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z	
		DEC2	Ws,Wd	Wd = Ws - 2	1	1	C,DC,N,OV,Z	
28	DISI	DISI	#lit14	Disable Interrupts for k Instruction Cycles	1	1	None	
29	DIV	DIV.S	Wm,Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV	
		DIV.SD	Wm,Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV	
		DIV.U	Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV	
		DIV.UD	Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV	
30	DIVF	DIVF	Wm,Wn	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV]
31	DO	DO	<pre>#lit14,Expr</pre>	Do Code to PC + Expr, lit14 + 1 Times	2	2	None]
		DO	Wn,Expr	Do Code to PC + Expr, (Wn) + 1 Times	2	2	None]
32	ED	ED	Wm*Wm,Acc,Wx,Wy,Wxd	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB, SA,SB,SAB]
33	EDAC	EDAC	Wm*Wm,Acc,Wx,Wy,Wxd	Euclidean Distance	1	1	OA,OB,OAB, SA,SB,SAB	



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С

None

None

N 7

N,Z

N.Z

N,Z

N.Z

None

N,Z

N.Z

None

None

N,Z

None

None

None

None

None

None

None

None

OA.OB.OAB.

SA,SB,SAB

OA,OB,OAB,

SA,SB,SAB

None

OA,OB,OAB,

SA.SB.SAB

INSTRUCTION SET OVERVIEW (CONTINUED) Base Assembly # of # of 184 Assembly Syntax Instr Description Words Mnemonic Cycles 34 EXCH EXCH Swap Wns with Wnd 1 1 Wns,Wnd 35 FBCL Find Bit Change from Left (MSb) Side 1 1 FBCL Ws,Wnd 36 FF1L FF1L Ws,Wnd Find First One from Left (MSb) Side 1 1 37 FF1R FF1R Ws.Wnd Find First One from Right (LSb) Side 1 1 38 2 2 GOTO GOTO Expr Go to Address GOTO Go to Indirect 1 2 Wn f = f + 1 39 1 C,DC,N,OV,Z TNC TNC f 1 WREG = f + 11 C,DC,N,OV,Z INC f,WREG 1 TNC Ws,Wd Wd = Ws + 11 1 C,DC,N,OV,Z 40 INC2 INC2 f = f + 2 1 1 C,DC,N,OV,Z f WREG = f + 21 C,DC,N,OV,Z INC2 f,WREG 1 INC2 Wd = Ws + 2 1 1 C,DC,N,OV,Z Ws,Wd 41 TOR TOR f f = f .IOR. WREG 1 1 WREG = f .IOR. WREG 1 1 IOR f,WREG Wd = lit10 .IOR. Wd 1 IOR #lit10,Wn 1 Wd = Wb .IOR. Ws 1 1 IOR Wb,Ws,Wd IOR Wb,#lit5,Wd Wd = Wb .IOR. lit5 1 1 42 LAC LAC Wso,#Slit4,Acc Load Accumulator 1 1 OA,OB,OAB, SA,SB,SAB 43 L'NK LNK #lit14 Link Frame Pointer 1 1 1 1 44 LSR f = Logical Right Shift f C,N,OV,Z LSR f LSR f,WREG WREG = Logical Right Shift f 1 1 C,N,OV,Z LSR Ws,Wd Wd = Logical Right Shift Ws 1 1 C,N,OV,Z Wnd = Logical Right Shift Wb by Wns 1 1 LSR Wb,Wns,Wnd Wnd = Logical Right Shift Wb by lit5 1 LSR Wb,#lit5,Wnd 1 45 OA,OB,OAB, MAC 1 1 MAC Wm*Wn, Acc, Wx, Wxd, Wy, Wyd Multiply and Accumulate SA SB SAB AWB MAC Wm*Wm,Acc,Wx,Wxd,Wy,Wyd Square and Accumulate 1 1 OA,OB,OAB, SA,SB,SAB 46 MOV MOV f,Wn Move f to Wn 1 1 MOV f Move f to f 1 1 Move f to WREG 1 1 MOV f,WREG MOV #lit16.Wn Move 16-bit Literal to Wn 1 1 Move 8-bit Literal to Wn MOV.b #lit8,Wn 1 1 MOV Wn,f Move Wn to f 1 1 MOV Wso,Wdo Move Ws to Wd 1 1 Move WREG to f 1 1 MOV WREG, f Move Double from W(ns):W(ns + 1) to Wd 2 MOV.D Wns,Wd 1 Move Double from Ws to W(nd + 1):W(nd) 1 2 MOV D Ws . Wnd 47 Prefetch and Store Accumulator 1 MOVSAC MOVSAC Acc, Wx, Wxd, Wy, Wyd, AWB 1

TABLE 24-2:

48

49

50

MPY

MPY.N

MSC

MPY

MPY

MPY.N

MSC

Wm*Wn, Acc, Wx, Wxd, Wy, Wyd

Wm*Wm,Acc,Wx,Wxd,Wy,Wyd

Wm*Wn, Acc, Wx, Wxd, Wy, Wyd

AWB

Wm*Wm, Acc, Wx, Wxd, Wy, Wyd

1

1

1

1

1

1

1

1

Multiply Wm by Wn to Accumulator

-(Multiply Wm by Wn) to Accumulator

Multiply and Subtract from Accumulator

Square Wm to Accumulator



TABLE 24-2: INSTRUCTION SET OVERVIEW (CONTINUED)

TABLE 24-2:		INSTRUCTION SET OVERVIEW (CONTINUED)				_		
Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# d Cycles	Statue Flags Affected	
51	MUL	MUL.SS	Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * signed(Ws)	1		Note	
		MUL.SU	Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws)	1	1	None	
		MUL.US	Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws)	1	1 _扫 -	扫上面的白外的图案,	加我为朋友
		MUL.UU	Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	None	
		MUL.SU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	None	
		MUL.UU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	None	
		MUL	f	W3:W2 = f * WREG	1	1	None	
52	NEG	NEG	Асс	Negate Accumulator	1	1	OA,OB,OAB, SA,SB,SAB	
		NEG	f	$f = \overline{f} + 1$	1	1	C,DC,N,OV,Z	
		NEG	f,WREG	WREG = \overline{f} + 1	1	1	C,DC,N,OV,Z	
		NEG	Ws,Wd	$Wd = \overline{Ws} + 1$	1	1	C,DC,N,OV,Z	
53	NOP	NOP		No Operation	1	1	None	
		NOPR		No Operation	1	1	None	
54	POP	POP	f	Pop f from Top-of-Stack (TOS)	1	1	None	1
		POP	Wdo	Pop from Top-of-Stack (TOS) to Wdo	1	1	None	1
		POP.D	Wnd	Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1)	1	2	None	
		POP.S		Pop Shadow Registers	1	1	All	
55	PUSH	PUSH	f	Push f to Top-of-Stack (TOS)	1	1	None	
		PUSH	Wso	Push Wso to Top-of-Stack (TOS)	1	1	None	
		PUSH.D	Wns	Push W(ns):W(ns + 1) to Top-of-Stack (TOS)	1	2	None	
		PUSH.S		Push Shadow Registers	1	1	None	
56	PWRSAV	PWRSAV	#lit1	Go into Sleep or Idle mode	1	1	WDTO,Sleep	
57	RCALL	RCALL	Expr	Relative Call	1	2	None	
		RCALL	Wn	Computed Call	1	2	None	
58	REPEAT	REPEAT	#lit14	Repeat Next Instruction lit14 + 1 Times	1	1	None	
		REPEAT	Wn	Repeat Next Instruction (Wn) + 1 Times	1	1	None	
59	RESET	RESET		Software Device Reset	1	1	None	
60	RETFIE	RETFIE		Return from Interrupt	1	3 (2)	None	
61	RETLW	RETLW	#lit10,Wn	Return with Literal in Wn	1	3 (2)	None	
62	RETURN	RETURN		Return from Subroutine	1	3 (2)	None	
63	RLC	RLC	f	f = Rotate Left through Carry f	1	1	C,N,Z	
		RLC	f,WREG	WREG = Rotate Left through Carry f	1	1	C,N,Z	
		RLC	Ws,Wd	Wd = Rotate Left through Carry Ws	1	1	C,N,Z	
64	RLNC	RLNC	f	f = Rotate Left (No Carry) f	1	1	N,Z	
		RLNC	f,WREG	WREG = Rotate Left (No Carry) f	1	1	N,Z	
		RLNC	Ws,Wd	Wd = Rotate Left (No Carry) Ws	1	1	N,Z	
65	RRC	RRC	f	f = Rotate Right through Carry f	1	1	C,N,Z	
	-	RRC	f,WREG	WREG = Rotate Right through Carry f	1	1	C,N,Z	
		RRC	Ws,Wd	Wd = Rotate Right through Carry Ws	1	1	C,N,Z	
66	RRNC	RRNC	f	f = Rotate Right (No Carry) f	1	1	N,Z	
		RRNC	f,WREG	WREG = Rotate Right (No Carry) f	1	1	N,Z	
		RRNC	Ws,Wd	Wd = Rotate Right (No Carry) Ws	1	1	N,Z	
67	SAC	SAC	Acc,#Slit4,Wdo	Store Accumulator	1	1	None	
07	SAC	SAC.R		Store Rounded Accumulator	1	1	None	
68	SE	SAC.R SE	Acc,#Slit4,Wdo Ws,Wnd	Wnd = Sign-Extended Ws	1	1	C,N,Z	1
69	SETM	SETM	f	f = 0xFFFF	1	1	None	1
00	UL IN		WREG	WREG = 0xFFFF	1	1	None	1
		SETM		WREG = 0xFFFF Ws = 0xFFFF	1	1	None	1
70	SFTAC	SETM	Ws Acc,Wn	Arithmetic Shift Accumulator by (Wn)	1	1	OA,OB,OAB, SA,SB,SAB	
		SFTAC	Acc,#Slit6	Arithmetic Shift Accumulator by Slit6	1	1	OA,OB,OAB, SA,SB,SAB	

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Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles	ihalvs illaus Attorned
71	SL	SL	f	f = Left Shift f	1	1	
		SL	f,WREG	WREG = Left Shift f	1	1	C,N,OV,Z
		SL	Ws,Wd	Wd = Left Shift Ws	1	1	扫C, 1, 2146二维码图案,
		SL	Wb,Wns,Wnd	Wnd = Left Shift Wb by Wns	1	1	N,Z
		SL	Wb,#lit5,Wnd	Wnd = Left Shift Wb by lit5	1	1	N,Z
72	SUB	SUB	Acc	Subtract Accumulators	1	1	OA,OB,OAB, SA,SB,SAB
		SUB	f	f = f – WREG	1	1	C,DC,N,OV,Z
		SUB	f,WREG	WREG = f – WREG	1	1	C,DC,N,OV,Z
		SUB	#lit10,Wn	Wn = Wn - lit10	1	1	C,DC,N,OV,Z
		SUB	Wb,Ws,Wd	Wd = Wb - Ws	1	1	C,DC,N,OV,Z
		SUB	Wb,#lit5,Wd	Wd = Wb - lit5	1	1	C,DC,N,OV,Z
73	SUBB	SUBB	f	$f = f - WREG - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	f,WREG	WREG = $f - WREG - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	#lit10,Wn	$Wn = Wn - lit10 - (\overline{C})$	1	1	C,DC,N,OV,Z
1		SUBB	Wb,Ws,Wd	$Wd = Wb - Ws - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	Wb,#lit5,Wd	$Wd = Wb - lit5 - (\overline{C})$	1	1	C,DC,N,OV,Z
74	SUBR	SUBR	f	f = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	f,WREG	WREG = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	Wb,Ws,Wd	Wd = Ws – Wb	1	1	C,DC,N,OV,Z
		SUBR	Wb,#lit5,Wd	Wd = lit5 – Wb	1	1	C,DC,N,OV,Z
75	SUBBR	SUBBR	f	$f = WREG - f - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBBR	f,WREG	WREG = WREG – f – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBBR	Wb,Ws,Wd	$Wd = Ws - Wb - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBBR	Wb,#lit5,Wd	$Wd = lit5 - Wb - (\overline{C})$	1	1	C,DC,N,OV,Z
76	SWAP	SWAP.b	Wn	Wn = Nibble Swap Wn	1	1	None
		SWAP	Wn	Wn = Byte Swap Wn	1	1	None
77	TBLRDH	TBLRDH	Ws,Wd	Read Prog<23:16> to Wd<7:0>	1	2	None
78	TBLRDL	TBLRDL	Ws,Wd	Read Prog<15:0> to Wd	1	2	None
79	TBLWTH	TBLWTH	Ws,Wd	Write Ws<7:0> to Prog<23:16>	1	2	None
80	TBLWTL	TBLWTL	Ws,Wd	Write Ws to Prog<15:0>	1	2	None
81	ULNK	ULNK		Unlink Frame Pointer	1	1	None
82	XOR	XOR	f	f = f .XOR. WREG	1	1	N,Z
		XOR	f,WREG	WREG = f .XOR. WREG	1	1	N,Z
		XOR	#lit10,Wn	Wd = lit10 .XOR. Wd	1	1	N,Z
		XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	N,Z
		XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	N,Z
83	ZE	ZE	Ws,Wnd	Wnd = Zero-Extend Ws	1	1	C,Z,N

TABLE 24-2: INSTRUCTION SET OVERVIEW (CONTINUED)

25.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers and dsPIC[®] digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
- MPLAB[®] IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB C Compiler for Various Device Families
 - HI-TECH C[®] for Various Device Families
 - MPASM[™] Assembler
 - MPLINK[™] Object Linker/ MPLIB[™] Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
 - MPLAB ICD 3
 - PICkit™ 3 Debug Express
- Device Programmers
 - PICkit[™] 2 Programmer
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

25.1 MPLAB Integrated De Environment Softwar



The MPLAB IDE software brings and development previously unseen in the meridian operating system-based application that contains:

- A single graphical interface to all debugging tools
- Simulator
- Programmer (sold separately)
- In-Circuit Emulator (sold separately)
- In-Circuit Debugger (sold separately)
- · A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- · Mouse over variable inspection
- Drag and drop variables from source to watch windows
- · Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- · Debug using:
 - Source files (C or assembly)
 - Mixed C and assembly
 - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.



25.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

25.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, preprocessor, and one-step driver, and can run on multiple platforms.

25.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- · Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

25.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines objects created by the MPASM Assemption MPLAB C18 C Compiler. It can link relocatable

from precompiled libraries, using directives归frem上编码图案, 加我为朋友, linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

25.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- · Support for the entire device instruction set
- · Support for fixed-point and floating-point data
- Command line interface
- · Rich directive set
- · Flexible macro language
- · MPLAB IDE compatibility

25.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC[®] DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

25.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC[®] Flash MCUs and dsPIC[®] Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with incircuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

25.9 MPLAB ICD 3 In-Circ System



MPLAB ICD 3 In-Circuit Debugger chip's most cost effective highdebugger/programmer for Microchip

nal Controller (DSC) and microcontroller (MCU) methodevices. It debugs and programs PIC[®] Flash microcontrollers and dsPIC[®] DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

25.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC[®] and dsPIC[®] Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming[™].

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.



25.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit[™] 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit[™] 2 enables in-circuit debugging on most PIC[®] microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

25.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

25.13 Demonstration/Develop Boards, Evaluation Kits, Starter Kits

A wide variety of demonstration, development evaluation boards for various PIC MCUs and ds

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM[™] and dsPICDEM[™] demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ[®] security ICs, CAN, IrDA[®], PowerSmart battery management, SEEVAL[®] evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

26.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33FJXXXMCX06A/X08A/X10A electrical characterinformation will be provided in future revisions of this document as it becomes available.

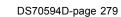
Absolute maximum ratings for the dsPIC33FJXXXMCX06A/X08A/X10A family are listed below. Exposure of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied _##BER, intty beta.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias	
Storage temperature	65°C to +160°C
Voltage on VDD with respect to Vss	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to Vss ⁽⁴⁾	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when $VDD \ge 3.0V^{(4)}$	-0.3V to +5.6V
Voltage on any 5V tolerant pin with respect to Vss when $V_{DD} < 3.0V^{(4)}$	-0.3V to 3.6V
Maximum current out of Vss pin	
Maximum current into VDD pin ⁽²⁾	
Maximum current sourced/sunk by any 2x I/O pin ⁽³⁾	8 mA
Maximum current sourced/sunk by any 4x I/O pin ⁽³⁾	
Maximum current sourced/sunk by any 8x I/O pin ⁽³⁾	
Maximum current sunk by all ports	
Maximum current sourced by all ports ⁽²⁾	200 mA

- **Note 1:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
 - 2: Maximum allowable current is a function of device maximum power dissipation (see Table 26-2).
 - **3:** Exceptions are CLKOUT, which is able to sink/source 25 mA, and the VREF+, VREF-, SCLx, SDAx, PGECx and PGEDx pins, which are able to sink/source 12 mA.
 - 4: See the "Pin Diagrams" section for 5V tolerant pins.







26.1 DC Characteristics

TABLE 26-1: OPERATING MIPS vs. VOLTAGE

Param	VDD Range	Temp Range	Max MIPS	
No.	(in Volts)	(in °C)	dsPIC33FJXXXMCX06A/X08A/X10A	
—	VBOR-3.6V ⁽¹⁾	-40°C to +85°C	40 40	-
_	VBOR-3.6V ⁽¹⁾	-40°C to +125°C	40	

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules such as the ADC will have degraded performance. Device functionality is tested but not characterized. Refer to parameter BO10 in Table 26-11 for the minimum and maximum BOR values.

TABLE 26-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Тур	Max	Unit
dsPIC33FJXXXMCX06A/X08A/X10A					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range		-40	_	+155	°C
Operating Ambient Temperature Range	TA	-40	_	+125	°C
Power Dissipation: Internal Chip Power Dissipation: $PINT = VDD x (IDD - \Sigma IOH)$	PD	Pint + Pi/o			W
I/O Pin Power Dissipation: I/O = Σ ({VDD - VOH} x IOH) + Σ (VOL x IOL)					
Maximum Allowed Power Dissipation	PDMAX	(TJ — TA)/θJ	IA	W

TABLE 26-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Тур	Max	Unit	Notes
Package Thermal Resistance, 100-pin TQFP (14x14x1 mm)	θJA	40		°C/W	1
Package Thermal Resistance, 100-pin TQFP (12x12x1 mm)	θJA	40	-	°C/W	1
Package Thermal Resistance, 80-pin TQFP (12x12x1 mm)	θJA	40	_	°C/W	1
Package Thermal Resistance, 64-pin TQFP (10x10x1 mm)	θJA	40	_	°C/W	1
Package Thermal Resistance, 64-pin QFN (9x9x0.9 mm)	θJA	28		°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ JA) numbers are achieved by package simulations.



TABLE 26-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			(unless	d Operat otherwis	ature	d) -40°C ≤	3.0V to 3 .6V TA \leq +85°C TA \leq +125°C TA \leq +125°C TA \leq +125°C	
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions ^{1-维码图案,} 加我	沩月
Operati	ng Voltag	e						
DC10	Supply V	/oltage						
	Vdd	_	3.0		3.6	V	—	
DC12	Vdr	RAM Data Retention Voltage ⁽²⁾	1.8		_	V	—	
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	—		Vss	V	_	
DC17	Svdd	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.03	_	_	V/ms	0-3.0V in 0.1s	

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

2: This is the limit to which VDD can be lowered without losing RAM data.



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TABLE 26-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS

Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended

Parameter No. ⁽³⁾	Typical ⁽²⁾	Max	Units		Conditions	扫一扫上面的二维码	
Operating Cur	rent (IDD) ⁽¹⁾						
DC20d	27	30	mA	-40°C			
DC20a	27	30	mA	+25°C	2.21/		
DC20b	27	30	mA	+85°C	- 3.3V	10 MIPS	
DC20c	27	35	mA	+125°C	1		
DC21d	36	40	mA	-40°C			
DC21a	37	40	mA	+25°C			
DC21b	38	45	mA	+85°C	- 3.3V	16 MIPS	
DC21c	39	45	mA	+125°C	1		
DC22d	43	50	mA	-40°C			
DC22a	46	50	mA	+25°C			
DC22b	46	55	mA	+85°C	- 3.3V	20 MIPS	
DC22c	47	55	mA	+125°C	1		
DC23d	65	70	mA	-40°C			
DC23a	65	70	mA	+25°C			
DC23b	65	70	mA	+85°C	3.3V	30 MIPS	
DC23c	65	70	mA	+125°C			
DC24d	84	90	mA	-40°C			
DC24a	84	90	mA	+25°C			
DC24b	84	90	mA	+85°C	- 3.3V	40 MIPS	
DC24c	84	90	mA	+125°C	1		

Note 1: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

• Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)

- CLKO is configured as an I/O input pin in the Configuration word
- All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (defined PMDx bits are set to zero and unimplemented PMDx bits are set to one)
- CPU executing while(1) statement
- · JTAG is disabled
- 2: These parameters are characterized but not tested in manufacturing.
- **3:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.



TABLE 26-6: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACT	ERISTICS		(unless oth		s: 3.0V to 3.6V ≤ Ta ≤ +85°C for Ind ≤ Ta ≤ +125°C for Ex	
Parameter No. ⁽³⁾	Typical ⁽²⁾	Max	Units		Conditions	扫一扫上面的二维码图案,扩
Idle Current (li	DLE): Core Of	f, Clock On	Base Current	(1)		
DC40d	3	25	mA	-40°C		
DC40a	3	25	mA	+25°C		
DC40b	3	25	mA	+85°C	3.3V	10 MIPS
DC40c	3	25	mA	+125°C	-	
DC41d	4	25	mA	-40°C		
DC41a	5	25	mA	+25°C	2.21/	
DC41b	6	25	mA	+85°C	3.3V	16 MIPS
DC41c	6	25	mA	+125°C		
DC42d	8	25	mA	-40°C		
DC42a	9	25	mA	+25°C	2.21/	
DC42b	10	25	mA	+85°C	3.3V	20 MIPS
DC42c	10	25	mA	+125°C	-	
DC43a	15	25	mA	+25°C		
DC43d	15	25	mA	-40°C	3.3∨	30 MIPS
DC43b	15	25	mA	+85°C	3.3V	30 MIPS
DC43c	15	25	mA	+125°C		
DC44d	16	25	mA	-40°C		
DC44a	16	25	mA	+25°C	2.21/	
DC44b	16	25	mA	+85°C	3.3V	40 MIPS
DC44c	16	25	mA	+125°C	1	

Note 1: Base IIDLE current is measured as follows:

• CPU core is off, oscillator is configured in EC mode and external clock active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)

· CLKO is configured as an I/O input pin in the Configuration word

· All I/O pins are configured as inputs and pulled to Vss

• MCLR = VDD, WDT and FSCM are disabled

• No peripheral modules are operating; however, every peripheral is being clocked (defined PMDx bits are set to zero and unimplemented PMDx bits are set to one)

- · JTAG is disabled
- **2:** These parameters are characterized but not tested in manufacturing.
- **3:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.



TABLE 26-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS

Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended

Parameter No. ⁽³⁾	Typical ⁽²⁾	Max	Units			Conditions	扫一扫上面的二维	
Power-Down	Current (IPD) ⁽	(1)						
DC60d	50	200	μA	-40°C				
DC60a	50	200	μA	+25°C	3.3V	Base Power-Down C	Current(3)	
DC60b	200	500	μA	+85°C		Dase Fower-Down G	unenter	
DC60c	600	1000	μA	+125°C				
DC61d	8	13	μA	-40°C				
DC61a	10	15	μA	+25°C	3.3V	Watchdog Timer Curr	urrent: ALADT(3)	
DC61b	12	20	μA	+85°C	3.3V			
DC61c	13	25	μΑ	+125°C				

Note 1: IPD (Sleep) current is measured as follows:

 CPU core is off, oscillator is configured in EC mode and external clock active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)

- · CLKO is configured as an I/O input pin in the Configuration word
- All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled, all peripheral modules except the ADC are disabled (PMDx bits are all '1's). The following ADC settings are enabled for each ADC module (ADCx) prior to executing the PWRSAV instruction: ADON = 1, VCFG = 1, AD12B = 1 and ADxMD = 0.
- VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to stand-by while the device is in Sleep mode)
- RTCC is disabled.
- JTAG is disabled
- 2: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated.
- **3:** The Watchdog Timer Current is the additional current consumed when the WDT module is enabled. This current should be added to the base IPD current.
- 4: These currents are measured on the device containing the most memory in this family.
- 5: These parameters are characterized, but are not tested in manufacturing.



DC CHARACTERISTICS: DOZE CURRENT (IDOZE) **TABLE 26-8:**

DC CHARAC	TERISTICS		$\begin{array}{l} \mbox{Standard Operating Conditions: } 3.0V \ to \ 3.6V \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \ for \ Induce -40^\circ C \leq TA \leq +125^\circ C \ for \ Extended \\ \end{array}$					
Parameter No.	Typical ⁽²⁾	Max	Doze Ratio	Units		Conditions	扫一扫上面的二维码图案,加:	
Doze Current	(IDOZE) ⁽¹⁾							
DC73a	11	35	1:2	mA		3.3V 3.3V		
DC73f	11	30	1:64	mA	-40°C		40 MIPS	
DC73g	11	30	1:128	mA				
DC70a	42	50	1:2	mA				
DC70f	26	30	1:64	mA	+25°C		40 MIPS	
DC70g	25	30	1:128	mA				
DC71a	41	50	1:2	mA		3.3V		
DC71f	25	30	1:64	mA	+85°C		40 MIPS	
DC71g	24	30	1:128	mA				
DC72a	42	50	1:2	mA				
DC72f	26	30	1:64	mA	+125°C	3.3V	40 MIPS	
DC72g	25	30	1:128	mA				

IDOZE is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading Note 1: and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDOZE measurements are as follows:

- Oscillator is configured in EC mode and external clock active, OSC1 is driven with external square wave from rail-to-rail with overshoot/undershoot < 250 mV
- · CLKO is configured as an I/O input pin in the Configuration word
- · All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- · No peripheral modules are operating; however, every peripheral is being clocked (defined PMDx bits are set to zero and unimplemented PMDx bits are set to one)
- CPU executing while (1) statement
- · JTAG is disabled
- 2: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated.



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TABLE 26-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) **DC CHARACTERISTICS** Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Ind $-40^{\circ}C \le TA \le +125^{\circ}C$ for E Typ⁽¹⁾ Characteristic Min Units Conditions Max Input Low Voltage I/O Pins 0.2 VDD V Vss

DIIO		101113	V 00		0.2 000	v	
DI15		MCLR	Vss	—	0.2 VDD	V	
DI16		I/O Pins with OSC1 or SOSCI	Vss	_	0.2 Vdd	V	
DI18		I/O Pins with I ² C™	Vss	—	0.3 VDD	V	SMBus disabled
DI19		I/O Pins with I ² C	Vss	—	0.8 V	V	SMBus enabled
	Vih	Input High Voltage					
DI20		I/O Pins Not 5V Tolerant ⁽⁴⁾ I/O Pins 5V Tolerant ⁽⁴⁾	0.7 VDD 0.7 VDD	_	Vdd 5.5	V V	
DI28		SDAx, SCLx	0.7 VDD	_	5.5	V	SMBus disabled
DI29		SDAx, SCLx	2.1	_	5.5	V	SMBus enabled
	ICNPU	CNx Pull-up Current					
DI30			50	250	400	μA	VDD = 3.3V, VPIN = VSS
	lı∟	Input Leakage Current ^(2,3)					
D150		I/O Pins 5V Tolerant ⁽⁴⁾	_	—	±2	μA	$\label{eq:VSS} \begin{split} &V{\sf SS} \leq V{\sf PIN} \leq V{\sf DD}, \\ &P{\sf in \ at \ high-impedance} \end{split}$
DI51		I/O Pins Not 5V Tolerant ⁽⁴⁾	—	_	±1	μA	$Vss \le VPIN \le VDD$, Pin at high-impedance, $-40^{\circ}C \le TA \le +85^{\circ}C$
DI51a		I/O Pins Not 5V Tolerant ⁽⁴⁾	—	—	±2	μA	Shared with external reference pins, -40°C \leq TA \leq +85°C
DI51b		I/O Pins Not 5V Tolerant ⁽⁴⁾	_	—	±3.5	μA	$Vss \le VPIN \le VDD$, Pin at high-impedance, -40°C \le TA \le +125°C
DI51c		I/O Pins Not 5V Tolerant ⁽⁴⁾	_	—	±8	μA	Analog pins shared with external reference pins, $-40^{\circ}C \le TA \le +125^{\circ}C$
DI55		MCLR	—	—	±2	μA	$Vss \leq V \text{PIN} \leq V \text{DD}$
D156		OSC1	_	—	±2	μA	$\label{eq:VSS} \begin{split} &V\text{SS} \leq V\text{PIN} \leq V\text{DD}, \\ &X\text{T and HS modes} \end{split}$

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

- **3:** Negative current is defined as current sourced by the pin.
- 4: See "Pin Diagrams" for a list of 5V tolerant pins.
- 5: VIL source < (VSS 0.3). Characterized but not tested.
- 6: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.
- 7: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
- 8: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.
- Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted pro-9: vided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

Param

No.

DI10

Symbol

VIL



TABLE 26-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINU

DC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for $-40^{\circ}C \le TA \le +125^{\circ}C$ for $-40^{\circ}C \le -125^{\circ}C$ for<						
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Cond指ions面的二维码图案,加我为			
DI60a	licl	Input Low Injection Current	0	_	₋₅ (5,8)	mA	All pins except VDD, Vss, AVDD, AVss, MCLR, VcAP, SOSCI, SOSCO, and RB11			
DI60b	Іісн	Input High Injection Current	0	_	+5(6,7,8)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, SOSCI, SOSCO, RB11, and all 5V tolerant pins ⁽⁷⁾			
DI60c	∑lict	Total Input Injection Current (sum of all I/O and control pins)	₋₂₀ (9)	_	+20(9)	mA	Absolute instantaneous sum of all \pm input injection currents from all I/O pins (IICL + IICH) $\leq \sum$ IICT			

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

- 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- **3:** Negative current is defined as current sourced by the pin.
- 4: See "Pin Diagrams" for a list of 5V tolerant pins.
- 5: VIL source < (Vss 0.3). Characterized but not tested.
- **6:** Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.
- 7: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
- 8: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.
- **9:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.



TABLE 26-10: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHA	ARACTER	Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for excendent						
Param No.	Symbol	Characteristic	Min	Тур	Мах	Units	Condition包上面的二维码图案,加我	
		Output Low Voltage I/O Pins: 2x Sink Driver Pins - All pins not defined by 4x or 8x driver pins	_	_	0.4	v	$IOL \leq 3 \text{ mA}, \text{ VDD} = 3.3 \text{ V}$	
DO10	Vol	Output Low Voltage I/O Pins: 4x Sink Driver Pins - RA2, RA3, RA9, RA10, RA14, RA15, RB0, RB1, RB11, RF4, RF5, RG2, RG3	_	_	0.4	v	IOL \leq 6 mA, VDD = 3.3V	
		Output Low Voltage I/O Pins: 8x Sink Driver Pins - OSC2, CLKO, RC15	_	_	0.4	v	IOL \leq 10 mA, VDD = 3.3V	
		Output High Voltage I/O Pins: 2x Source Driver Pins - All pins not defined by 4x or 8x driver pins	2.4	_	_	v	$IOL \ge -3 \text{ mA}, \text{ VDD} = 3.3 \text{V}$	
DO20 Voh	Voн	Output High Voltage I/O Pins: 4x Source Driver Pins - RA2, RA3, RA9, RA10, RA14, RA15, RB0, RB1, RB11, RF4, RF5, RG2, RG3	2.4	_	_	v	$IOL \ge -6 \text{ mA}, \text{ VDD} = 3.3 \text{V}$	
		Output High Voltage I/O Pins: 8x Source Driver Pins - OSC2, CLKO, RC15	2.4	_	_	v	IoL ≥ -10 mA, VDD = 3.3V	
		Output High Voltage I/O Pins:	1.5	_	_		IOH ≥ -6 mA, VDD = 3.3V See Note 1	
		2x Source Driver Pins - All pins not defined by 4x or 8x driver pins	2.0	_	_	v	IOH ≥ -5 mA, VDD = 3.3V See Note 1	
			3.0	_	_		IOH ≥ -2 mA, VDD = 3.3V See Note 1	
DO20A Voh1		Output High Voltage 4x Source Driver Pins - RA2, RA3,	1.5	_	_		IOH ≥ -12 mA, VDD = 3.3V See Note 1	
	RA9, RA10, RA14, RA15, RB0, RB1, RB11, RF4, RF5, RG2, RG3	2.0	_	_	v	IOH ≥ -11 mA, VDD = 3.3V See Note 1		
			3.0	_	_		IOH ≥ -3 mA, VDD = 3.3V See Note 1	
		Output High Voltage 8x Source Driver Pins - OSC2,	1.5	_	_		IOH ≥ -16 mA, VDD = 3.3V See Note 1	
		CLKO, RC15	2.0		_	V	IOH ≥ -12 mA, VDD = 3.3V See Note 1	
			3.0	_			IOH ≥ -4 mA, VDD = 3.3V See Note 1	

Note 1: Parameters are characterized, but not tested.



TABLE 26-11: ELECTRICAL CHARACTERISTICS: BOR

DC CHA	DC CHARACTERISTICS		(unless otherwis	$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Param.	Symbol	Characteris	stic ⁽¹⁾	Min ⁽¹⁾	Тур	Max ⁽¹⁾	Units	Gonditions,	加我为朋友。
BO10	VBOR	BOR Event on VDD Trans	sition High-to-Low	2.40		2.55	V	Vdd	
Mate 4	Deve			- + + +	·	for a la sulta a			

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

TABLE 26-12: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHA	DC CHARACTERISTICS			-	vise state	ponditions: 3.0V to 3.6V ed) $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended			
Param No.	Symbol	Characteristic	Min Typ ⁽¹⁾ Max U		Units	Conditions			
		Program Flash Memory							
D130	Eр	Cell Endurance	10,000	—	—	E/W	—		
D131	Vpr	VDD for Read	VMIN	—	3.6	V	Vмın = Minimum operating voltage		
D132b	VPEW	VDD for Self-Timed Write	VMIN	—	3.6	V	Vмın = Minimum operating voltage		
D134	TRETD	Characteristic Retention	20	—		Year	Provided no other specifications are violated		
D135	IDDP	Supply Current during Programming	—	10		mA	_		
D136a	Trw	Row Write Time	1.32	—	1.74	ms	Trw = 11064 FRC cycles, TA = +85°C, see Note 2		
D136b	Trw	Row Write Time	1.28	—	1.79	ms	Trw = 11064 FRC cycles, Ta = +150°C, see Note 2		
D137a	TPE	Page Erase Time	20.1	—	26.5	ms	TPE = 168517 FRC cycles, TA = +85°C, see Note 2		
D137b	TPE	Page Erase Time	19.5	—	27.3	ms	TPE = 168517 FRC cycles, TA = +150°C, see Note 2		
D138a	Tww	Word Write Cycle Time	42.3	—	55.9	μs	Tww = 355 FRC cycles, TA = +85°C, see Note 2		
D138b	Tww	Word Write Cycle Time	41.1	—	57.6	μs	Tww = 355 FRC cycles, TA = +150°C, see Note 2		

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

2: Other conditions: FRC = 7.37 MHz, TUN<5:0> = b '011111 (for Min), TUN<5:0> = b '100000 (for Max). This parameter depends on the FRC accuracy (see Table 26-19) and the value of the FRC Oscillator Tuning register (see Register 9-4). For complete details on calculating the Minimum and Maximum time, see Section 5.3 "Programming Operations".

TABLE 26-13: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

(unless	$\begin{array}{ll} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq Ta \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq Ta \leq +125^{\circ}C \mbox{ for Extended} \end{array}$										
Param.	Symbol	Characteristics	Min	Тур	Max	Units	Comments				
	- CEFC External Filter Capacitor Value 4.7 10 - μF Capacitor must be low series resistance (< 5 ohms)										

26.2 AC Characteristics and Timing Parameters

The information contained in this section defines dsPIC33FJXXXMCX06A/X08A/X10A AC characteristics and timing parameters.



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TABLE 26-14: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)
AC CHARACTERISTICS	$\begin{array}{rl} \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ -40^\circ C \leq TA \leq +125^\circ C \mbox{ for Extended} \\ \mbox{Operating voltage VDD range as described in Table 26-1.} \end{array}$

FIGURE 26-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

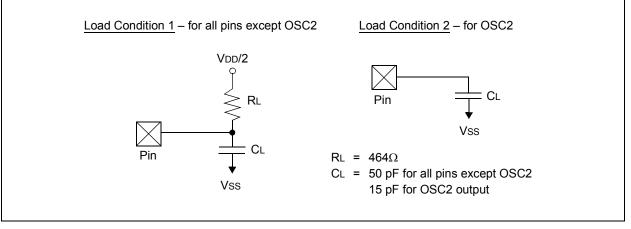


TABLE 26-15: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions
DO50	Cosc2	OSC2/SOSC2 Pin	_	_	15	pF	In XT and HS modes when external clock is used to drive OSC1
DO56	Сю	All I/O Pins and OSC2	—	_	50	pF	EC mode
DO58	Св	SCLx, SDAx		—	400	pF	In I ² C™ mode

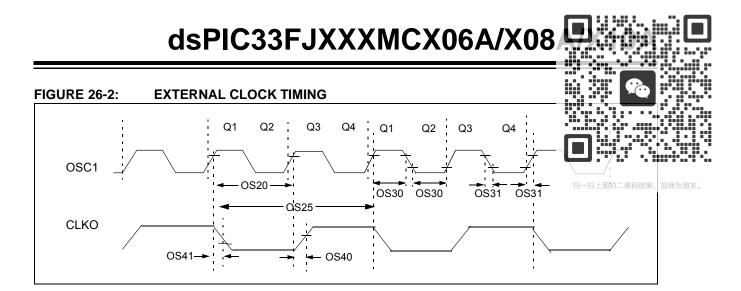


TABLE 26-16: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHA	RACTEF	RISTICS	$\begin{array}{llllllllllllllllllllllllllllllllllll$							
Param No.	Symb	Characteristic	Min	Typ ⁽¹⁾	Мах	Units	Conditions			
OS10	FIN	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	40	MHz	EC			
		Oscillator Crystal Frequency	3.5 10 —		10 40 33	MHz MHz kHz	XT HS SOSC			
OS20	Tosc	Tosc = 1/Fosc	12.5	—	DC	ns	_			
OS25	Тсү	Instruction Cycle Time ⁽²⁾	25		DC	ns	_			
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.375 x Tosc	—	0.625 x Tosc	ns	EC			
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	20	ns	EC			
OS40	TckR	CLKO Rise Time ⁽³⁾	—	5.2	_	ns	_			
OS41	TckF	CLKO Fall Time ⁽³⁾	—	5.2	—	ns	—			
OS42	Gм	External Oscillator Transconductance ⁽⁴⁾	14	16	18	mA/V	VDD = 3.3V, TA = +25°C			

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

2: Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.

- 3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.
- 4: Data for this parameter is preliminary. This parameter is characterized, but not tested in manufacturing.



TABLE 26-17: PLL CLOCK TIMING SPECIFICATIONS (VDD = 3.0V TO 3.6V)

Standard Operating Conditions: 3.0V to 3.6V

(unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C < TA \le +125^{\circ}C$ for Extended

				-40*	$C \leq IA \leq \cdot$	+125 01	for Extended	
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions ^{目上面的二维}	码图案
OS50	Fplli	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	0.8	_	8.0	MHz	ECPLL, HSPLL, XTPLL modes	
OS51	Fsys	On-Chip VCO System Frequency	100	—	200	MHz	_	
OS52	TLOCK	PLL Start-up Time (Lock Time)	0.9	1.5	3.1	ms	—	1
OS53	DCLK	CLKO Stability (Jitter)	-3.0	0.5	3.0	%	Measured over 100 ms period	

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

AC CHARACTERISTICS

2: These parameters are characterized by similarity but are not tested in manufacturing. This specification is based on clock cycle by clock cycle measurements. To calculate the effective jitter for individual time base or communication clocks used by peripherals use the formula:

Peripheral Clock Jitter = DCLK / $\sqrt{(Fosc/Peripheral bit rate clock)}$

Example Only: Fosc = 80 MHz, DCLK = 3%, SPI bit rate clock, (i.e. SCK), is 5 MHz

SPI SCK Jitter = [DCLK / \sqrt{80 MHz/5 MHz}] = [3%/\sqrt{16}] = [3% / 4] = 0.75%

TABLE 26-18: AC CHARACTERISTICS: INTERNAL FRC ACCURACY

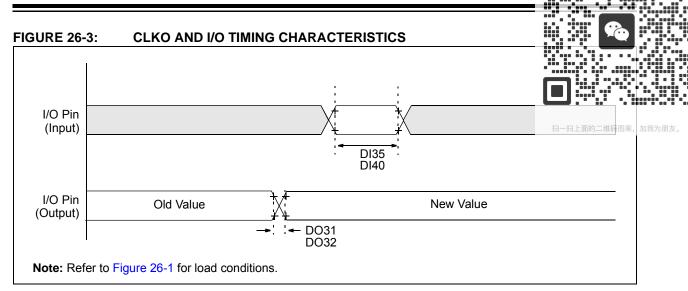
АС СНА	RACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended								
Param No.	Characteristic	Min	Тур	Max	Units Conditions						
	Internal FRC Accuracy @	FRC Fr	equency	= 7.37 N	IHz ⁽¹⁾						
F20a	FRC	-2	_	+2	%	$-40^{\circ}C \le TA \le +85^{\circ}C \qquad \text{VDD} = 3.0\text{-}3.6\text{V}$					
F20b	FRC -5 +5 % -40°C \leq TA \leq +125°C VDD = 3.0-3.6						VDD = 3.0-3.6V				

Note 1: Frequency calibrated at 25°C and 3.3V. TUN bits can be used to compensate for temperature drift.

TABLE 26-19: INTERNAL LPRC ACCURACY

AC CH	ARACTERISTICS		$\begin{array}{llllllllllllllllllllllllllllllllllll$								
Param No.	Characteristic	Min	Тур	Max	Units	Co	onditions				
	LPRC @ 32.768 kHz ⁽¹)									
F21a	LPRC	-30	—	+30	%	$-40^{\circ}C \le TA \le +85^{\circ}C \qquad \qquad$					
F21b	LPRC -35 - +35 % -40°C \leq TA \leq +125°C -										

Note 1: Change of LPRC frequency as VDD changes.



AC CHAR	ACTERISTI	CS	(unless other	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$							
Param No.	Symbol	Character	Characteristic			Max	Units	Conditions			
DO31	TIOR	Port Output Rise Tim	e	_	10	25	ns	—			
DO32	TIOF	Port Output Fall Time	9	_	10	25	ns	—			
DI35	TINP	INTx Pin High or Low	20		_	ns	—				
DI40	Trbp	CNx High or Low Tim	2		—	TCY	—				

TABLE 26-20: I/O TIMING REQUIREMENTS

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

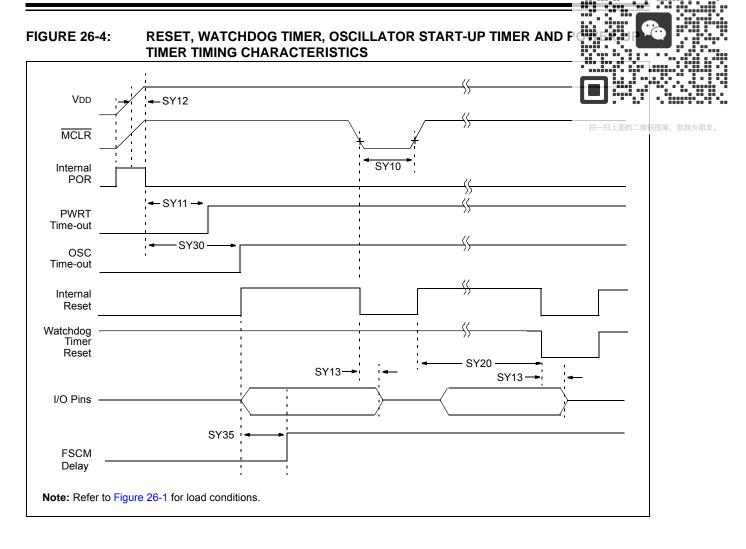




TABLE 26-21: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWE TIMING REQUIREMENTS

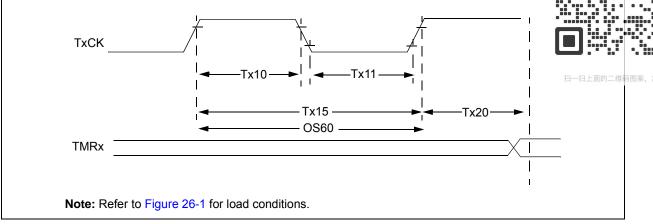
AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended								
Param No.	Symbol Characteristic		Min	Min Typ ⁽²⁾		Units	Conditions					
SY10	TMCL	MCLR Pulse Width (low)	2	_		μs	-40°C to +85°C					
SY11 SY12 SY13	Tpwrt Tpor Tioz	Power-up Timer Period Power-on Reset Delay I/O High-Impedance from MCLR Low or Watchdog		2 4 8 16 32 64 128 10 0.72	 30 1.2	ms μs μs	-40°C to +85°C User programmable -40°C to +85°C —					
SY20	Twdt1	Timer Reset Watchdog Timer Time-out Period	_			_	See Section 23.4 "Watchdog Timer (WDT)" and LPRC specification F21 (Table 26-19)					
SY30	Tost	Oscillator Start-up Timer Period	-	1024 Tosc	—	-	Tosc = OSC1 period					
SY35	TFSCM	Fail-Safe Clock Monitor Delay	-	500	900	μS	-40°C to +85°C					

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.



FIGURE 26-5: TIMER1, 2, 3, 4, 5, 6, 7, 8 AND 9 EXTERNAL CLOCK TIMING CHARACT



АС СНА	RACTERIST	ICS		$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$							
Param No.	Symbol	Charact	eristic		Min	Тур	Max	Units	Conditions		
TA10	ТтхН	TxCK High Time	Synchronous, no prescaler Synchronous, with prescaler		Tcy + 20	—	—	ns	Must also meet parameter TA15		
					(Tcy + 20)/N	—	—	ns	N = prescale value (1, 8, 64,		
			Asynchr	onous	20	_	_	ns	256)		
TA11	ΤτxL				(Tcy + 20)/N	—	—	ns	Must also meet parameter TA15		
			Synchronous, with prescaler		20	—	—	ns	N = prescale value (1, 8, 64,		
			Asynchr	onous	20	—	_	ns	256)		
TA15	ΤτχΡ	TxCK Input Period	Synchro no presc		2Tcy + 40	—	—	ns	—		
			Synchro with pres		Greater of: 40 ns or (2TcY + 40)/N	—	_	_	N = prescale value (1, 8, 64, 256)		
			Asynchr	onous	40	—	_	ns	—		
OS60	Ft1	SOSC1/T1CK Oscil Frequency Range (o by setting bit, TCS (oscillator e	enabled	DC		50	kHz	_		
TA20	TCKEXTMRL	Delay from Externa Edge to Timer Incre		lock	0.75 Tcy + 40		1.75 Tcy + 40	ns	_		

TABLE 26-22: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS⁽¹⁾

Note 1: Timer1 is a Type A.



TABLE 26-23: TIMER2, TIMER4, TIMER6 AND TIMER8 EXTERNAL CLOCK TIMING REQUIREMENTS

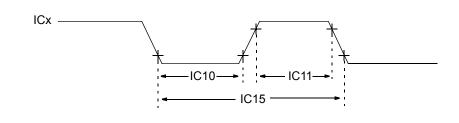
AC CHARACTERISTICS				(unles	ard Operating s otherwise s ting temperatu	tated) re -40°	°C≤ Ta≤	+85°C 1	
Param No.	Symbol	Charact	teristic		Min	Тур	Max	Units	Conditions
TB10	TtxH	TxCK High Time	Synchror	nous	Greater of	_		ns	Must also meet
			mode		20 or (TCY + 20)/N		_	ns	parameter TB15 N = prescale value (1, 8, 64, 256)
TB11	TtxL	TxCK Low Time	Synchror	nous	Greater of	_	_	ns	Must also meet
			mode		20 or (Tcy + 20)/N	—	—	ns	parameter TB15 N = prescale value (1, 8, 64, 256)
TB15	TtxP	TxCK Input Period	Synchror mode	nous	Greater of 40 or (2Tcy + 40)/N	_	_	ns	N = prescale value (1, 8, 64, 256)
TB20	TCKEXT- MRL	Delay from Extern Edge to Timer Inc		lock	0.75 Tcy + 40	_	1.75 Tcy + 40	ns	_

Note 1: These parameters are characterized, but are not tested in manufacturing.

TABLE 26-24:TIMER3, TIMER5, TIMER7 AND TIMER9 EXTERNAL CLOCK TIMING
REQUIREMENTS

AC CHARACTERISTICS				$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$						
Param No.SymbolCharacteristicMinTypM							Мах	Units	Conditions	
TC10	TtxH	TxCK High Time	Synchro	nous	Тсү + 20	—	_	ns	Must also meet parameter TC15	
TC11	TtxL	TxCK Low Time	Synchro	nous	Tcy + 20	—	—	ns	Must also meet parameter TC15	
TC15	TtxP	TxCK Input Period	Synchro with pre		2 Tcy + 40	-	—	ns	N = prescale value (1, 8, 64, 256)	
TC20 TCKEXTMRL Delay from External TxCK CI Edge to Timer Increment					0.75 Tcy + 40	—	1.75 Tcy + 40		—	

FIGURE 26-6: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS





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Note: Refer to Figure 26-1 for load conditions.

TABLE 26-25: INPUT CAPTURE TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$							
Param No.	Symbol	Characte	ristic ⁽¹⁾	tic ⁽¹⁾ Min Max Un						
IC10	TccL	ICx Input Low Time	No prescaler	0.5 Tcy + 20	_	ns	—			
			With prescaler	10	_	ns				
IC11	TccH	ICx Input High Time	No prescaler	0.5 Tcy + 20	—	ns	—			
			With prescaler	10	_	ns				
IC15	TccP	ICx Input Period		(Tcy + 40)/N	—	ns	N = prescale value (1, 4, 16)			

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 26-7: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS

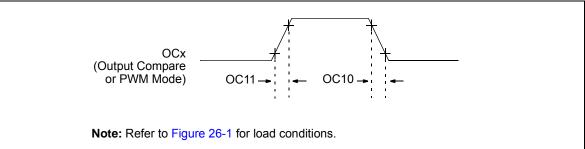


TABLE 26-26: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$						
Param No.	Symbol	Characteristic ⁽¹⁾	Min Typ Max Units Conditions						
OC10	TccF	OCx Output Fall Time	_	_	_	ns	See parameter D032		
OC11	TccR	OCx Output Rise Time	— — ns See parameter D031						

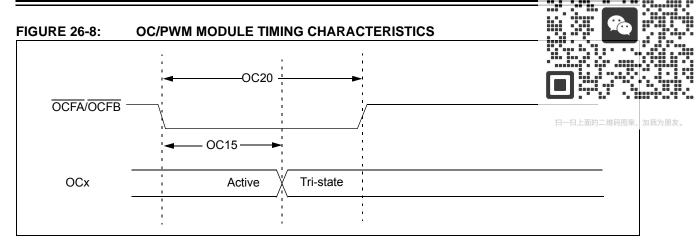


TABLE 26-27: SIMPLE OC/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$						
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур	Max	Units	Conditions		
OC15	Tfd	Fault Input to PWM I/O Change	_	_	Tcy + 20	ns	_		
OC20	TFLT	Fault Input Pulse Width	Tcy + 20		—	ns	—		

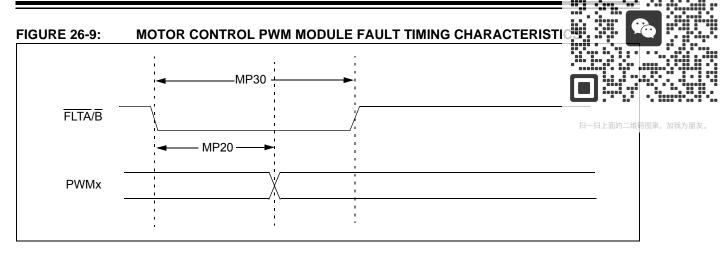


FIGURE 26-10: MOTOR CONTROL PWM MODULE TIMING CHARACTERISTICS

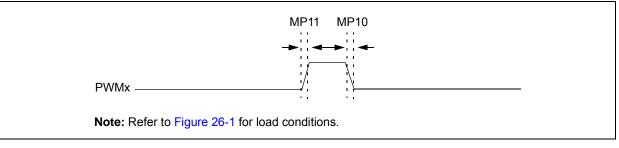


TABLE 26-28: MOTOR CONTROL PWM MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур	Max	Units	Conditions	
MP10	TFPWM	PWM Output Fall Time	—		_	ns	See parameter D032	
MP11	TRPWM	PWM Output Rise Time	_	—	—	ns	See parameter D031	
MP20	Tfd	Fault Input ↓ to PWM I/O Change	_	_	50	ns		
MP30	Tfh	Minimum Pulse Width	50	_		ns	—	

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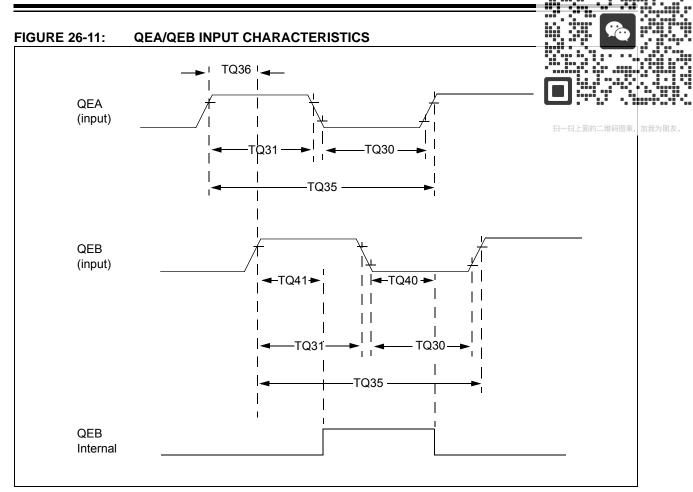


TABLE 26-29: QUADRATURE DECODER TIMING REQUIREMENTS

AC CHARACTERISTICS			(unle	dard Operating ss otherwise s ating temperatu	stated) re -40°(C ≤ TA ≤ ·	to 3.6V +85°C for Industrial 125°C for Extended
Param No.	Symbol	Characteristic ⁽¹⁾		Тур ⁽²⁾	Max	Units	Conditions
TQ30	TQUL	Quadrature Input Low Time		6 Tcy	—	ns	
TQ31	ΤουΗ	Quadrature Input High Time		6 Tcy	_	ns	—
TQ35	TQUIN	Quadrature Input Period		12 TCY	_	ns	—
TQ36	TQUP	Quadrature Phase Period		3 Tcy	_	ns	_
TQ40	TQUFL	Filter Time to Recognize Low with Digital Filter	v	3 * N * Tcy	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 3)
TQ41	TQUFH	Filter Time to Recognize Hig with Digital Filter	h	3 * N * Tcy	_	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 3)

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

3: N = Index Channel Digital Filter Clock Divide Select bits. Refer to **Section 15. "Quadrature Encoder Interface (QEI)"** (DS70208) in the "*dsPIC33F/PIC24H Family Reference Manual*".

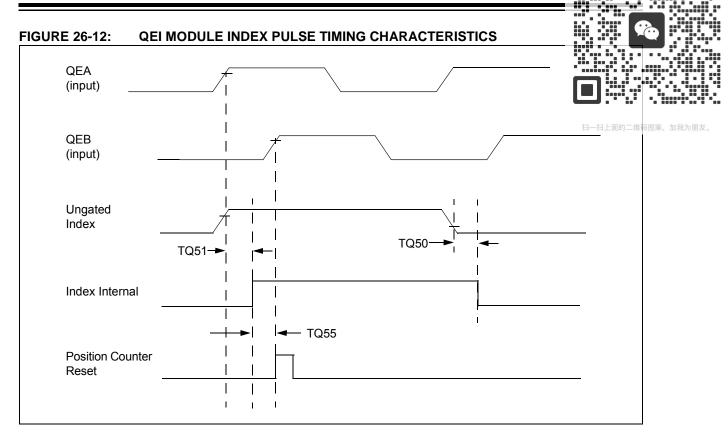


TABLE 26-30: QEI INDEX PULSE TIMING REQUIREMENTS

AC CHA	AC CHARACTERISTICS) 40°C ≤ T.	A≤ +85°	.6V C for Industrial C for Extended
Param No.	Symbol	Characteristic	. ⁽¹⁾	Min	Max	Units	Conditions
TQ50	TqiL	Filter Time to Recognize with Digital Filter	Low	3 * N * Tcy		ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 2)
TQ51	TqiH	Filter Time to Recognize with Digital Filter	High	3 * N * Tcy	_	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 2)
TQ55	Tqidxr	Index Pulse Recognized Counter Reset (ungated		3 TCY	_	ns	_

Note 1: These parameters are characterized but not tested in manufacturing.

2: Alignment of index pulses to QEA and QEB is shown for position counter Reset timing only. Shown for forward direction only (QEA leads QEB). Same timing applies for reverse direction (QEA lags QEB) but index pulse recognition occurs on falling edge.

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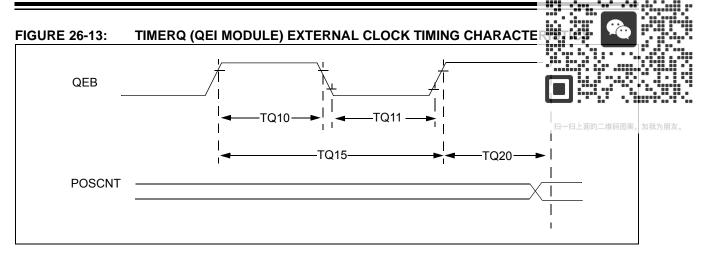


TABLE 26-31: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) **AC CHARACTERISTICS** Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial -40°C \leq TA \leq +125°C for Extended Param Characteristic⁽¹⁾ Symbol Units Conditions Min Тур Max No. TQ10 TtQH **TQCK High Time** Synchronous, TCY + 20 Must also meet ns with prescaler parameter TQ15 TQ11 TtQL **TQCK Low Time** Synchronous, TCY + 20 Must also meet ns with prescaler parameter TQ15 TQ15 TtQP **TQCP** Input Synchronous, 2 * TCY + 40 ns ____ ____ ____ Period with prescaler TQ20 **TCKEXTMRL** Delay from External TxCK Clock 1.5 TCY 0.5 TCY Edge to Timer Increment



TABLE 26-32: SPIX MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARACTERISTICS			Standard Operating (unless otherwise s Operating temperation				
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	СКР	扫 一系队员 的二维码	③ 图案,加我为朋友。
15 MHz	Table 26-33	—	—	0,1	0,1	0,1	
10 MHz	—	Table 26-34	—	1	0,1	1	
10 MHz	—	Table 26-35	—	0	0,1	1	
15 MHz	—	—	Table 26-36	1	0	0	
11 MHz	_	_	Table 26-37	1	1	0]
15 MHz	_	—	Table 26-38	0	1	0]
11 MHz	_	_	Table 26-39	0	0	0]

FIGURE 26-14: SPIX MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY CKE = 0) TIMING CHARACTERISTICS

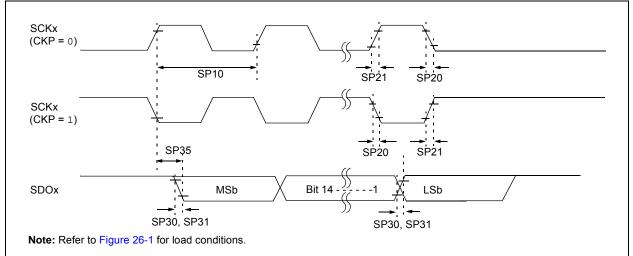
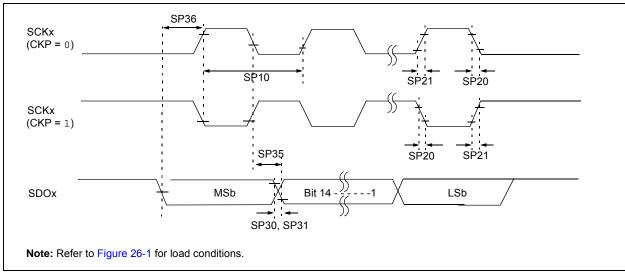


FIGURE 26-15: SPIX MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY CKE = 1) TIMING CHARACTERISTICS



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TABLE 26-33: SPIX MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING RE

АС СНА	AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}$ $-40^{\circ}C \le TA \le +12^{\circ}$						
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур ⁽²⁾	Max	Units	Conditions维码图案,加我为			
SP10	TscP	Maximum SCK Frequency	—	_	15	MHz	See Note 3			
SP20	TscF	SCKx Output Fall Time	-	—	—	ns	See parameter DO32 and Note 4			
SP21	TscR	SCKx Output Rise Time	_	—	—	ns	See parameter DO31 and Note 4			
SP30	TdoF	SDOx Data Output Fall Time	_	—	_	ns	See parameter DO32 and Note 4			
SP31	TdoR	SDOx Data Output Rise Time	_	_	_	ns	See parameter DO31 and Note 4			
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	_			
SP36	TdiV2scH, TdiV2scL	SDOx Data Output Setup to First SCKx Edge	30		_	ns	_			

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

3: The minimum clock period for SCKx is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

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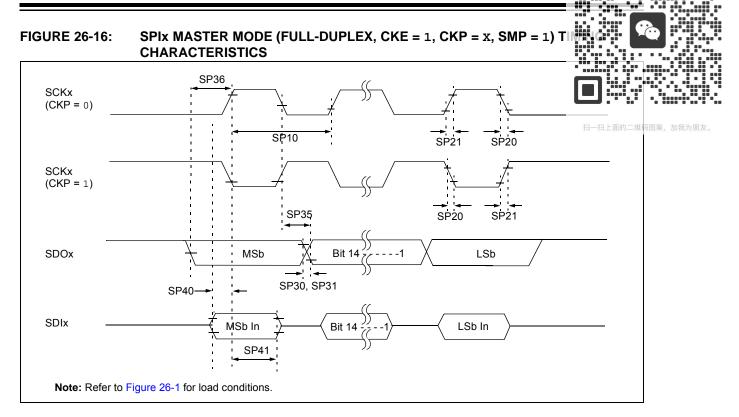


TABLE 26-34:SPIX MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING
REQUIREMENTS

АС СНА	RACTERIST	(unless c	Operatin otherwise g temperat	stated) ture -40	°C ≤ Ta ≤	/ to 3.6V +85°C for Industrial +125°C for Extended	
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур ⁽²⁾	Max	Units	Conditions
SP10	TscP	Maximum SCK Frequency	—	_	10	MHz	See Note 3
SP20	TscF	SCKx Output Fall Time	—	—	_	ns	See parameter DO32 and Note 4
SP21	TscR	SCKx Output Rise Time	—	—	_	ns	See parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	_	ns	See parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	-	—	ns	See parameter DO31 and Note 4
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	—
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—		ns	_
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_		ns	_
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

- **3:** The minimum clock period for SCKx is 100 ns. The clock generated in Master mode must not violate this specification.
- **4:** Assumes 50 pF load on all SPIx pins.

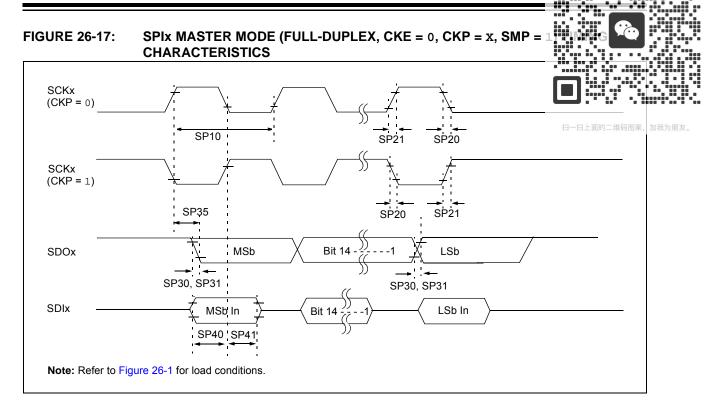


TABLE 26-35:SPIX MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING
REQUIREMENTS

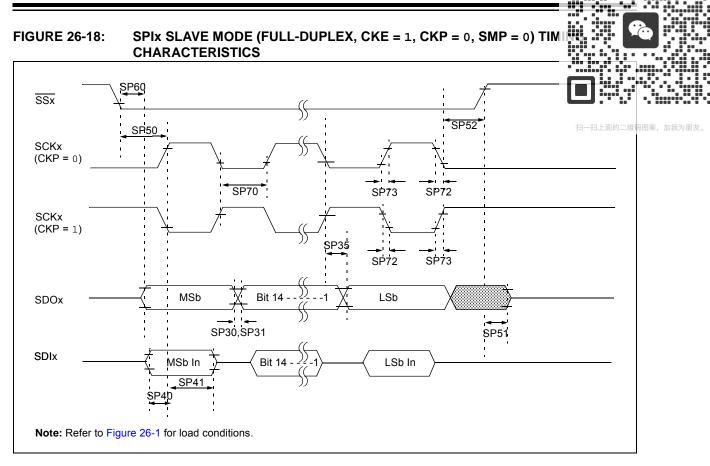
АС СНА	RACTERIST	(unless o	Operatin therwise temperat	stated) ture -40	°C ≤ Ta ≤	/ to 3.6V +85°C for Industrial +125°C for Extended	
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур ⁽²⁾	Max	Units	Conditions
SP10	TscP	Maximum SCK Frequency	_	-	10	MHz	-40°C to +125°C and see Note 3
SP20	TscF	SCKx Output Fall Time	_	—	_	ns	See parameter DO32 and Note 4
SP21	TscR	SCKx Output Rise Time	_	—	_	ns	See parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	_	—	_	ns	See parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	_	-	_	ns	See parameter DO31 and Note 4
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	_
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	_	ns	_
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—		ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30			ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

3: The minimum clock period for SCKx is 100 ns. The clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.



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TABLE 26-36: SPIX SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIM REQUIREMENTS



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AC CHA	ARACTERIS	FICS	Standard Op (unless othe Operating ter	rwise st	ated) e -40°	C ≤ TA ≤	+85° C industial +125°C for Extended
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур ⁽²⁾	Max	Units	扫一扫上面的二维码图案,为 Conditions
SP70	TscP	Maximum SCK Input Frequency	—	—	15	MHz	See Note 3
SP72	TscF	SCKx Input Fall Time	—	_		ns	See parameter DO32 and Note 4
SP73	TscR	SCKx Input Rise Time	—	—	_	ns	See parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	—	_	ns	See parameter DO31 and Note 4
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	_
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	_	ns	_
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	_	ns	_
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	_
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx \uparrow or SCKx Input	120	—	_	ns	_
SP51	TssH2doZ	SSx	10	—	50	ns	-
SP52	TscH2ssH TscL2ssH	SSx after SCKx Edge	1.5 TCY + 40	_	_	ns	See Note 4
SP60	TssL2doV	SDOx Data Output Valid after SSx Edge	—	—	50	ns	—

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

3: The minimum clock period for SCKx is 66.7 ns. Therefore, the SCK clock generated by the Master must not violate this specificiation.

4: Assumes 50 pF load on all SPIx pins.

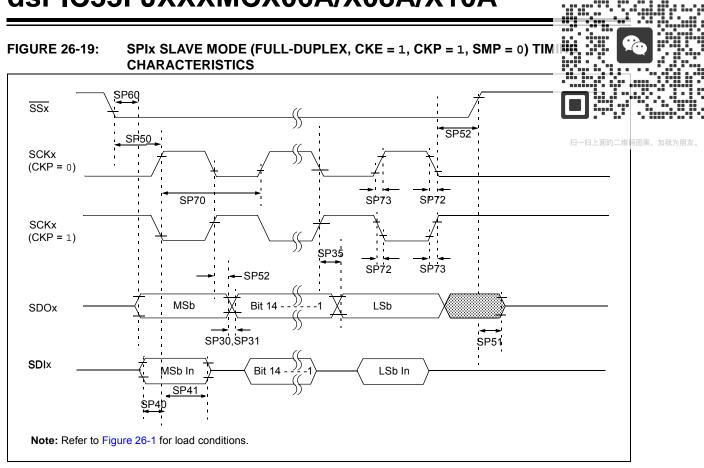


TABLE 26-37:SPIX SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TINREQUIREMENTS



AC CHA	ARACTERIS	TICS	Standard Operating Conditions: 2.4V to 3(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}$ $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extend						
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур ⁽²⁾	Max	Units	日一月上面的二维码图案,加 Conditions		
SP70	TscP	Maximum SCK Input Frequency	_		11	MHz	See Note 3		
SP72	TscF	SCKx Input Fall Time	—	_	_	ns	See parameter DO32 and Note 4		
SP73	TscR	SCKx Input Rise Time	—	_	_	ns	See parameter DO31 and Note 4		
SP30	TdoF	SDOx Data Output Fall Time	—	_	_	ns	See parameter DO32 and Note 4		
SP31	TdoR	SDOx Data Output Rise Time	—		-	ns	See parameter DO31 and Note 4		
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	—		
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	_	_	ns	—		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30			ns	—		
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	_	_	ns	_		
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx \uparrow or SCKx Input	120	_	-	ns	_		
SP51	TssH2doZ	SSx	10	_	50	ns	—		
SP52	TscH2ssH TscL2ssH	SSx after SCKx Edge	1.5 TCY + 40	_	_	ns	See Note 4		
SP60	TssL2doV	SDOx Data Output Valid after SSx Edge	—	_	50	ns	-		

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

3: The minimum clock period for SCKx is 91 ns. Therefore, the SCK clock generated by the Master must not violate this specificiation.

4: Assumes 50 pF load on all SPIx pins.

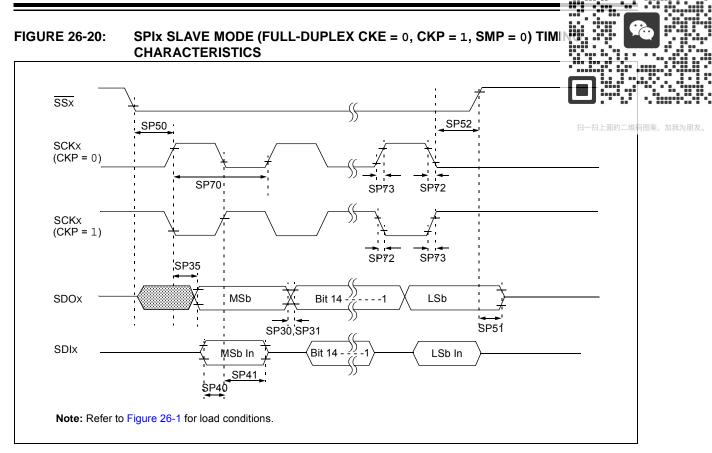


TABLE 26-38: SPIX SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIN REQUIREMENTS



AC CHA	ARACTERIS	TICS	Standard Op (unless othe Operating ter	rwise st	ated) e -40°	°C ≤ TA ≤	+85°C for Extended
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур ⁽²⁾	Max	Units	日一日上面的一堆码图案, Conditions
SP70	TscP	Maximum SCK Input Frequency	_		15	MHz	See Note 3
SP72	TscF	SCKx Input Fall Time	—			ns	See parameter DO32 and Note 4
SP73	TscR	SCKx Input Rise Time	—			ns	See parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—		_	ns	See parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—			ns	See parameter DO31 and Note 4
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	—
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30		_	ns	—
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_		ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30			ns	—
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx \uparrow or SCKx Input	120	Ι		ns	—
SP51	TssH2doZ	SSx	10	—	50	ns	-
SP52	TscH2ssH TscL2ssH	SSx after SCKx Edge	1.5 TCY + 40	_	_	ns	See Note 4

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

3: The minimum clock period for SCKx is 66.7 ns. Therefore, the SCK clock generated by the Master must not violate this specificiation.

4: Assumes 50 pF load on all SPIx pins.

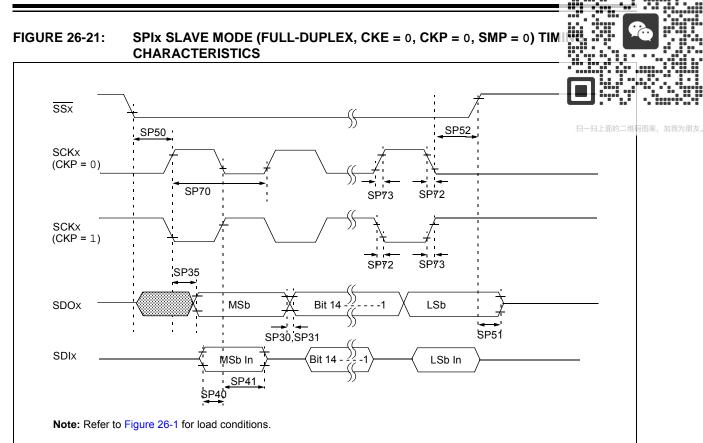


TABLE 26-39: SPIX SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIM REQUIREMENTS



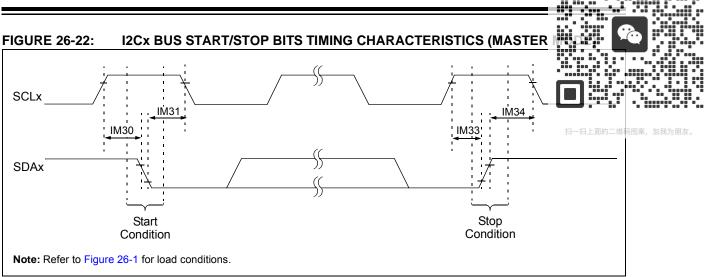
AC CHA	ARACTERIS	TICS	Standard Op (unless othe Operating ter	+85° C for Extended			
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур ⁽²⁾	Max	Units	日一日上面的一堆码图案, Conditions
SP70	TscP	Maximum SCK Input Frequency	_	_	11	MHz	See Note 3
SP72	TscF	SCKx Input Fall Time	—	_	_	ns	See parameter DO32 and Note 4
SP73	TscR	SCKx Input Rise Time	—	_	_	ns	See parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	_	_	ns	See parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	_	_	ns	See parameter DO31 and Note 4
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	—
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	_	ns	—
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_		ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	_	-	ns	—
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx \uparrow or SCKx Input	120	_	_	ns	_
SP51	TssH2doZ	SSx	10	—	50	ns	_
SP52	TscH2ssH TscL2ssH	SSx after SCKx Edge	1.5 TCY + 40	—	_	ns	See Note 4

Note 1: These parameters are characterized, but are not tested in manufacturing.

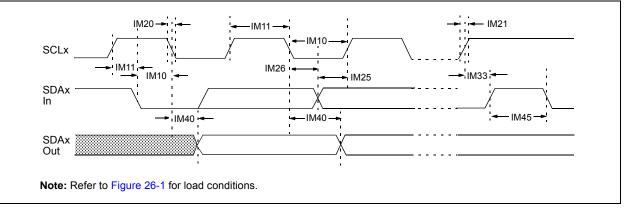
2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

3: The minimum clock period for SCKx is 91 ns. Therefore, the SCK clock generated by the Master must not violate this specificiation.

4: Assumes 50 pF load on all SPIx pins.







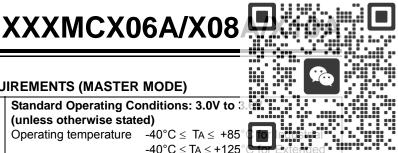


TABLE 26-40: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

Γ

AC CHA	ARACTER	ISTICS		Standard Operation (unless otherwise Operating tempera	e stated) iture -40	$0^{\circ}C \le TA \le$ $0^{\circ}C \le TA \le$	≤ +85° (fo)
Param No.	Symbol	Charact	teristic	Min ⁽¹⁾	Мах	Units	Conditions ^{维码图案,}
IM10	TLO:SCL	Clock Low Time	100 kHz mode	Tcy/2 (BRG + 1)	—	μs	—
			400 kHz mode	TCY/2 (BRG + 1)	_	μS	—
			1 MHz mode ⁽²⁾	TCY/2 (BRG + 1)	_	μS	—
IM11	THI:SCL	Clock High Time	100 kHz mode	TCY/2 (BRG + 1)	_	μS	—
			400 kHz mode	TCY/2 (BRG + 1)	_	μS	—
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	—	μS	—
IM20	TF:SCL	SDAx and SCLx	100 kHz mode	—	300	ns	CB is specified to be
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF
			1 MHz mode ⁽²⁾	—	100	ns	
IM21	TR:SCL	SDAx and SCLx	100 kHz mode	_	1000	ns	CB is specified to be
		Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF
			1 MHz mode ⁽²⁾	_	300	ns	
IM25	TSU:DAT	Data Input	100 kHz mode	250	_	ns	_
		Setup Time	400 kHz mode	100		ns	
			1 MHz mode ⁽²⁾	40	—	ns	
M26	THD:DAT	Data Input	100 kHz mode	0	—	μS	_
		Hold Time	400 kHz mode	0	0.9	μS	
			1 MHz mode ⁽²⁾	0.2	—	μS	
IM30	TSU:STA	Start Condition	100 kHz mode	Tcy/2 (BRG + 1)	—	μS	Only relevant for
		Setup Time	400 kHz mode	Tcy/2 (BRG + 1)	—	μS	Repeated Start
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	—	μS	condition
IM31	THD:STA	Start Condition	100 kHz mode	Tcy/2 (BRG + 1)	_	μs	After this period the
		Hold Time	400 kHz mode	Tcy/2 (BRG + 1)	_	μS	first clock pulse is
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	_	μs	generated
IM33	Tsu:sto	Stop Condition	100 kHz mode	Tcy/2 (BRG + 1)	—	μS	_
		Setup Time	400 kHz mode	Tcy/2 (BRG + 1)	—	μS	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	—	μS	
IM34	THD:STO	Stop Condition	100 kHz mode	Tcy/2 (BRG + 1)	—	ns	_
		Hold Time	400 kHz mode	Tcy/2 (BRG + 1)	—	ns	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)		ns	
IM40	TAA:SCL	Output Valid	100 kHz mode	_	3500	μS	_
		From Clock	400 kHz mode	—	1000	μS	_
			1 MHz mode ⁽²⁾	_	400	μS	_
M45	TBF:SDA	Bus Free Time	100 kHz mode	4.7		μs	Time the bus must be
			400 kHz mode	1.3	_	μ S	free before a new
			1 MHz mode ⁽²⁾	0.5		μ S	transmission can start
M50	Св	Bus Capacitive L		_	400	pF	
IM51	TPGD	Pulse Gobbler De		65	390	ns	See Note 3

Note 1: BRG is the value of the I²C[™] Baud Rate Generator. Refer to Section 19. "Inter-Integrated Circuit (I²C[™])" (DS70195) in the "dsPIC33F/PIC24H Family Reference Manual".

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: Typical value for this parameter is 130 ns.

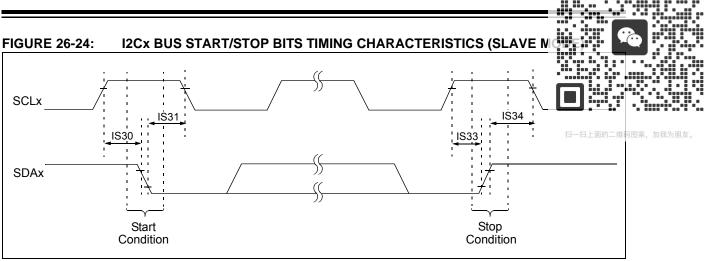


FIGURE 26-25: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)

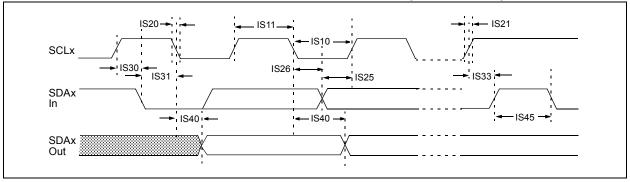




TABLE 26-41: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHA	RACTERIS		Standard Op (unless othe Operating ten	rwise st	ated) ə -40°	$C \le TA \le +8$ $C \le TA \le +12$ $C \le TA \le +12$	
Param No. Symbol Characteristic		Min	Max Units		Condition 理的图案		
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7		μS	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	_	μS	Device must operate at a minimum of 10 MHz
			1 MHz mode ⁽¹⁾	0.5	_	μS	—
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0		μS	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	_	μS	Device must operate at a minimum of 10 MHz
			1 MHz mode ⁽¹⁾	0.5	_	μs	—
IS20	TF:SCL	SDAx and SCLx	100 kHz mode	—	300	ns	CB is specified to be from
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF
			1 MHz mode ⁽¹⁾	—	100	ns	
S21	TR:SCL	SDAx and SCLx	100 kHz mode	l —	1000	ns	CB is specified to be from
		Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF
			1 MHz mode ⁽¹⁾	_	300	ns	
S25	TSU:DAT	Data Input	100 kHz mode	250	_	ns	
		Setup Time	400 kHz mode	100		ns	1
			1 MHz mode ⁽¹⁾	100		ns	1
IS26	THD:DAT	Data Input	100 kHz mode	0		μs	
		Hold Time	400 kHz mode	0	0.9	μs	1
			1 MHz mode ⁽¹⁾	0	0.3	μS	1
S30	TSU:STA	Start Condition	100 kHz mode	4.7	_	μs	Only relevant for Repeated
		Setup Time	400 kHz mode	0.6	_	μS	Start condition
			1 MHz mode ⁽¹⁾	0.25	_	μs	1
IS31	THD:STA	Start Condition	100 kHz mode	4.0	_	μs	After this period, the first
		Hold Time	400 kHz mode	0.6	—	μs	clock pulse is generated
			1 MHz mode ⁽¹⁾	0.25	—	μS	
IS33	Tsu:sto	Stop Condition	100 kHz mode	4.7	—	μs	—
		Setup Time	400 kHz mode	0.6	_	μs	1
			1 MHz mode ⁽¹⁾	0.6	—	μs	1
IS34	THD:STO	Stop Condition	100 kHz mode	4000	—	ns	
		Hold Time	400 kHz mode	600	—	ns	1
			1 MHz mode ⁽¹⁾	250		ns	1
IS40	TAA:SCL	Output Valid	100 kHz mode	0	3500	ns	
		From Clock	400 kHz mode	0	1000	ns	1
			1 MHz mode ⁽¹⁾	0	350	ns	1
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	_	μs	Time the bus must be free
			400 kHz mode	1.3		μS	before a new transmission
			1 MHz mode ⁽¹⁾	0.5		μs	can start
IS50	Св	Bus Capacitive Lo			400	pF	

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

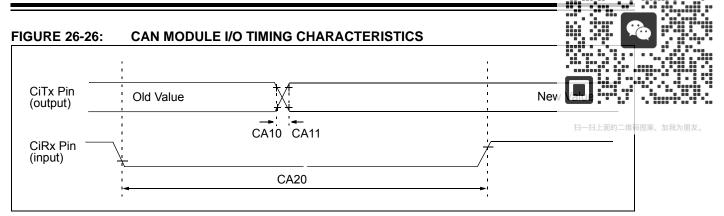


TABLE 26-42: ECAN™ TECHNOLOGY MODULE I/O TIMING REQUIREMENTS

AC CHARA	ACTERISTIC	S	(unless	d Operation otherwise ng temper	se stated) -40°C ≤ ⁻	3.0V to 3.6V TA \leq +85°C for Industrial TA \leq +125°C for Extended
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур	Max	Units	Conditions
CA10	TioF	Port Output Fall Time	_	_	_	ns	See parameter D032
CA11	TioR	Port Output Rise Time	—	_	_	ns	See parameter D031
CA20	Tcwf	Pulse Width to Trigger CAN Wake-up Filter	120	_	_	ns	—



TABLE 26-43: ADC MODULE SPECIFICATIONS

AC CH	ARACTER	RISTICS	(unless oth	nerwise	ture -40°C ≤	≤ Ta ≤ ·	/ to 3.6V +85°C for Incu	
Param No.	Symbol	Characteristic	Min.	Тур	Max.	Units	Cond記行力。 加加 Cond記 Cond記 Cond記 Cond記 Cond記 Cond記 Cond記 Cond記 Cond記 Cond記 Cond記 Cond記 Cond記 Cond記 Cond記 Cond記 Cond Cond Cond Cond Cond Cond Cond Cond	1我为朋友。
			Device	Suppl	/			
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 3.0	_	Lesser of VDD + 0.3 or 3.6	V	_	
AD02	AVss	Module Vss Supply	Vss – 0.3	_	Vss + 0.3	V	—	
			Reference	ce Inpu	ts			
AD05	Vrefh	Reference Voltage High	AVss + 2.5		AVdd	V	—	
AD05a			3.0		3.6	V	VREFH = AVDD VREFL = AVSS = 0	
AD06	VREFL	Reference Voltage Low	AVss	_	AVDD - 2.5	V	—	
AD06a			0	_	0	V	VREFH = AVDD VREFL = AVSS = 0	
AD07	VREF	Absolute Reference Voltage	2.5	_	3.6	V	VREF = VREFH - VREFL	
AD08	IREF	Current Drain	_		10	μA	ADC off	
AD08a	Iad	Operating Current	_	7.0 2.7	9.0 3.2	mA mA	10-bit ADC mode, see Note 1 12-bit ADC mode, see Note 1	
			Analog	g Input		•		
AD12	VINH	Input Voltage Range Vімн	VINL	—	Vrefh	V	This voltage reflects Sample and Hold Channels 0, 1, 2 and 3 (CH0-CH3), positive input	
AD13	VINL	Input Voltage Range Vın∟	Vrefl	_	AVss + 1V	V	This voltage reflects Sample and Hold Channels 0, 1, 2 and 3 (CH0-CH3), negative input	
AD17	Rin	Recommended Impedance of Analog Voltage Source			200 200	Ω Ω	10-bit ADC 12-bit ADC	



TABLE 26-44: ADC MODULE SPECIFICATIONS (12-BIT MODE)⁽¹⁾

AC CHA	RACTERIS	STICS	(unless	otherwi	se state	d) 40°C ≤ [·]	: 3.0V to 3.6V TA \leq +85°C for Indust TA \leq +125°C for Extended
Param No.	Symbol	Characteristic	Min.	Тур	Max.	Units	Conditions 扫一扫上面的二维
		ADC Accuracy (12-Bit Mo	de) – Mea	asureme	nts with	Externa	al Vref+/Vref-
AD20a	Nr	Resolution	1:	2 data bi	ts	bits	—
AD21a	INL	Integral Nonlinearity	-2	—	+2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD22a	DNL	Differential Nonlinearity	>-1	_	<1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD23a	Gerr	Gain Error	—	3.4	10	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD24a	EOFF	Offset Error	Q	0.9	5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD25a	—	Monotonicity	_	_	—	—	Guaranteed
		ADC Accuracy (12-Bit Mo	de) – Mea	asureme	ents with	Interna	I VREF+/VREF-
AD20b	Nr	Resolution	1:	2 data bi	ts	bits	—
AD21b	INL	Integral Nonlinearity	-2		+2	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD22b	DNL	Differential Nonlinearity	>-1		<1	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD23b	Gerr	Gain Error	—	10.5	20	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD24b	EOFF	Offset Error	—	3.8	10	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD25b		Monotonicity	—				Guaranteed
		Dynami	c Perforn	nance (1	2-Bit Mo	de)	
AD30a	THD	Total Harmonic Distortion	—	—	-75	dB	_
AD31a	SINAD	Signal to Noise and Distortion	68.5	69.5		dB	_
AD32a	SFDR	Spurious Free Dynamic Range	80		_	dB	_
AD33a	Fnyq	Input Signal Bandwidth			250	kHz	
AD34a	ENOB	Effective Number of Bits	11.09	11.3	—	bits	—

Note 1: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

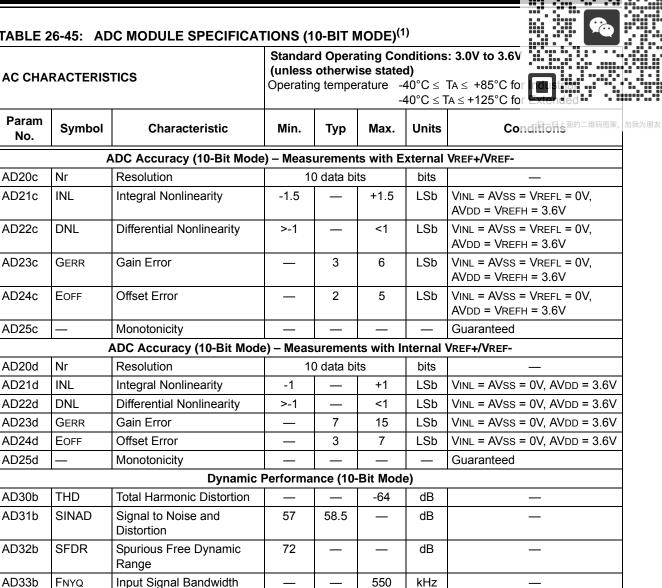


TABLE 26-45: ADC MODULE SPECIFICATIONS (10-BIT MODE)⁽¹⁾

Note 1: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

9.16

9.4

bits

Effective Number of Bits

ENOB

AD34b

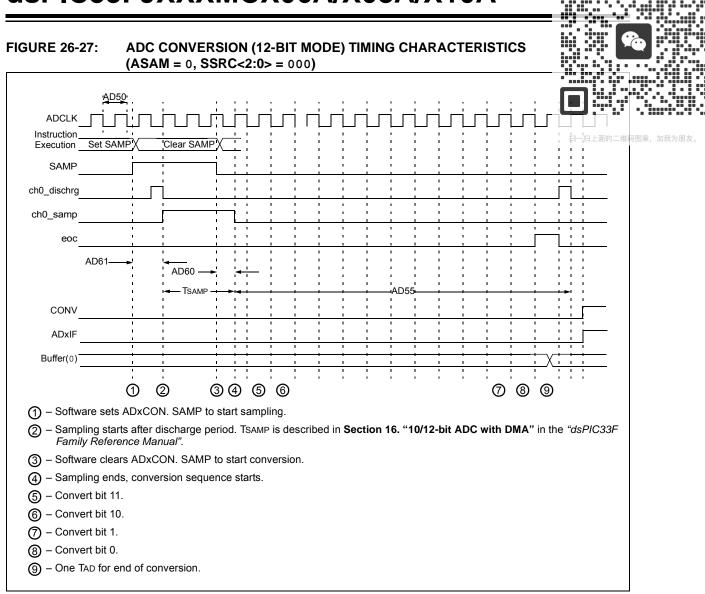




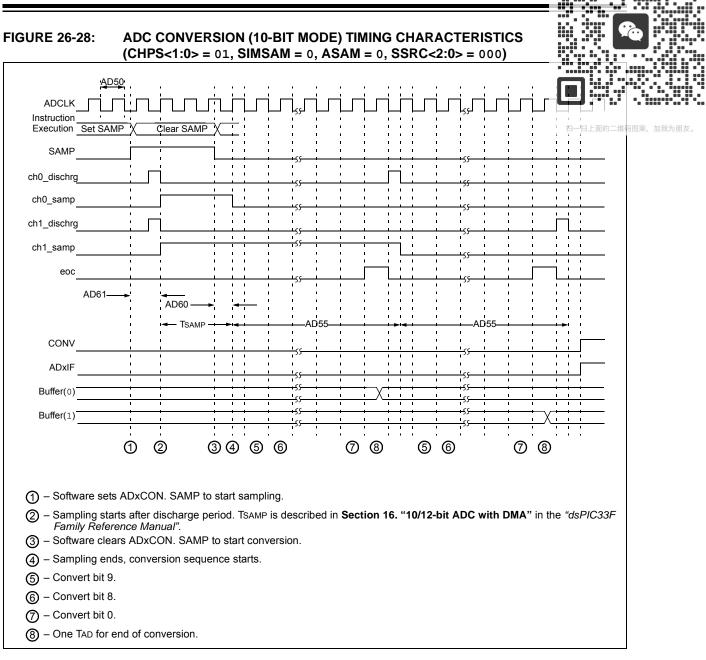
TABLE 26-46: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}$ $-40^{\circ}C \le TA \le +125^{\circ}$					
Param No.	Symbol	Characteristic	Min.	Тур	Max.	Units	Conditions维码图案,加	
		Cloc	k Paramet	ers	•			
AD50a	Tad	ADC Clock Period	117.6			ns	—	
AD51a	tRC	ADC Internal RC Oscillator Period	—	250	_	ns	_	
		Con	version R	ate				
AD55a	tCONV	Conversion Time	_	14 Tad			—	
AD56a	FCNV	Throughput Rate	_	_	500	ksps	—	
AD57a	TSAMP	Sample Time	3.0 Tad		_	—	—	
		Timin	g Parame	ters				
AD60a	tPCS	Conversion Start from Sample Trigger ^(1,2)	2.0 Tad	—	3.0 Tad	—	_	
AD61a	tPSS	Sample Start from Setting Sample (SAMP) bit ^(1,2)	2.0 TAD	—	3.0 Tad	—	_	
AD62a	tcss	Conversion Completion to Sample Start (ASAM = 1) ^(1,2)	—	0.5 TAD	—	—	_	
AD63a	tdpu	Time to Stabilize Analog Stage from ADC Off to ADC On ^(1,2,3)	—		20	μs	_	

Note 1: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

2: These parameters are characterized but not tested in manufacturing.

3: tDPU is the time required for the ADC module to stabilize when it is turned on (AD1CON1<ADON> = 1). During this time, the ADC result is indeterminate.



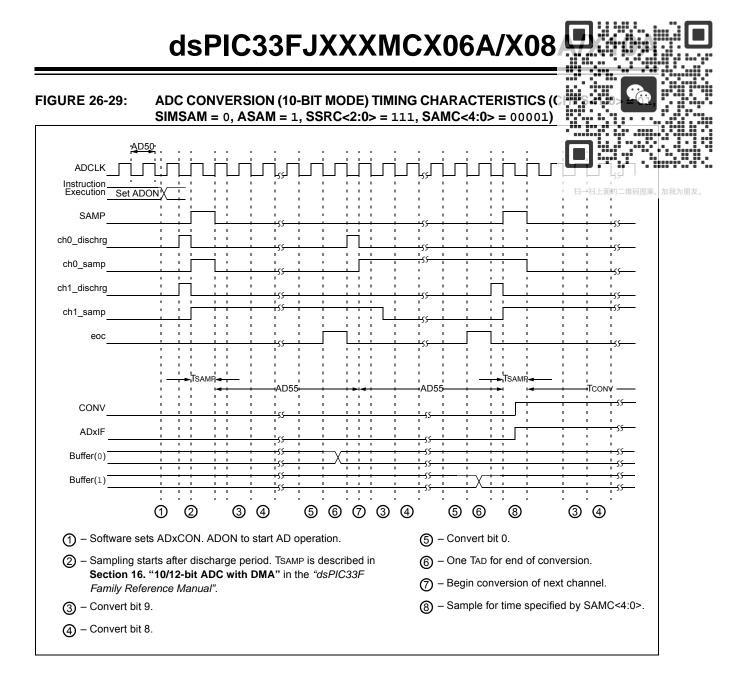




TABLE 26-47: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$					
Param No.	Symbol	Characteristic	Min.	Typ ⁽¹⁾	Max.	Units	Conditions 扫一扫上面的二维离图	
		Cloc	k Parame	ters				
AD50b	TAD	ADC Clock Period	76			ns	—	
AD51b	tRC	ADC Internal RC Oscillator Period	_	250	_	ns	—	
		Con	version F	late				
AD55b	tCONV	Conversion Time	_	12 TAD	_	_	_	
AD56b	FCNV	Throughput Rate	—		1.1	Msps	—	
AD57b	TSAMP	Sample Time	2 Tad		_		—	
		Timin	g Paramo	eters				
AD60b	tPCS	Conversion Start from Sample Trigger ^(1,2)	2.0 TAD	_	3.0 Tad	_	Auto-Convert Trigger (SSRC<2:0> = 111) not selected	
AD61b	tPSS	Sample Start from Setting Sample (SAMP) bit ^(1,2)	2.0 Tad	—	3.0 Tad	—	_	
AD62b	tcss	Conversion Completion to Sample Start (ASAM = 1) ^(1,2)	—	0.5 Tad	—	—	—	
AD63b	tdpu	Time to Stabilize Analog Stage from ADC Off to ADC On ^(1,3)			20	μS	—	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

3: tDPU is the time required for the ADC module to stabilize when it is turned on (AD1CON1<ADON> = 1). During this time, the ADC result is indeterminate.

TABLE 26-48: DMA READ/WRITE TIMING REQUIREMENTS

АС СНА	ARACTERISTICS	(unless o	Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended						
Param No.	Characteristic	Min.	Min. Typ Max. Units Condition						
DM1a	DMA Read/Write Cycle Time	_	_	2 Tcy	ns	This characteristic applies to dsPIC33FJ256MCX06A/X08A/X10A devices only.			
DM1b DMA Read/Write Cycle Time		—	—	1 Тсү	ns	This characteristic applies to all devices with the exception of the dsPIC33FJ256MCX06A/X08A/X10A.			

27.0 HIGH TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33FJXXXMCX06A/X08A/X10A electrical characte operating in an ambient temperature range of -40°C to +150°C.

The specifications between -40°C to +150°C are identical to those shown in **Section 26.0 "Electrical** for operation between -40°C to +125°C, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, parameter DC10 in methods Section 26.0 "Electrical Characteristics" is the Industrial and Extended temperature equivalent of HDC10.

Absolute maximum ratings for the dsPIC33FJXXXMCX06A/X08A/X10A high temperature devices are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings⁽¹⁾

Ambient temperature under bias ⁽⁴⁾	40°C to +150°C
Storage temperature	65°C to +160°C
Voltage on VDD with respect to Vss	0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to Vss ⁽⁵⁾	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when $VDD < 3.0V^{(5)}$	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when VDD $\geq 3.0 V^{(5)}$	0.3V to 5.6V
Voltage on VCAP with respect to Vss	2.25V to 2.75V
Maximum current out of Vss pin	60 mA
Maximum current into Vod pin ⁽²⁾	60 mA
Maximum junction temperature	+155°C
Maximum current sourced/sunk by any 2x I/O pin ⁽³⁾	2 mA
Maximum current sourced/sunk by any 4x I/O pin ⁽³⁾	4 mA
Maximum current sourced/sunk by any 8x I/O pin ⁽³⁾	8 mA
Maximum current sunk by all ports combined	10 mA
Maximum current sourced by all ports combined ⁽²⁾	10 mA

- **Note 1:** Stresses above those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.
 - 2: Maximum allowable current is a function of device maximum power dissipation (see Table 27-2).
 - **3:** Unlike devices at 125°C and below, the specifications in this section also apply to the CLKOUT, VREF+, VREF-, SCLx, SDAx, PGECx, and PGEDx pins.
 - 4: AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time from 125°C to 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.
 - 5: Refer to the "Pin Diagrams" section for 5V tolerant pins.





27.1 High Temperature DC Characteristics

TABLE 27-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range	Temperature Range	Max MIPS				
Characteristic	(in Volts)	(in °C)	dsPIC33FJXXXMCX06A/X08A/X10A				
HDC5	VBOR to 3.6V ⁽¹⁾	-40°C to +150°C	20 月二月上面的二维彩图案,加我为朋友。				

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules such as the ADC will have degraded performance. Device functionality is tested but not characterized. Refer to parameter BO10 in Table 26-11 for the minimum and maximum BOR values.

TABLE 27-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Тур	Max	Unit
High Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+155	°C
Operating Ambient Temperature Range	TA	-40	—	+150	°C
Power Dissipation: Internal chip power dissipation: $PINT = VDD x (IDD - \Sigma IOH)$ I/O Pin Power Dissipation: $I/O = \Sigma (\{VDD - VOH\} x IOH) + \Sigma (VOL x IOL)$	PD	I	Pint + Pi/c)	W
Maximum Allowed Power Dissipation	Pdmax	(Tj - Ta)/θja			W

TABLE 27-3: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARA	CTERISTIC	(unless c	Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature						
Parameter No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions		
Operating V	Voltage								
HDC10	Supply Voltage								
VDD — 3.0 3.3 3.6 V -40°C to +150°C									

TABLE 27-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACT	ERISTICS		(unless oth	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature				
Parameter No.	Typical	Мах	Units			Conditions		
Power-Down	Current (IPD)							
HDC60e	250	2000	μA	μA +150°C 3.3V Base Power-Down Current ^(1,3)				
Note 1: Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and								

Note 1: Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and pulled to Vss. WDT, etc., are all switched off, and VREGS (RCON<8>) = 1.

2: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

3: These currents are measured on the device containing the most memory in this family.

4: These parameters are characterized, but are not tested in manufacturing.

DC CHARACT	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$ for High T							
Parameter No.	Typical	Мах	Units					
Power-Down (Current (IPD)						扫一扫上面的二维码图案,	加我为朋友。
HDC61c	3	5	μA	+150°C	3.3V	Watchdog Timer	Current: ∆IwDT ^(2,4)	

Note 1: Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and pulled to Vss. WDT, etc., are all switched off, and VREGS (RCON<8>) = 1.

- 2: The ∆ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.
- 3: These currents are measured on the device containing the most memory in this family.
- 4: These parameters are characterized, but are not tested in manufacturing.

TABLE 27-5: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)

DC CHARA	Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature							
Parameter No.	Doze Ratio	Units	Conditions					
HDC72a	39	45	1:2	mA				
HDC72f	18	25	1:64	mA	+150°C 3.3V 20 MIPS			
HDC72g	18	25	1:128	mA				

Note 1: Parameters with Doze ratios of 1:2 and 1:64 are characterized, but are not tested in manufacturing.



图案,加我为朋友.

TABLE 27-6: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS Standard Operating Conditions: 3.0V to 3.0 (unless otherwise stated) DC CHARACTERISTICS Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}$ Temperature Symbol Characteristic Units Conditions Param. Min. Тур. Max. Output Low Voltage I/O Pins: $IOL \leq 1.8$ mA, VDD = 3.3V V 0.4 2x Sink Driver Pins - All pins not See Note 1 defined by 4x or 8x driver pins **Output Low Voltage** I/O Pins: $IOL \leq 3.6 \text{ mA}, \text{ VDD} = 3.3 \text{ V}$ HDO10 VOL 4x Sink Driver Pins - RA2, RA3, RA9, V 0.4 See Note 1 RA10, RA14, RA15, RB0, RB1, RB11, RF4, RF5, RG2, RG3 **Output Low Voltage** I/O Pins: $IOL \leq 6 \text{ mA. VDD} = 3.3 \text{V}$ 0.4 V 8x Sink Driver Pins - OSC2, CLKO, See Note 1 **RC15 Output High Voltage** I/O Pins: $IOL \ge -1.8 \text{ mA}, \text{ VDD} = 3.3 \text{ V}$ 2.4 V 2x Source Driver Pins - All pins not See Note 1 defined by 4x or 8x driver pins **Output High Voltage** I/O Pins: $IOL \ge -3 \text{ mA}, \text{ VDD} = 3.3 \text{ V}$ V 4x Source Driver Pins - RA2, RA3, 2.4 HDO20 Vон See Note 1 RA9, RA10, RA14, RA15, RB0, RB1, RB11, RF4, RF5, RG2, RG3 **Output High Voltage** I/O Pins: $IOL \ge -6 \text{ mA}, \text{ VDD} = 3.3 \text{ V}$ 8x Source Driver Pins - OSC2, CLKO, 2.4 V See Note 1 **RC15**

1.5

2.0

3.0

1.5

2.0

3.0

1.5

2.0

Output High Voltage

Output High Voltage

Output High Voltage

2x Source Driver Pins - All pins not

4x Source Driver Pins - RA2, RA3,

RB11, RF4, RF5, RG2, RG3

RA9, RA10, RA14, RA15, RB0, RB1,

8x Source Driver Pins - OSC2, CLKO,

defined by 4x or 8x driver pins

I/O Pins:

Note 1: Parameters are characterized, but not tested.

RC15

HDO20A Voh1

 $IOH \ge -1.9 \text{ mA}, \text{ VDD} = 3.3 \text{ V}$

See Note 1

IOH \geq -1.85 mA, VDD =

3.3V See **Note 1** IOH ≥ -1.4 mA. VDD = 3.3V

See Note 1

IOH \geq -3.9 mA, VDD = 3.3V

See Note 1

 $IOH \ge -3.7 \text{ mA}, \text{ VDD} = 3.3 \text{ V}$

See **Note 1** IOH ≥ -2 mA. VDD = 3.3V

See Note 1

IOH \geq -7.5 mA, VDD = 3.3V

See Note 1

 $IOH \ge -6.8 \text{ mA}, \text{VDD} = 3.3 \text{V}$

See **Note 1** IOH ≥ -3 mA, VDD = 3.3V

See Note 1

V

V

V

27.2 AC Characteristics and Timing Parameters

The information contained in this section defines dsPIC33FJXXXMCX06A/X08A/X10A AC characteristics and timing parameters for high temperature devices. However, all AC timing specifications in this section are the same as those in Section 26.2 "AC Characteristics and Timing Parameters", with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, parameter OS53 in Section 26.2 "AC Characteristics and Timing Parameters" is the Industrial and Extended temperature equivalent of HOS53.

TABLE 27-7: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)
	$\begin{array}{llllllllllllllllllllllllllllllllllll$

FIGURE 27-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

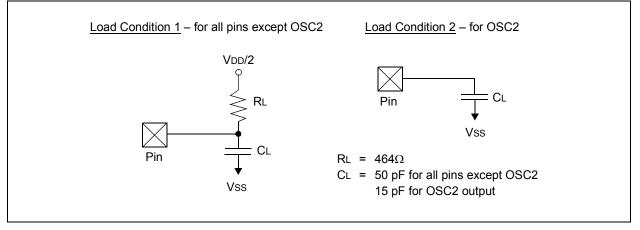
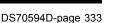


TABLE 27-8: PLL CLOCK TIMING SPECIFICATIONS

-	AC TERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature						
Param No. Symbol		Characteristic	Characteristic Min Typ Max Units Cond					
HOS53	53 DCLK CLKO Stability (Jitter) ⁽¹⁾		-5	0.5	5	%	Measured over 100 ms period	

Note 1: These parameters are characterized, but are not tested in manufacturing.



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TABLE 27-9: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature								
Param No.	Characteristic	Min	Тур	Max	Units	Condition			
	LPRC @ 32.768 kHz ⁽¹⁾						扫一扫上回的	8图案,加我为朋友。	
HF21	LPRC	-70 ⁽²⁾		+70 ⁽²⁾	%	$-40^{\circ}C \le TA \le +150^{\circ}C$	-		

Note 1: Change of LPRC frequency as VDD changes.

2: Characterized but not tested.

TABLE 27-10: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS

-	AC TERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature							
Param No. Symbol		Characteristic ⁽¹⁾	Min	Min Typ Ma		Units	Conditions		
HSP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge		10	25	ns	_		
HSP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	28	_	_	ns	_		
HSP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	35			ns	—		

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 27-11: SPIX MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

	AC CTERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature								
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур	Max	Units	Conditions			
HSP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	10	25	ns				
HSP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	35	_	—	ns	_			
HSP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	28	_	—	ns	_			
HSP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	35	_	—	ns	_			

Note 1: These parameters are characterized but not tested in manufacturing.



TABLE 27-12: SPIX MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

CHARA	AC CTERISTICS	Standard Operating Conditions Operating temperature -40°C					
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур	Max	Units	Conditions*
HSP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	35	ns	<u>扫一扫</u> 上面的二维码图案,加我为
HSP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	25	—	—	ns	_
HSP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	25	—	—	ns	_
HSP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance	15	_	55	ns	See Note 2

Note 1: These parameters are characterized but not tested in manufacturing.

2: Assumes 50 pF load on all SPIx pins.

TABLE 27-13: SPIX MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

	AC TERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature								
Param No.	Symbol	Characteristic ⁽¹⁾ Min Typ Max				Units	Conditions			
HSP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge			35	ns	_			
HSP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	25	_	_	ns	_			
HSP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	25			ns	_			
HSP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance	15	_	55	ns	See Note 2			
HSP60	TssL2doV	SDOx Data Output Valid after SSx Edge	_		55	ns	—			

Note 1: These parameters are characterized but not tested in manufacturing.

2: Assumes 50 pF load on all SPIx pins.



		10110								
	AC TERISTICS	Standard Operating Con Operating temperature			•	, , , , , , , , , , , , , , , , , , , ,				
Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions		•	
		I	Referenc	e Input	S		扫	一扫上面的二维	冯图案,加	我为朋友。
HAD08	IREF	Current Drain		250	600	μA	ADC operating, See No	ote 1		
			—	—	50	μA	ADC off, See Note 1			

Note 1: These parameters are not characterized or tested in manufacturing.

TABLE 27-15: ADC MODULE SPECIFICATIONS (12-BIT MODE)⁽³⁾

-	AC TERISTICS									
Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions			
ADC Accuracy (12-bit Mode) – Measurements with external VREF+/VREF- ⁽¹⁾										
AD23a	Gerr	Gain Error	—	5	10	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V			
AD24a	EOFF	Offset Error	_	2	5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V			
	AD	C Accuracy (12-bit Mode	e) – Meas	uremen	ts with in	ternal V	/REF+/VREF- ⁽¹⁾			
AD23a	Gerr	Gain Error	2	10	20	LSb	VINL = AVSS = 0V, AVDD = 3.6V			
AD24a	EOFF	Offset Error	2	5	10	LSb	VINL = AVSS = 0V, AVDD = 3.6V			
		Dynamic	Performa	nce (12	-bit Mode	e) ⁽²⁾	•			
HAD33a	Fnyq	Input Signal Bandwidth	_		200	kHz	—			

Note 1: These parameters are characterized, but are tested at 20 ksps only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

TABLE 27-16: ADC MODULE SPECIFICATIONS (10-BIT MODE)⁽³⁾

AC CHARACTERISTICSStandard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature										
Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions			
ADC Accuracy (12-bit Mode) – Measurements with external VREF+/VREF- ⁽¹⁾										
AD23b	Gerr	Gain Error	—	3	6	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V			
AD24b	EOFF	Offset Error	—	2	5	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V			
	AD	C Accuracy (12-bit Mode)	– Measu	irement	s with int	ernal V	REF+/VREF- ⁽¹⁾			
AD23b	Gerr	Gain Error		7	15	LSb	VINL = AVSS = 0V, AVDD = 3.6V			
AD24b	EOFF	Offset Error		3	7	LSb	VINL = AVSS = 0V, AVDD = 3.6V			
	Dynamic Performance (10-bit Mode) ⁽²⁾									
HAD33b	Fnyq	Input Signal Bandwidth			400	kHz	—			
HAD33b					400	kHz	—			

e 1: These parameters are characterized, but are tested at 20 ksps only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.



CHARAC	ated)									
Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions			
		Cloc	k Parame	ters			扫一扫上面的二维码图案,加			
HAD50	Tad	ADC Clock Period ⁽¹⁾	147			ns	—			
Conversion Rate										
HAD56	FCNV	Throughput Rate ⁽¹⁾	—		400	Ksps	_			
				-						

TABLE 27-17: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 27-18: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS

-	AC TERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Dperating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature							
Param No.	Symbol	Characteristic	Characteristic Min Typ Max Units Conditions							
	Clock Parameters									
HAD50	TAD	ADC Clock Period ⁽¹⁾	104	_	_	ns	—			
Conversion Rate										
HAD56	FCNV	v Throughput Rate ⁽¹⁾ — — 800 Ksps —								
Mata A.		wasters are characterized but no	4.4.5.5.6.e.e.d.1.		a fa contina na					

Note 1: These parameters are characterized but not tested in manufacturing.

NOTES:

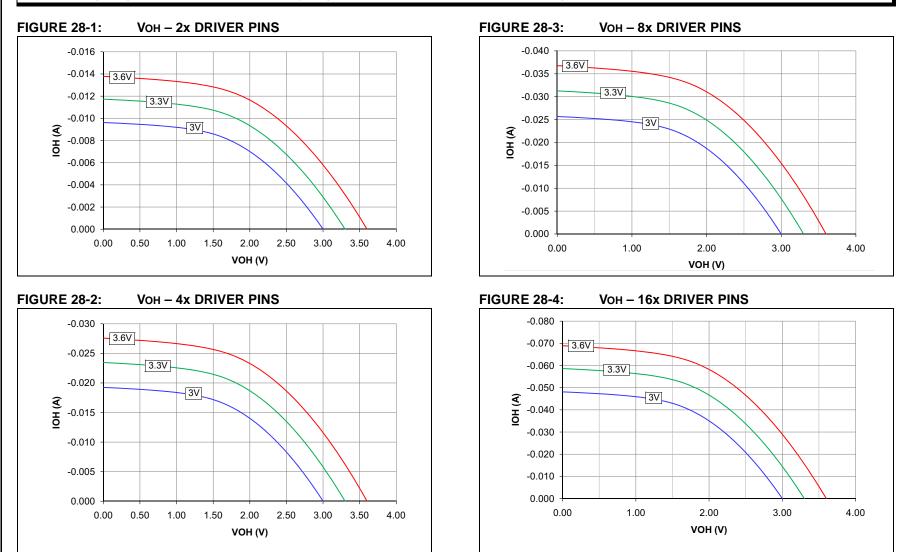


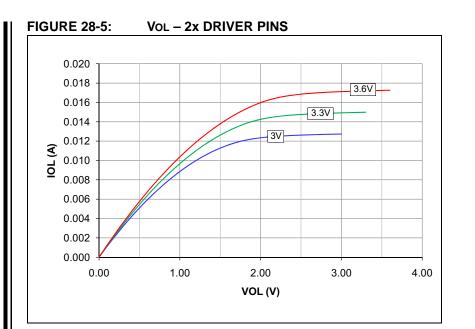
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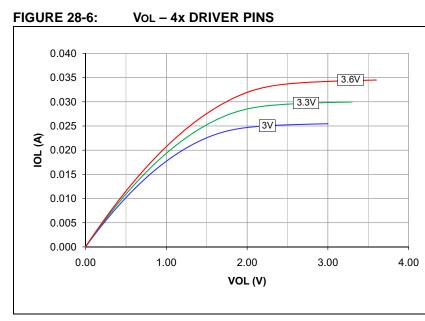


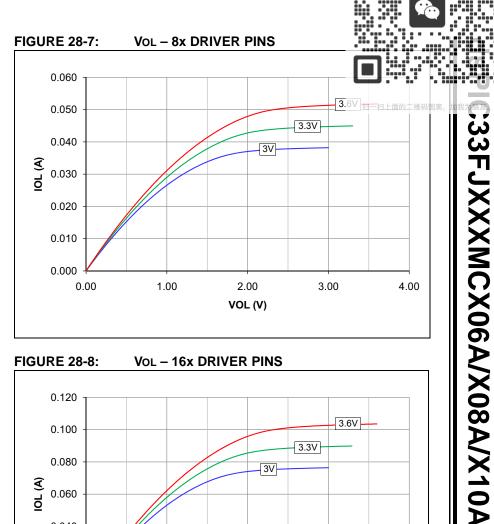
28.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

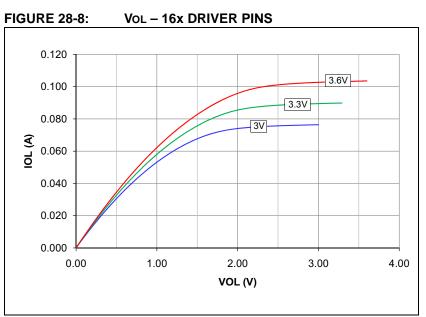
Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating as range (e.g., outside specified power supply range) and therefore, outside the warranted range.

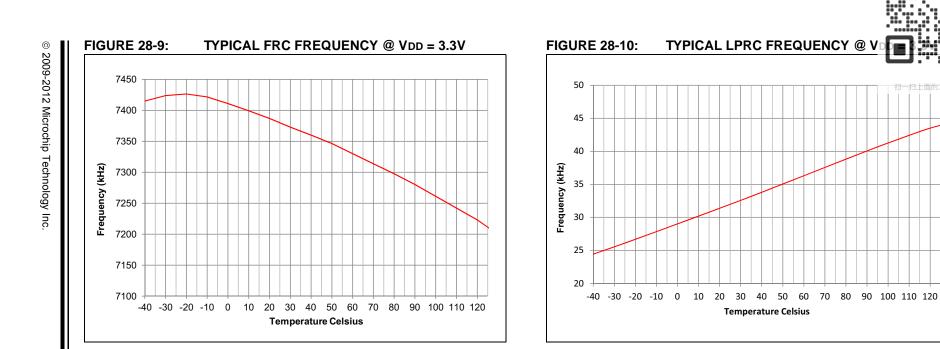












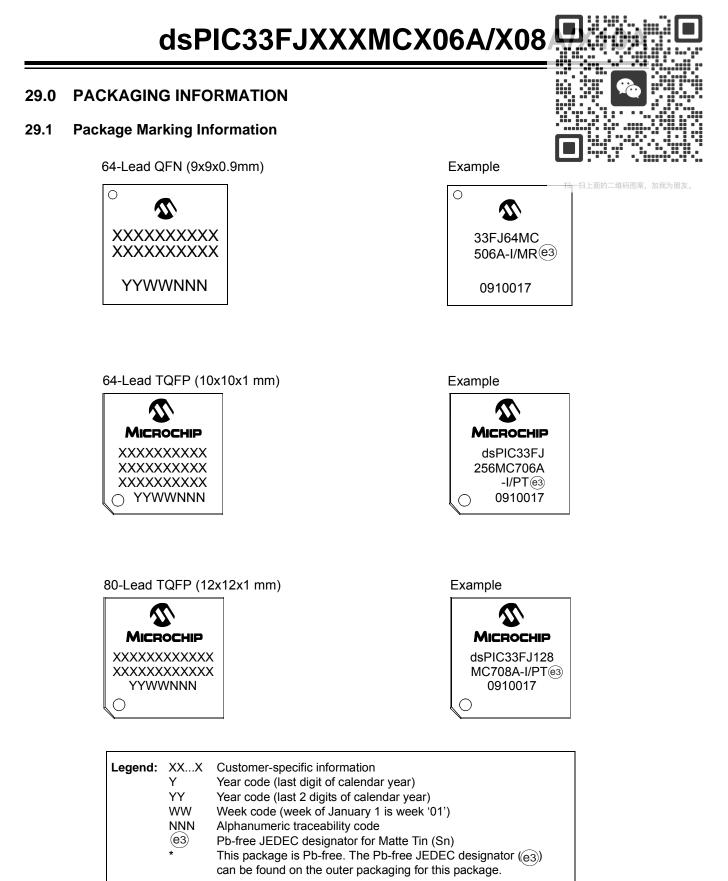
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NOTES:



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29.1 Package Marking Information (Continued)

100-Lead TQFP (12x12x1 mm)



Example







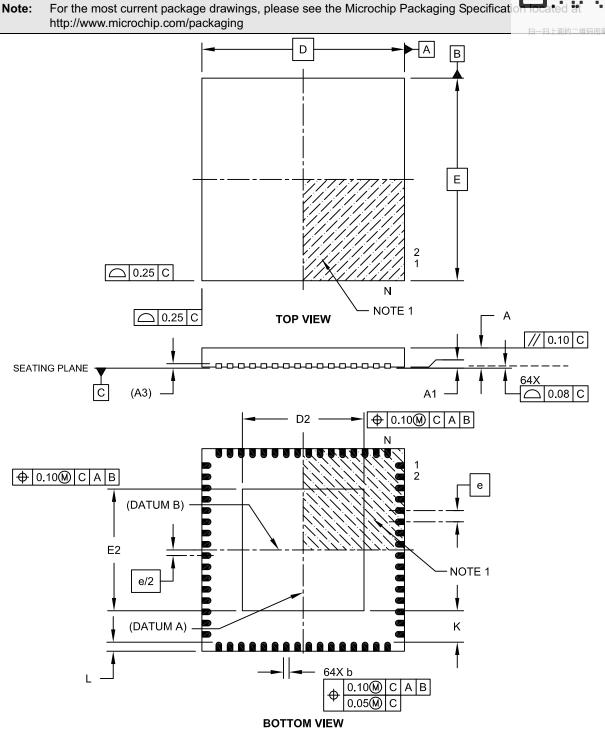




Legend	: XXX Y YY WW NNN @3 *	Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	be carrie	nt the full Microchip part number cannot be marked on one line, it will d over to the next line, thus limiting the number of available s for customer-specific information.

29.2 Package Details

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]



Microchip Technology Drawing C04-154A Sheet 1 of 2

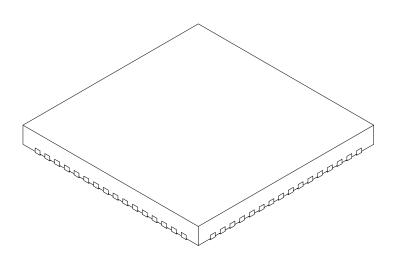


64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

For the most current package drawings, please see the Microchip Packaging Specification Ic Note: http://www.microchip.com/packaging



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	Units	N	MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX		
Number of Pins	Ν	N 64				
Pitch	е		0.50 BSC			
Overall Height	Α	0.80	0.90	1.00		
Standoff	A1	0.00	0.02	0.05		
Contact Thickness	A3	0.20 REF				
Overall Width	Е		9.00 BSC			
Exposed Pad Width	E2	5.30	5.40	5.50		
Overall Length	D		9.00 BSC			
Exposed Pad Length	D2	5.30	5.40	5.50		
Contact Width	b	0.20	0.25	0.30		
Contact Length	L	0.30	0.40	0.50		
Contact-to-Exposed Pad	К	0.20	-	-		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

Dimensioning and tolerancing per ASME Y14.5M.
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.

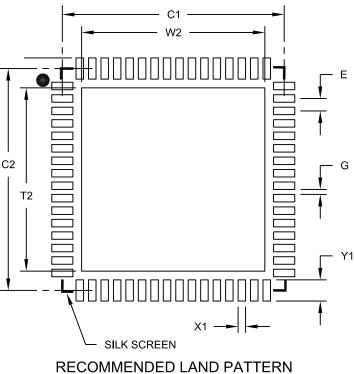
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2

扫一扫上面的二维码图案,加我为朋友。

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specificat http://www.microchip.com/packaging



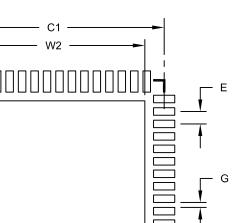
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E			
Optional Center Pad Width	W2	7.3		
Optional Center Pad Length	T2			7.35
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2149A

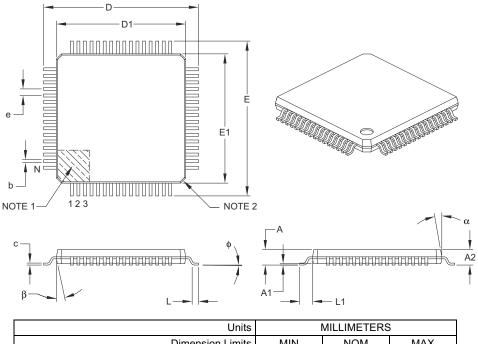




扫一扫上面的二维码图案,加我为朋友。

64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification Ic http://www.microchip.com/packaging



Units			MILLIMETERS	5
	Dimension Limits	MIN	NOM	MAX
Number of Leads	Ν		64	
Lead Pitch	е		0.50 BSC	
Overall Height	A	1	_	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	С	0.09	-	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

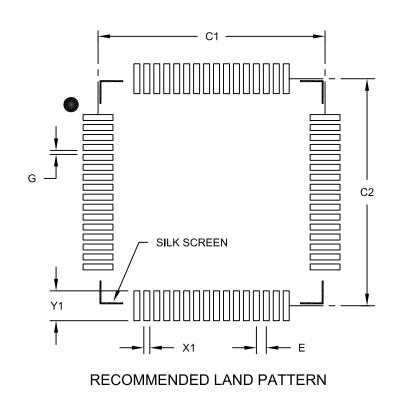
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085B

64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footpr

Note: For the most current package drawings, please see the Microchip Packaging Specificat http://www.microchip.com/packaging

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	Units	Ν	ILLIMETER	S
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1	11.40		
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

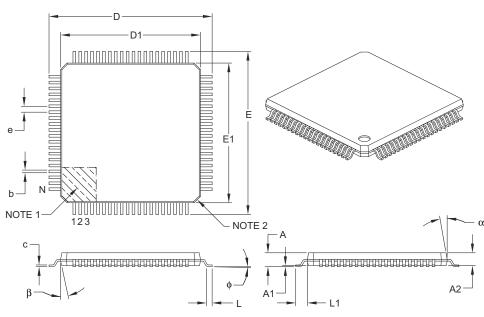
Microchip Technology Drawing No. C04-2085B



扫一扫上面的二维码图案,加我为朋友。

80-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification Ic http://www.microchip.com/packaging



	Units		MILLIMETERS	;
D	imension Limits	MIN	NOM	MAX
Number of Leads	N		80	
Lead Pitch	е		0.50 BSC	
Overall Height	А	_	_	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	3.5°	7°
Overall Width	E	14.00 BSC		
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	С	0.09	-	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

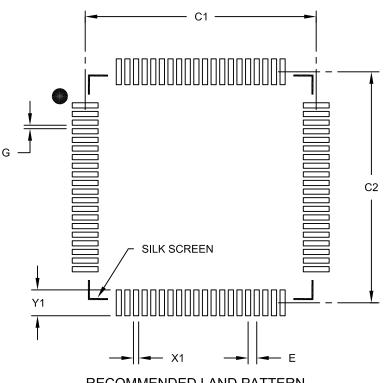
Microchip Technology Drawing C04-092B

80-Lead Plastic Thin Quad Flatpack (PT)-12x12x1mm Body, 2.00 mm Footprin

Note: For the most current package drawings, please see the Microchip Packaging Specificat http://www.microchip.com/packaging



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RECOMMENDED LAND PATTERN

	Units		/ILLIMETER	<u>c</u>	
Dimension	n Limits	MIN	NOM	MAX	
Contact Pitch	E	0.50 BSC			
Contact Pad Spacing	C1	13.40			
Contact Pad Spacing	C2		13.40		
Contact Pad Width (X80)	X1			0.30	
Contact Pad Length (X80)	Y1			1.50	
Distance Between Pads	G	0.20			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

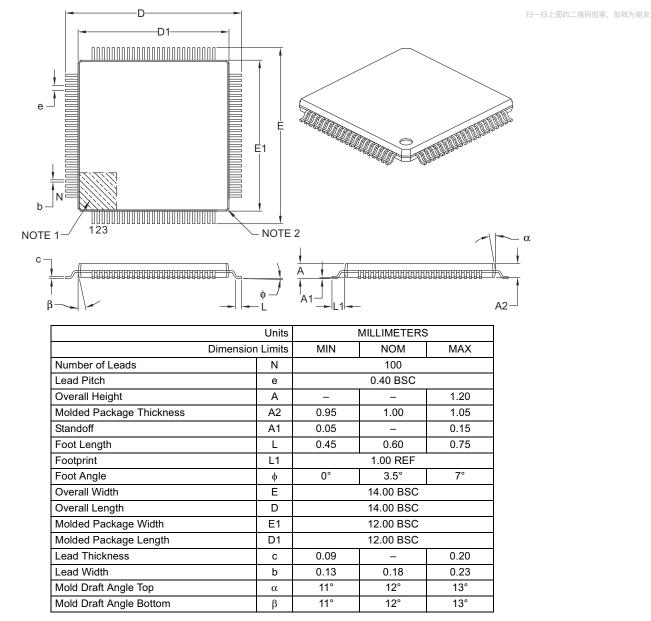
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2092B



100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification Ic http://www.microchip.com/packaging



Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

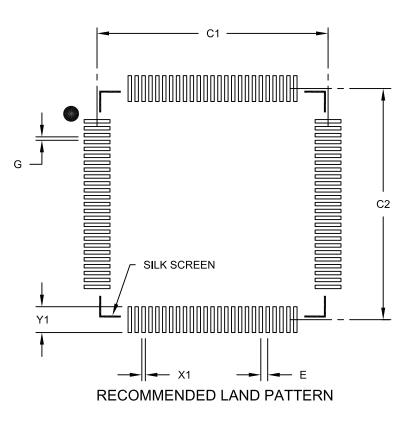
Microchip Technology Drawing C04-100B

100-Lead Plastic Thin Quad Flatpack (PT)-12x12x1mm Body, 2.00 mm Footprint

Note: For the most current package drawings, please see the Microchip Packaging Specificat http://www.microchip.com/packaging



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	Units		/ILLIMETER	S
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Contact Pad Spacing	C1	13.40		
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

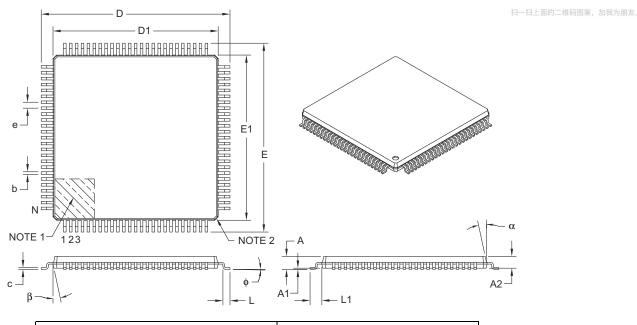
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2100B



100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification Ic http://www.microchip.com/packaging



	Units		MILLIMETERS	5
	Dimension Limits	MIN	NOM	MAX
Number of Leads	N		100	
Lead Pitch	e		0.50 BSC	
Overall Height	А	-	-	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	—	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	3.5°	7°
Overall Width	E	16.00 BSC		
Overall Length	D		16.00 BSC	
Molded Package Width	E1		14.00 BSC	
Molded Package Length	D1		14.00 BSC	
Lead Thickness	С	0.09	-	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

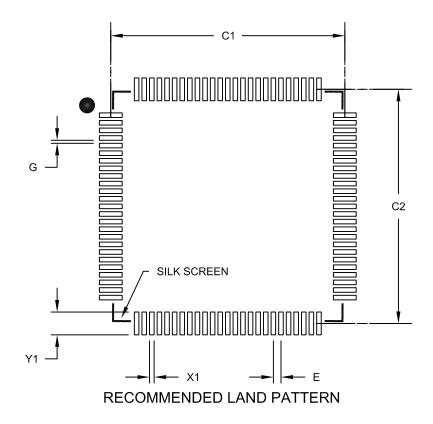
Microchip Technology Drawing C04-110B

100-Lead Plastic Thin Quad Flatpack (PF) - 14x14x1 mm Body 2.00 mm Footprin

Note: For the most current package drawings, please see the Microchip Packaging Specification http://www.microchip.com/packaging



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	Units		MILLIMETER	S
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1	15.40		
Contact Pad Spacing	C2		15.40	
Contact Pad Width (X100)	X1			0.30
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2110B

NOTES:



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APPENDIX A: MIGRATING FROM dsPIC33FJXXXMCX06/ X08/X10 DEVICES TO dsPIC33FJXXXMCX06A/ X08A/X10A DEVICES

The dsPIC33FJXXXMCX06A/X08A/X10A devices were designed to enhance the dsPIC33FJXXXMCX06/ X08/X10 families of devices.

In general, the dsPIC33FJXXXMCX06A/X08A/X10A devices are backward-compatible with dsPIC33FJXXXMCX06/X08/X10 devices; however, manufacturing differences may cause dsPIC33FJXXXMCX06A/X08A/X10A devices to behave differently from dsPIC33FJXXXMCX06/X08/X10 devices. Therefore, complete system test and characterization is recommended if dsPIC33FJXXXMCX06A/X08A/X10A devices are used to replace dsPIC33FJXXXMCX06/X08/X10 devices.

The following enhancements were introduced:

- Extended temperature support of up to +125°C
- Enhanced Flash module with higher endurance and retention
- New PLL Lock Enable Configuration bit
- Added Timer5 trigger for ADC1 and Timer3 trigger for ADC2



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APPENDIX B: REVISION HISTORY

Revision A (May 2009)

This is the initial released version of the document.

Revision B (October 2009)

The revision includes the following global update:

• Added Note 2 to the shaded table that appears at the beginning of each chapter. This new note provides information regarding the availability of registers and their associated bits.

This revision also includes minor typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in the following table.

TABLE B-1: MAJOR SECTION UPDATES

Section Name	Update Description
"16-bit Digital Signal Controllers (up to 256 KB Flash and 30 KB SRAM) with Motor Control and Advanced Analog"	Added information on high temperature operation (see " Operating Range:").
Section 11.0 "I/O Ports"	Changed the reference to digital-only pins to 5V tolerant pins in the second paragraph of Section 11.2 " Open-Drain Configuration ".
Section 20.0 "Universal Asynchronous Receiver Transmitter (UART)"	Updated the two baud rate range features to: 10 Mbps to 38 bps at 40 MIPS.
Section 22.0 "10-bit/12-bit Analog-to-Digital Converter (ADC)"	Updated the ADCx block diagram (see Figure 22-1).
Section 23.0 "Special Features"	Updated the second paragraph and removed the fourth paragraph in Section 23.1 "Configuration Bits" .
	Updated the Device Configuration Register Map (see Table 23-1).
Section 26.0 "Electrical Characteristics"	Updated the Absolute Maximum Ratings for high temperature and added Note 4.
	Updated Power-Down Current parameters DC60d, DC60a, DC60b, and DC60d (see Table 26-7).
	Added I2Cx Bus Data Timing Requirements (Master Mode) parameter IM51 (see Table 26-40).
	Updated the SPIx Module Slave Mode (CKE = 1) Timing Characteristics (see Figure 26-17).
	Updated the Internal LPRC Accuracy parameters (see Table 26-19).
	Updated the ADC Module Specifications (12-bit Mode) parameters AD23a, AD24a, AD23b, and AD24b (see Table 26-46).
	Updated the ADC Module Specifications (10-bit Mode) parameters AD23c, AD24c, AD23d, and AD24d (see Table 26-46).
Section 27.0 "High Temperature Electrical Characteristics"	Added new chapter with high temperature specifications.
"Product Identification System"	Added the "H" definition for high temperature.



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Revision C (March 2011)

This revision includes typographical and formatting changes throughout the data sheet text. In addition, all instances of VDDCORE have been removed.

All other major changes are referenced by their respective section in the following table.

TABLE B-2: MAJOR SECTION UPDATES

Section Name	Update Description
Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers"	Updated the title of Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)".
	The frequency limitation for device PLL start-up conditions was updated in Section 2.7 "Oscillator Value Conditions on Device Start-up".
	The second paragraph in Section 2.9 "Unused I/Os" was updated.
Section 4.0 "Memory Organization"	The All Resets values for the following SFRs in the Timer Register Map were changed (see Table 4-6): • TMR1
	• TMR2
	• TMR3
	• TMR4
	• TMR5
	• TMR6
	• TMR7
	• TMR8
	• TMR9
Section 9.0 "Oscillator Configuration"	Added Note 3 to the OSCCON: Oscillator Control Register (see Register 9-1).
	Added Note 2 to the CLKDIV: Clock Divisor Register (see Register 9-2).
	Added Note 1 to the PLLFBD: PLL Feedback Divisor Register (see Register 9-3).
	Added Note 2 to the OSCTUN: FRC Oscillator Tuning Register (see Register 9-4).
Section 22.0 "10-bit/12-bit Analog-to-Digital Converter (ADC)"	Updated the VREFL references in the ADC1 module block diagram (see Figure 22-1).
Section 23.0 "Special Features"	Added a new paragraph and removed the third paragraph in Section 23.1 "Configuration Bits ".
	Added the column "RTSP Effects" to the Configuration Bits Descriptions (see Table 23-2).



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TABLE B-2: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description		
Section 26.0 "Electrical Characteristics"	Removed Note 4 from the DC Temperature and Voltage Specifications (see Table 26-4).		
	Updated the maximum value for parameter DI19 and added plane parameters DI28, DI29, DI60a, DI60b, and DI60c to the i/O Pin inp Specifications (see Table 26-9).	〕二维码 Dut	图案,加我为朋友。
	Removed Note 2 from the AC Characteristics: Internal RC Accura (see Table 26-18).	су	
	Updated the characteristic description for parameter DI35 in the I/ Timing Requirements (see Table 26-20).	0	
	Updated the ADC Module Specification minimum values for parameters AD05 and AD07, and updated the maximum value for parameter AD06 (see Table 26-43).	r	
	Added Note 1 to the ADC Module Specifications (12-bit Mode) (se Table 26-44).	e	
	Added Note 1 to the ADC Module Specifications (10-bit Mode) (se Table 26-45).	ee	
	Added DMA Read/Write Timing Requirements (see Table 26-48).		
Section 27.0 "High Temperature Electrical Characteristics"	Updated all ambient temperature end range values to +150°C throughout the chapter.		
	Updated the storage temperature end range to +160°C.		
	Updated the maximum junction temperature from +145°C to +155°	°C.	
	Updated the maximum values for High Temperature Devices in th Thermal Operating Conditions (see Table 27-2).	e	
	Updated the ADC Module Specifications (12-bit Mode), removing parameters with the exception of HAD33a (see Table 27-14).	all	
	Updated the ADC Module Specifications (10-bit Mode), removing parameters with the exception of HAD33b (see Table 27-16).	all	

Revision D (June 2012)

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in the following table.



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TABLE B-3: MAJOR SECTION UPDATES

Section Name	Update Description
Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers"	Updated the Recommended Minimum Connection (see Figure 2-1).
Section 9.0 "Oscillator Configuration"	Updated the COSC<2:0> and NOSC<2:0> bit value definitions for '001' (see Register 9-1).
Section 22.0 "10-bit/12-bit Analog-to-Digital Converter (ADC)"	Updated the Analog-to-Digital Conversion Clock Period Block Diagram (see Figure 22-2).
Section 23.0 "Special Features"	Added Note 3 to the On-chip Voltage Regulator Connections (see Figure 23-1).
Section 26.0 "Electrical Characteristics"	Updated "Absolute Maximum Ratings".
	Updated Operating MIPS vs. Voltage (see Table 26-1).
	Removed parameter DC18 from the DC Temperature and Voltage Specifications (see Table 26-4).
	Updated the notes in the following tables:
	• Table 26-5
	• Table 26-6
	• Table 26-7
	• Table 26-8
	Updated the I/O Pin Output Specifications (see Table 26-10).
	Updated the Conditions for parameter BO10 (see Table 26-11).
	Updated the Conditions for parameters D136b, D137b and D138b (TA = 150°C) (see Table 26-12).
Section 27.0 "High Temperature Electrical	Updated "Absolute Maximum Ratings ⁽¹⁾ ".
Characteristics"	Updated the I/O Pin Output Specifications (see Table 27-6).
	Removed Table 26-7: DC Characteristics: Program Memory.

NOTES:



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Revision Level — Tape and Reel Flag Temperature Rang	illy Size (KB) J (if applice e		a) dsPIC33FJ256M Motor Control ds 64-Kbyte progra 64-pin, Industrial TQFP package.	sPIC33, I m me <u>pony_{a上}面的二维码图案,</u> 加我为朋 I temperature,
Architecture:	33 =	16-bit Digital Signal Controller		
Flash Memory Family:	FJ =	Flash program memory, 3.3V		
Product Group:	MC5 = MC7 =	Motor Control family Motor Control family		
Pin Count:	06 = 08 = 10 =	64-pin 80-pin 100-pin		
Temperature Range:	I = E = H =	-40°C to +125°C (Extended)		
Package:	PT = PF = MR =	10x10 or 12x12 mm TQFP (Thin Quad Flatpack) 14x14 mm TQFP (Thin Quad Flatpack) 9x9 mm QFN (Plastic Quad Flatpack)		
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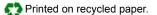
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