

**VDS= -30V**

RDS(ON), V<sub>GS</sub>@-10V, I<sub>D</sub>S@-8.0A = 22mΩ

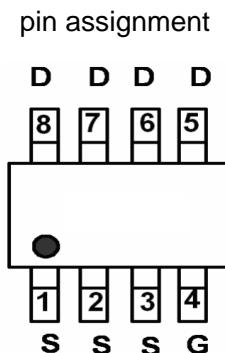
RDS(ON), Vgs@-4.5V, Ids@-6.0A = 35mΩ

## Features

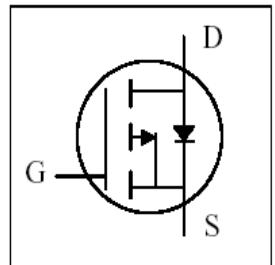
## Advanced trench process technology

## High Density Cell Design For Ultra Low On-Resistance

## Package Dimensions



The diagram illustrates the top view and side cross-section of an SOP-8 package. The top view shows a rectangular body with eight lead pins at the bottom, labeled with dimensions A (height), B (width), C (total height), D (lead thickness), E (lead pitch), F (lead height), G (lead width), and H (lead thickness). The side cross-section provides a detailed view of the lead structure, showing internal dimensions M, N, O, P, Q, R, S, T, U, V, W, X, Y, Z, and the lead height of 0.25.



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	M	0.10	0.25
B	4.80	5.00	H	0.35	0.49
C	3.80	4.00	L	1.35	1.75
D	0°	8°	J	0.375 REF.	
E	0.40	0.90	K	45°	
F	0.19	0.25	G	1.27 TYP.	

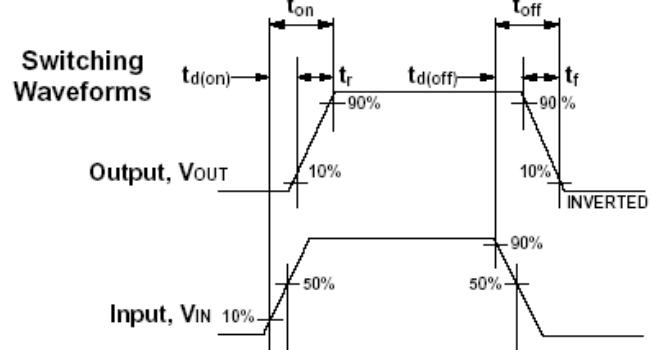
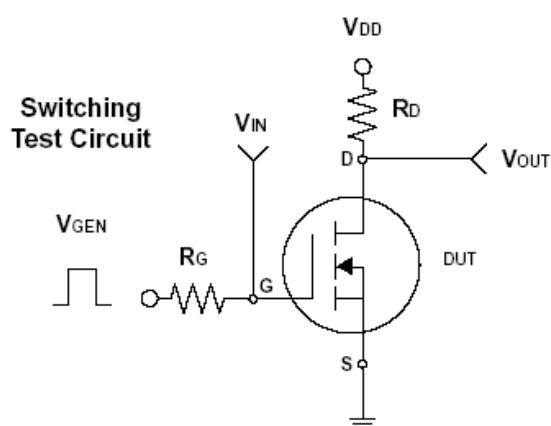
**Maximum Ratings and Thermal Characteristics (TA = 25°C unless otherwise noted)** 25°C

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	-30	V	
Gate-Source Voltage	V <sub>GS</sub>	± 20		
Continuous Drain Current	I <sub>D</sub>	-10	A	
Pulsed Drain Current	I <sub>DM</sub>	-50		
Maximum Power Dissipation	TA = 25°C	P <sub>D</sub>	2.5	W
	TA = 75°C		1.2	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C	
Junction-to-Ambient Thermal Resistance (PCB mounted)	R <sub>θJA</sub>	50	°C/W	

**ELECTRICAL CHARACTERISTICS**

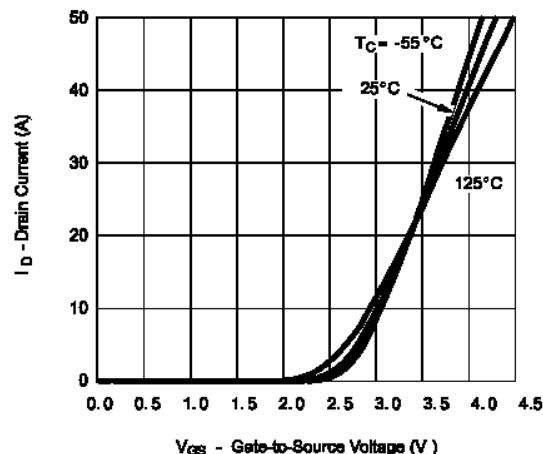
Parameter	符号	Test Condition	最小值	典型值	最大值	单位
<b>Static</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -8.0A$	18.0	22.0	35.0	$m\Omega$
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -4.5V, I_D = -6.0A$		25.0		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1	-1.4	-3	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -24V, V_{GS} = 0V$			-1	$\mu A$
Gate Body Leakage	$I_{GSS}$	$V_{GS} = \pm 20V, V_{DS} = 0V$			$\pm 100$	nA
Forward Transconductance	$g_f$	$V_{DS} = -10V, I_D = -5A$		21		S
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS} = -15V, I_D = -1.5A$ $V_{GS} = 10V$		26		nC
Gate-Source Charge	$Q_{gs}$			2.6		
Gate-Drain Charge	$Q_{gd}$			4.8		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15V, RL = 15\Omega$ $I_D = -1A, V_{GEN} = -10V$ $R_G = 6\Omega$		17		ns
Turn-On Rise Time	$t_r$			14		
Turn-Off Delay Time	$t_{d(off)}$			83		
Turn-Off Fall Time	$t_f$			33		
Input Capacitance	$C_{iss}$	$V_{DS} = -15V, V_{GS} = 0V$ $f = 200KHz$		1600		pF
Output Capacitance	$C_{oss}$			225		
Reverse Transfer Capacitance	$C_{rss}$			165		
<b>Source-Drain Diode 源漏二极管参数</b>						
Max. Diode Forward Current	$I_s$			-2.1		A
Diode Forward Voltage	$V_{SD}$	$I_s = -2.1A, V_{GS} = 0V$		0.78		V

Note: Pulse test: pulse width <= 300us, duty cycle<= 2%

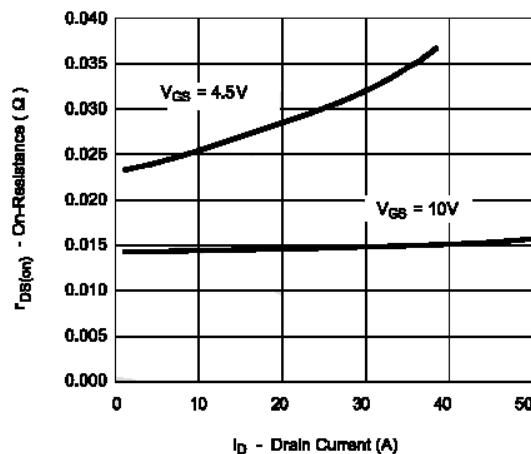


Typical Characteristics ( $T_J = 25^\circ\text{C}$  Noted)

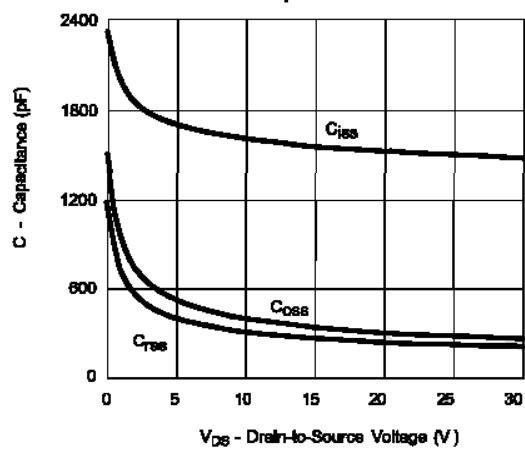
Transfer Characteristics



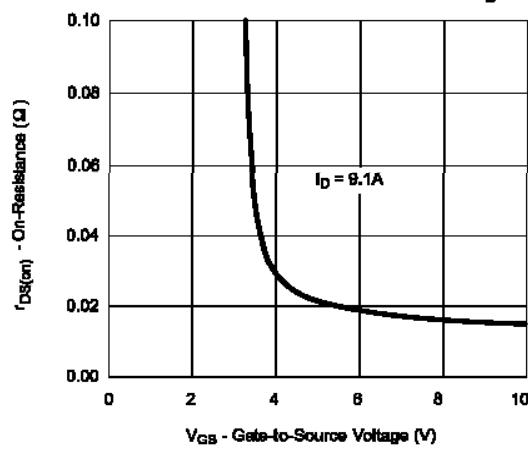
On-Resistance vs. Drain Current



Capacitance



On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

