

200V Half Bridge Driver

PRODUCT SUMMARY

- V_{OFFSET} 200 V max.
- $I_{\text{O}+/-}$ (min) 130 mA/270 mA
- V_{OUT} 10 V - 20 V
- $t_{\text{on/off}}$ (typ.) 160 ns/220 ns
- Delay Matching (typ.) 60 ns

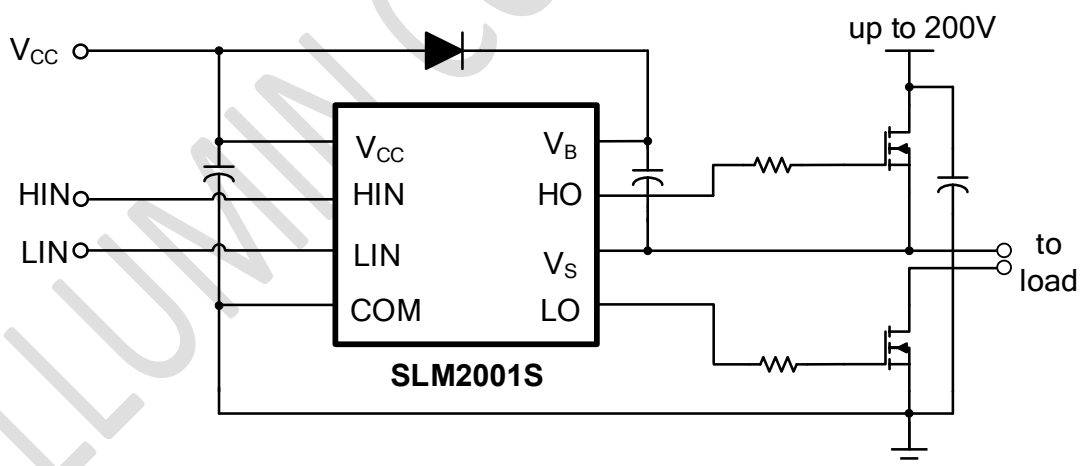
GENERAL DESCRIPTION

The SLM2101S is a high voltage, high speed power MOSFET and IGBT drivers. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to +200 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout
- 3.3 V, 5 V, and 15 V logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- RoHS compliant
- SOIC-8 and DIP 8 package

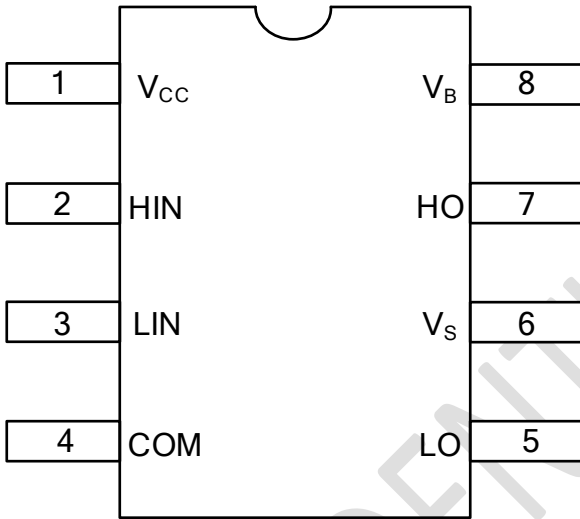
TYPICAL APPLICATION CIRCUIT



(Refer to Lead Assignments for correct configuration). This diagram shows electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Typical Application Circuit

PIN CONFIGURATION

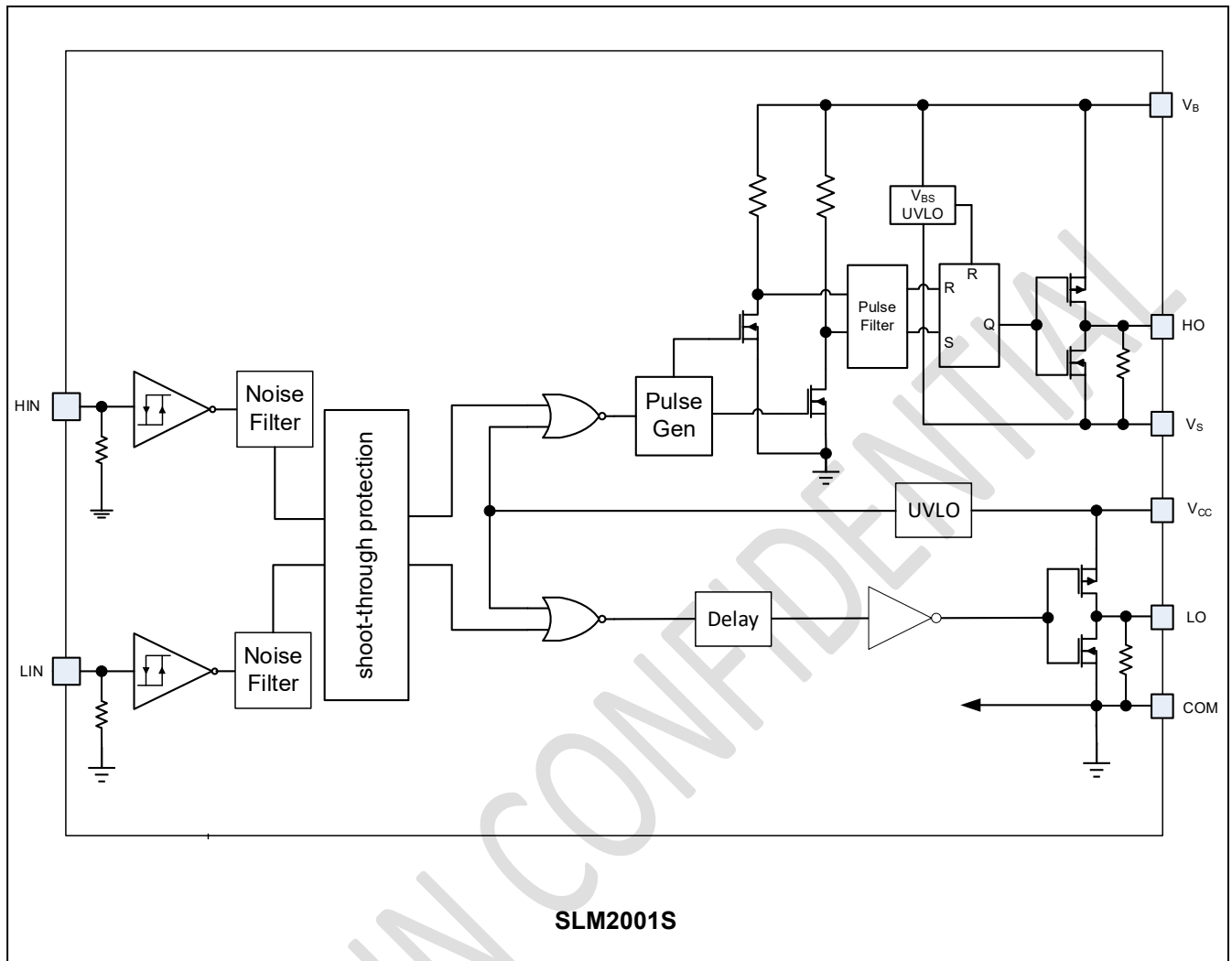
Package	Pin Configuration (Top View)
SOIC-8 and PDIP-8	

PIN DESCRIPTION

No.	Pin	Description
1	V _{CC}	Low-side and logic fixed supply
2	HIN	Logic input for high-side gate driver output (HO), in phase
3	LIN	Logic input for low-side gate driver output (LO), in phase
4	COM	Low-side return
5	LO	Low-side gate drive output
6	V _S	High-side floating supply return
7	HO	High-side gate drive output
8	V _B	High-side floating supply

ORDERING INFORMATION
Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
SLM2001SCA-13GTR	SOIC8, Pb-Free	2500/Reel
SLM2001SCA-GT	SOIC8, Pb-Free	100/Tube
SLM2001SDA-GT	PDIP8, Pb-Free	100/Tube

FUNCTIONAL BLOCK DIAGRAM


ABSOLUTE MAXIMUM RATINGS

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating absolute voltage		-0.3	225	V
V_S	High-side floating supply offset voltage		$V_B - 25$	$V_B + 0.3$	
V_{HO}	High-side floating output voltage		$V_S - 0.3$	$V_B + 0.3$	
V_{CC}	Low-side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low-side output voltage		-0.3	$V_{CC} + 0.3$	
V_{IN}	Logic input voltage (HIN & LIN)		-0.3	$V_{CC} + 0.3$	
dV_S/dt	Allowable offset supply voltage transient		---	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25^\circ\text{C}$	PDIP-8	---	1.0	W
		SOIC-8	---	0.625	
R_{thJA}	Thermal resistance, junction to ambient	PDIP-8	---	125	$^\circ\text{C/W}$
		SOIC-8	---	200	
T_J	Junction temperature		---	150	$^\circ\text{C}$
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		---	300	

Note:

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating absolute voltage	$V_S + 10$	$V_S + 20$	V
V_S	High-side floating supply offset voltage	Note 1	200	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side and logic fixed supply voltage	10	20	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & LIN)	0	V_{CC}	
T_A	Ambient temperature	- 40	125	$^\circ\text{C}$

Note:

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at a 15 V differential.

DYNAMIC ELECTRICAL CHARACTERISTICS
 $V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$, $C_L = 1000\text{ pF}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	$V_S = 0\text{ V}$	---	160	220	ns
t_{off}	Turn-off propagation delay	$V_S = 0\text{ V}$	---	220	280	
t_r	Turn-on rise time		---	70	170	
t_f	Turn-off fall time		---	35	90	
MT	Delay matching, HS & LS turn-on/off		---	---	60	

STATIC ELECTRICAL CHARACTERISTICS
 $V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified. The V_{IN} , V_{TH} , and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Logic "1" input voltage	$V_{CC} = 10\text{ V to }20\text{ V}$	2.5	---	---	V
V_{IL}	Logic "0" input voltage		---	---	0.8	
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	$I_O = 20\text{ mA}$	---	0.4	0.6	
V_{OL}	Low level output voltage, V_O		---	0.1	0.2	
I_{LK}	Offset supply leakage current	$V_B = V_S = 600\text{ V}$	---	---	50	μA
I_{QBS}	Quiescent V_{BS} supply current	$V_{IN} = 0\text{ V}$	---	60	78	
I_{QCC}	Quiescent V_{CC} supply current		---	200	305	
I_{IN+}	Logic "1" input bias current	$V_{IN} = 5\text{ V}$	---	8	15	
I_{IN-}	Logic "0" input bias current	$V_{IN} = 0\text{ V}$	---	---	5	
V_{CCUV+} V_{BSUV+}	V_{CC} & V_{BS} supply undervoltage positive going threshold		8	8.9	9.8	V
V_{CCUV-} V_{BSUV-}	V_{CC} & V_{BS} supply undervoltage negative going threshold		7.4	8.2	9	
I_{O+}	Output high short circuit pulsed current	$V_O = 15\text{ V}$ $V_{IN} = \text{Logic "1"}$ $PW \leq 10\text{ }\mu\text{s}$	130	290		mA
I_{O-}	Output low short circuit pulsed current	$V_O = 0\text{ V}$ $V_{IN} = \text{Logic "0"}$ $PW \leq 10\text{ }\mu\text{s}$	270	600		

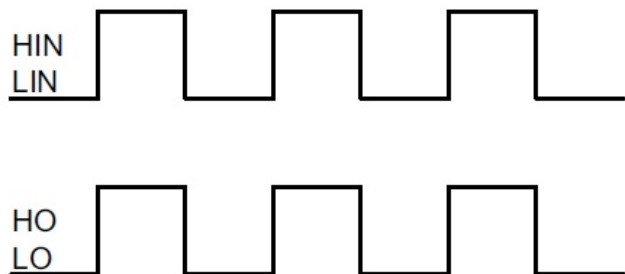


Figure 1. Input/Output Timing Diagram

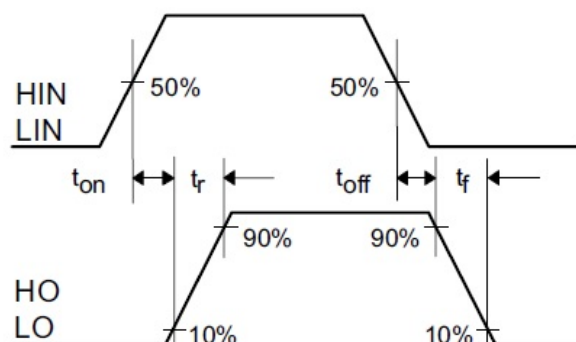


Figure 2. Switching Time Waveform Definitions

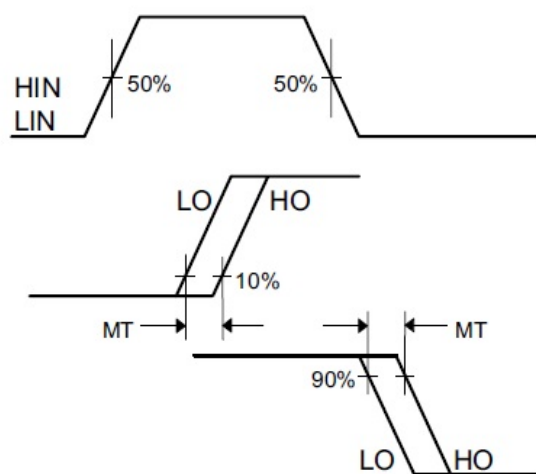
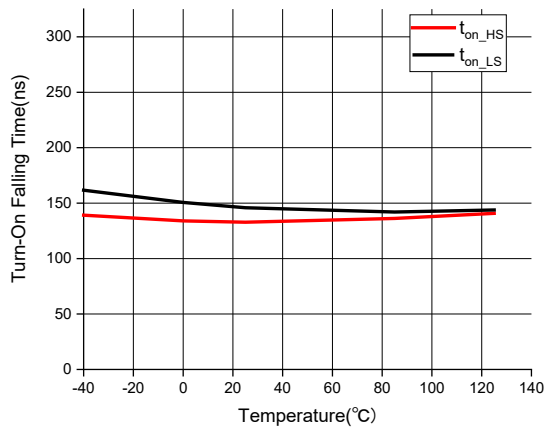
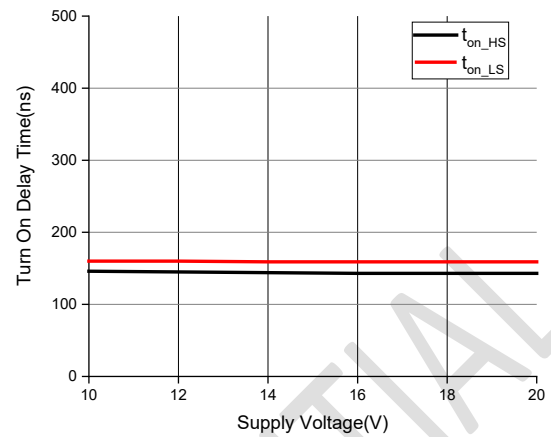
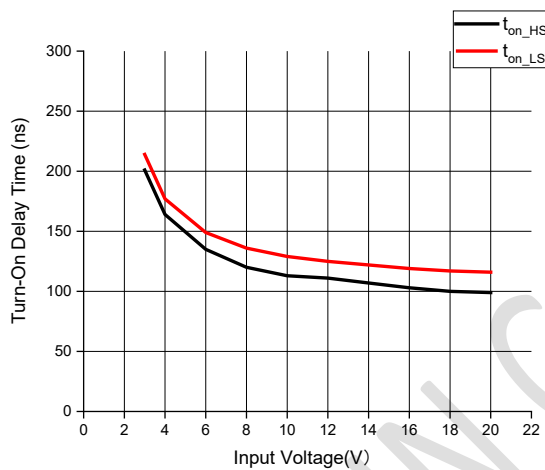
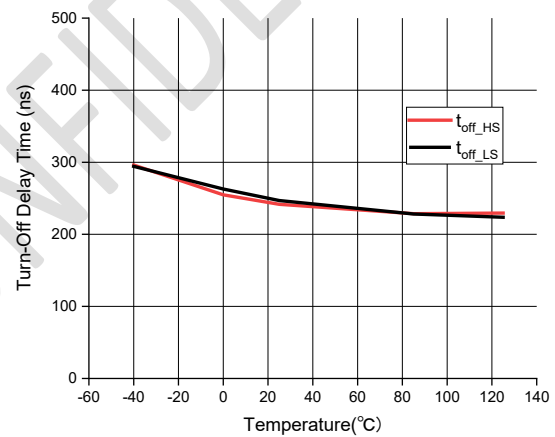
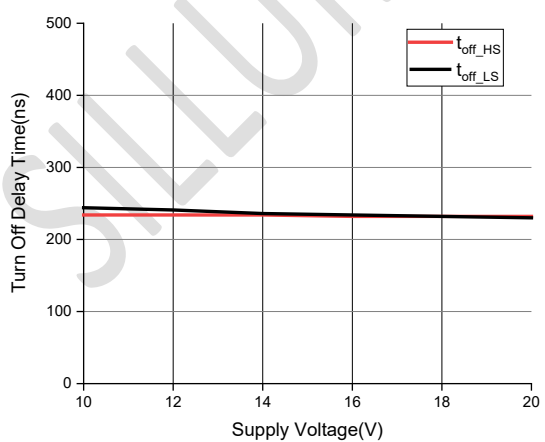
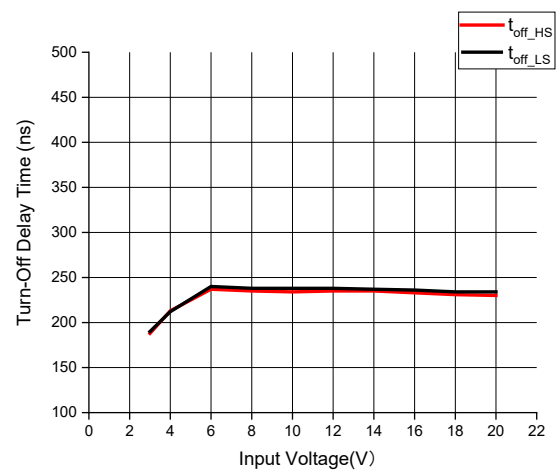
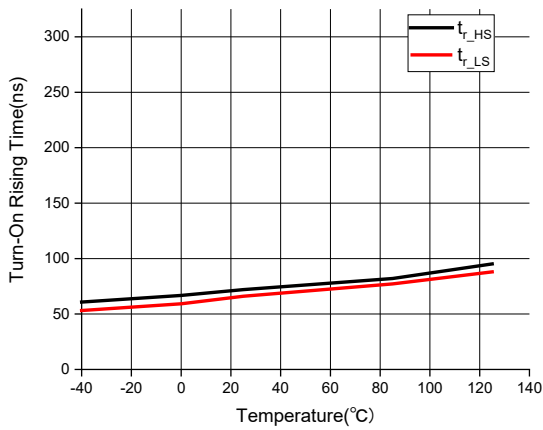
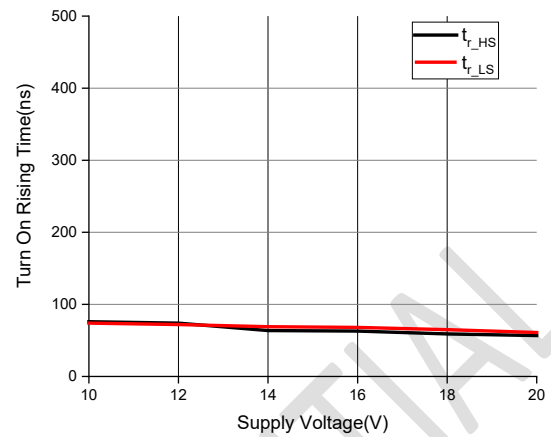
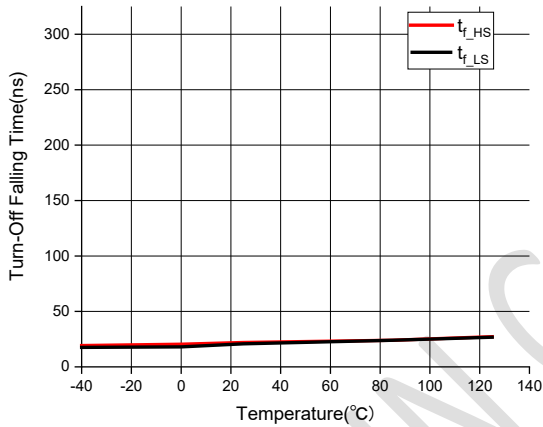
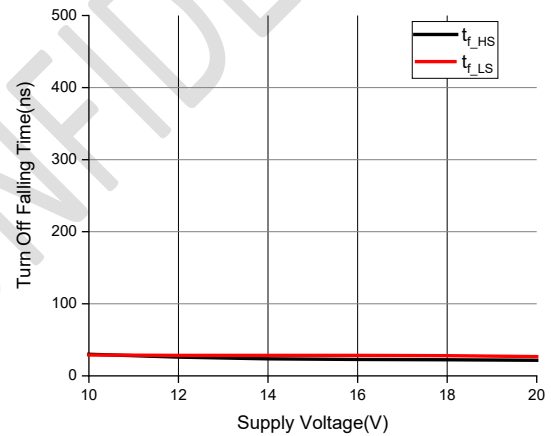
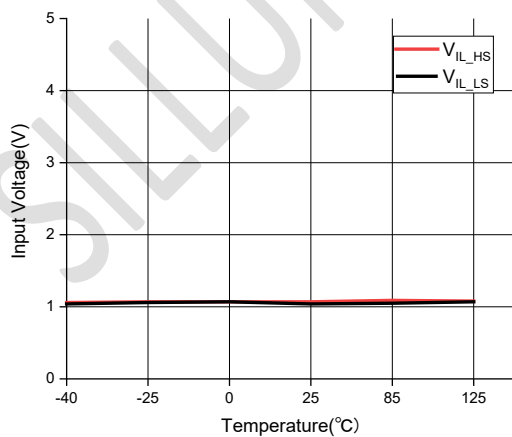
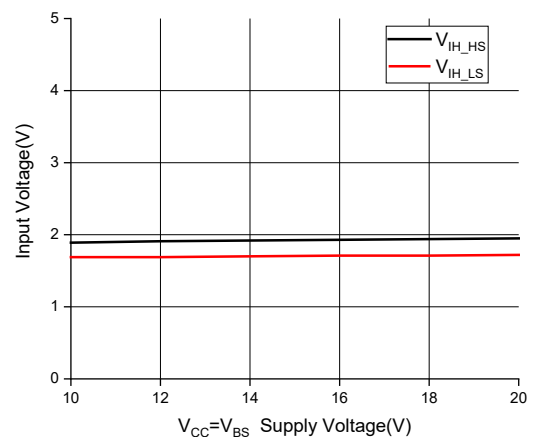
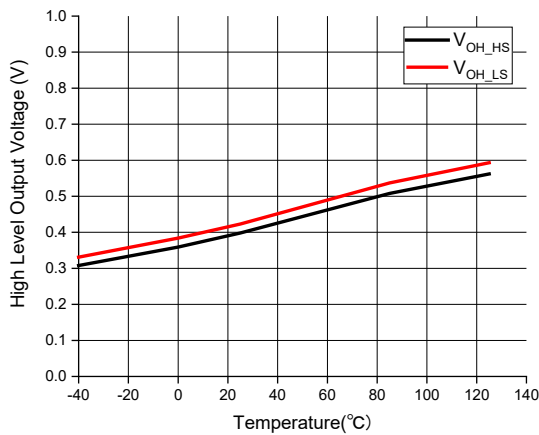
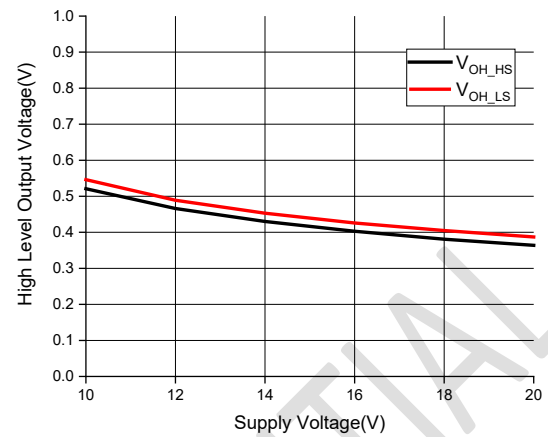
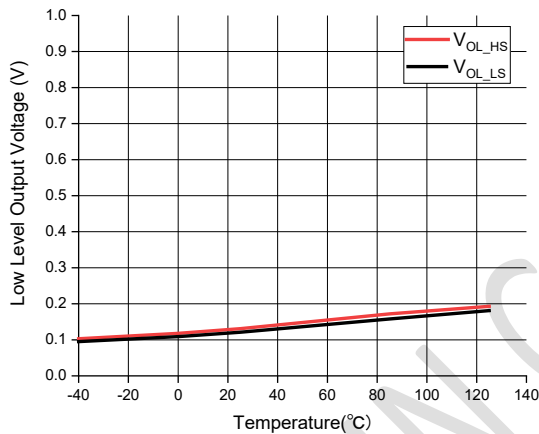
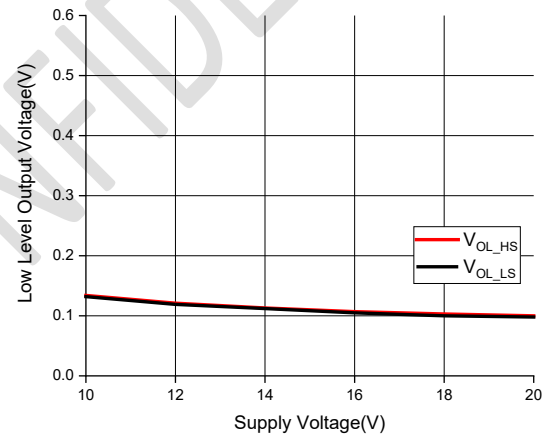
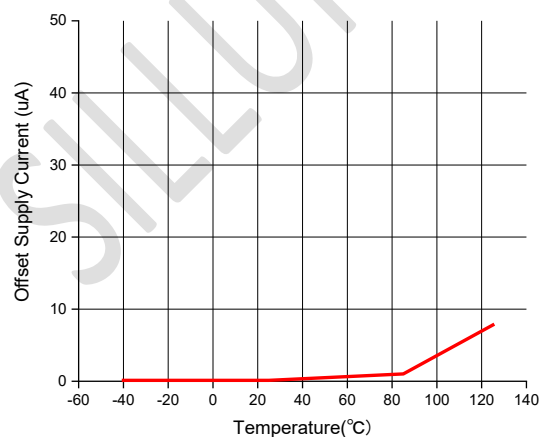
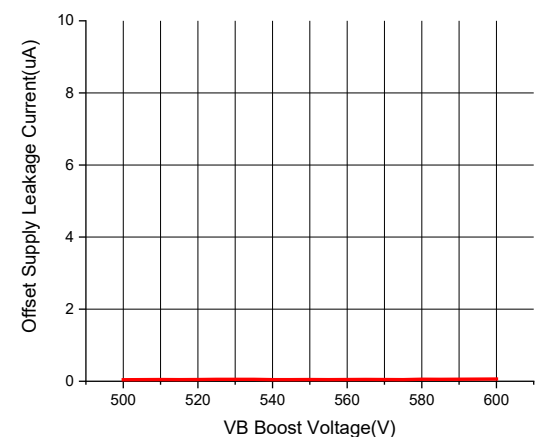
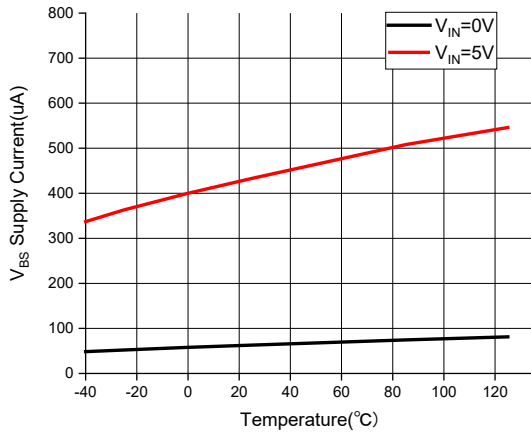
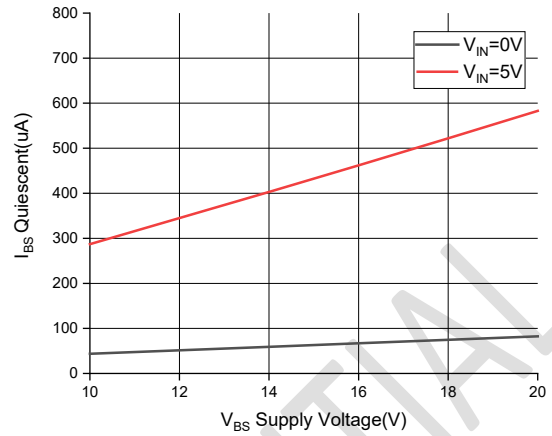
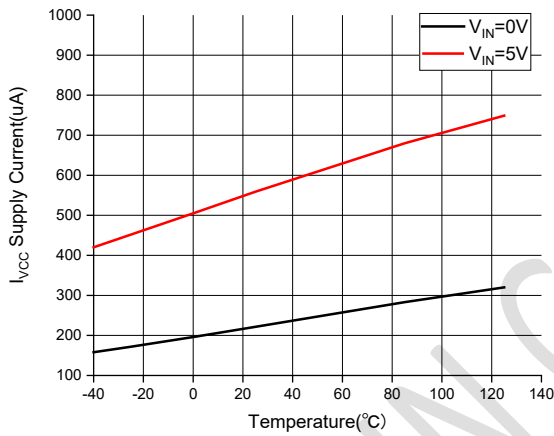
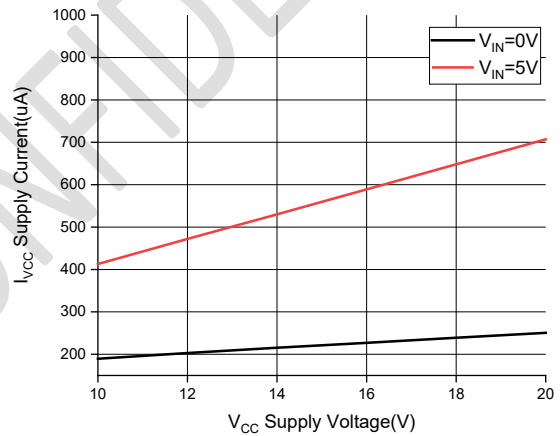
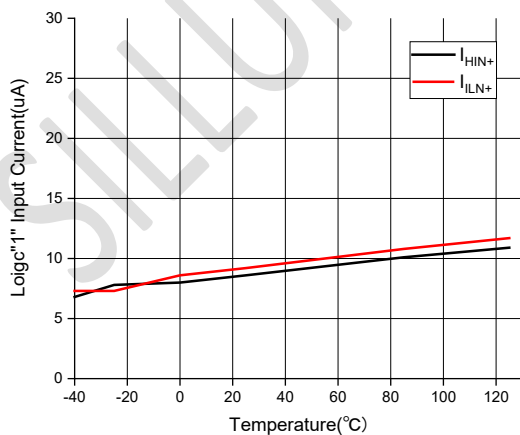
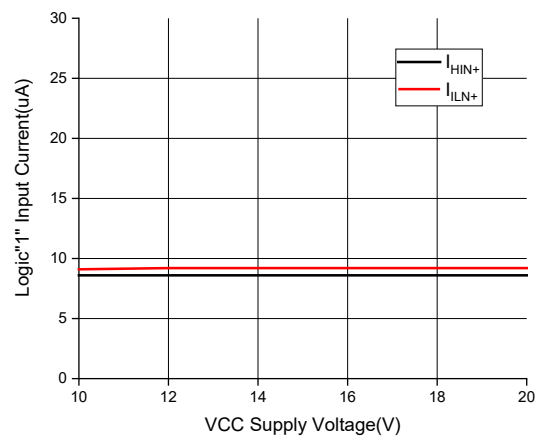


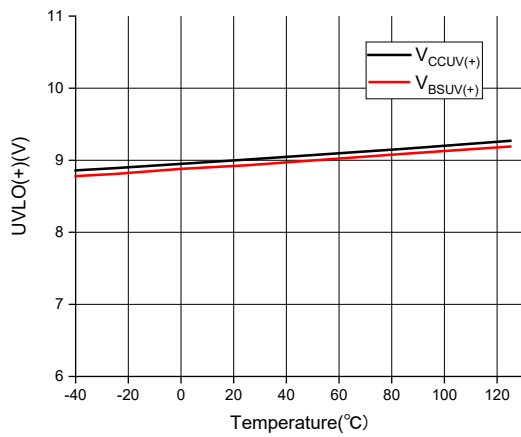
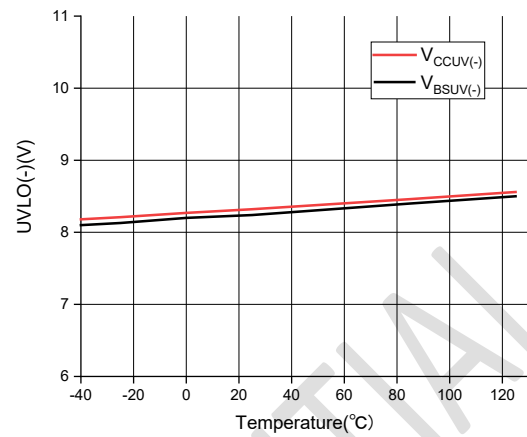
Figure 3. Delay Matching Waveform Definitions

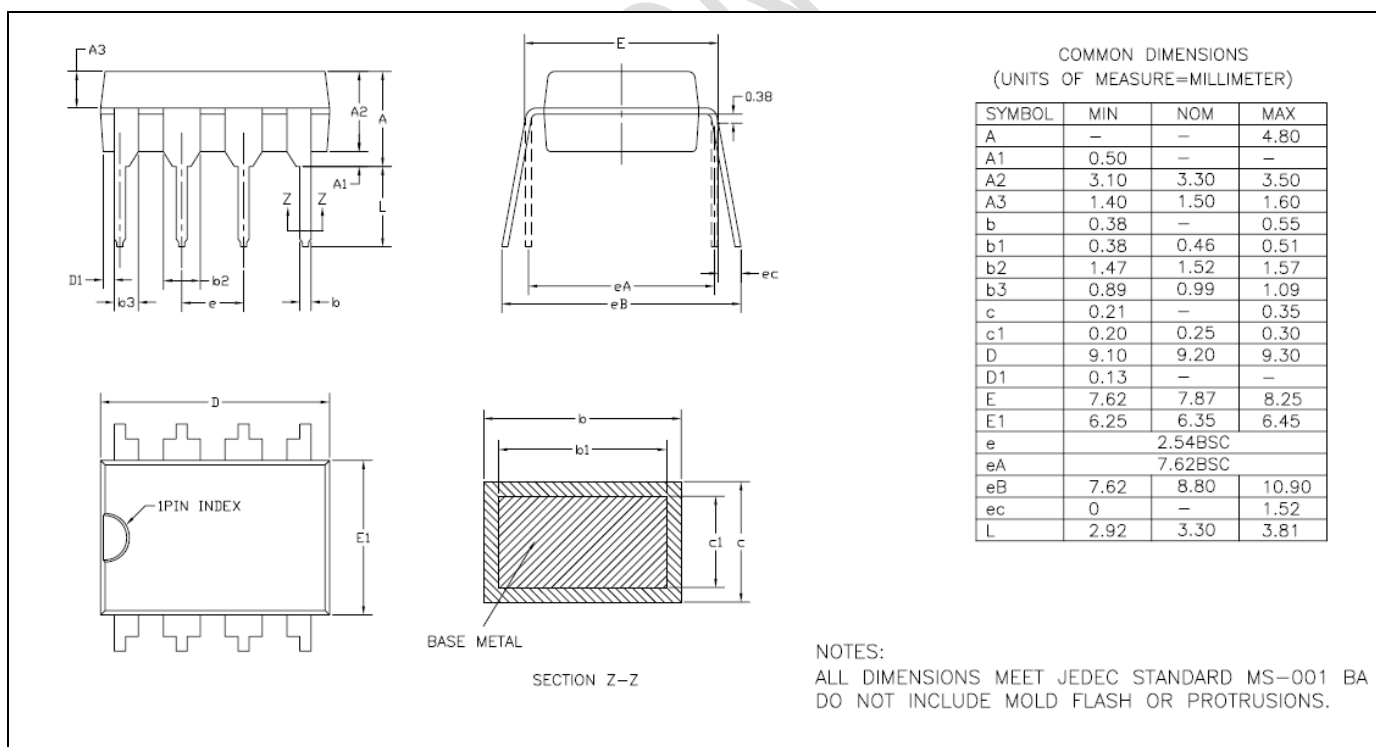
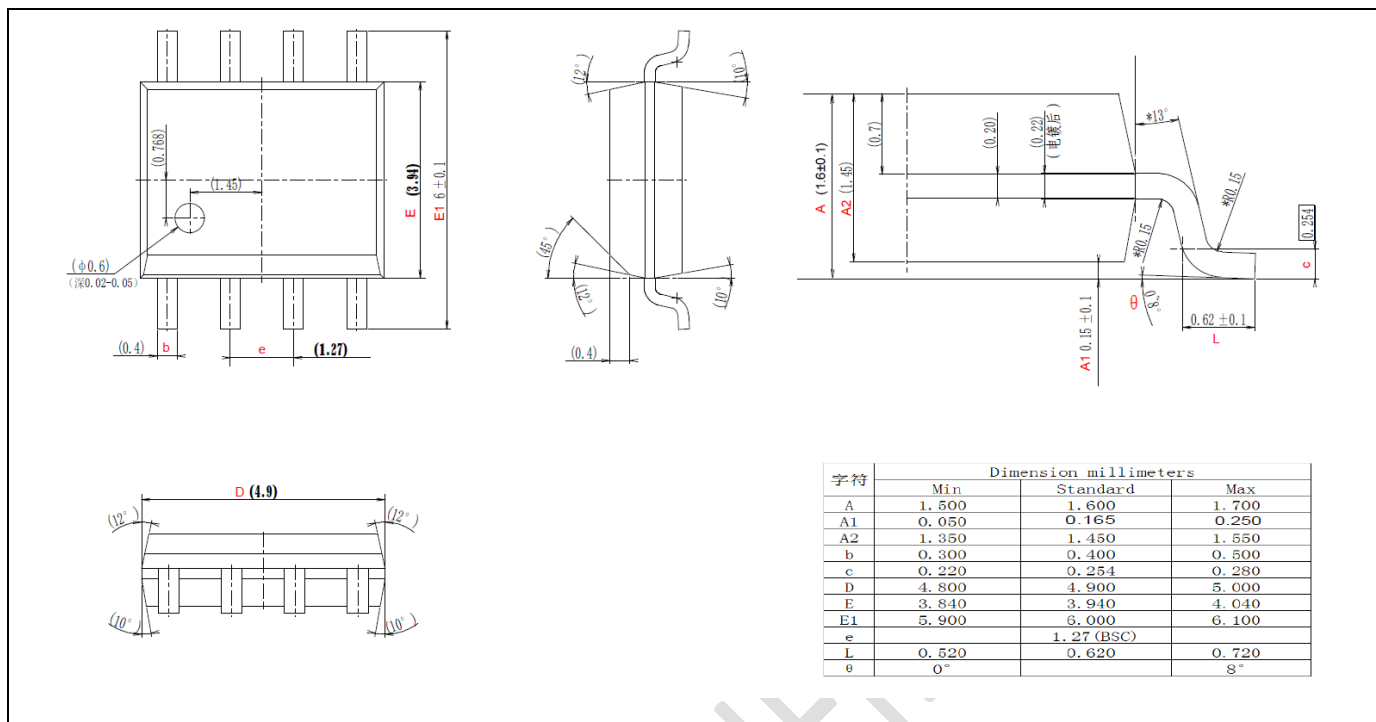

Turn-On Delay Time vs Temperature

Turn-On Delay Time vs Supply Voltage

Turn-On Delay Time vs Input Voltage

Turn-Off Delay Time vs Temperature

Turn-Off Delay Time vs Supply Voltage

Turn-Off Delay Time vs Input Voltage


Turn-On Rising Time Vs Temperature

Turn-On Rising Time vs Supply Voltage

Turn-Off Falling Time Vs Temperature

Turn-Off Falling Time Vs Supply Voltage

Logic "1" Input Voltage Vs Temperature

Logic "1" Input Voltage Vs Supply Voltage


High Level Output Voltage Vs Temperature

High Level Output Voltage Vs Supply Voltage

Low Level Output Voltage Vs Temperature

Low Level Output Voltage Vs Supply Voltage

Offset Supply Current Vs Temperature

Offset Supply Current Vs Voltage


 V_{BS} Supply Current Vs Temperature

 V_{BS} Supply Current Vs Voltage

 V_{CC} Supply Current Vs Temperature

 V_{CC} Supply Current Vs Voltage

Logic "1" Input Current Vs Temperature

Logic "1" Input Current Vs Voltage


V_{CC} & V_{BS} UVLO (+) Vs Temperature

V_{CC} & V_{BS} UVLO (-) Vs Temperature

PACKAGE CASE OUTLINES


Revision History

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet, 2019-8-29	
Whole document	new company logo released
Page 1	Removed "Fig 1. "
Rev 1.1 datasheet, 2019-10-21	
Page 1	Change "high side and low side driver" to "half-bridge driver"
Page 1	Change "independent" to "dependent"
Rev 1.2 datasheet, 2020-5-15	
Page 5	I _{QBS} and I _{QCC} change
Rev 1.3 datasheet, 2020-8-23	
Page 5	V _{OH} and V _{OL} test condition change
	I _{IN+} change