ASL3417SHN

Enhanced three channel LED buck driver with limp-home

Rev. 4 — 16 September 2019 Product data sheet

1. Introduction

The ASL3417SHN is a three channel buck mode LED driver IC with a Limp-home mode. It delivers constant average DC current to LEDs independent of the input voltage. The ASL3417SHN supports up to three output channels. It means that with one driver IC 1, 2 or 3 LED strings can be driven independently of each other. It provides a cost effective design solution, specifically targeting automotive exterior and interior lighting applications.

2. General description

The ASL3417SHN has a hysteretic buck DC-to-DC topology. With input voltages from 10 V to 80 V, it allows maximum flexibility on output voltages for each channel, enabling applications with up to 20 LEDs. It also provides an output current of up to and above 1.5 A per channel.[1] Furthermore, two output channels can be connected together to provide an even higher current. It drives an external high-side N channel MOSFET from an internally regulated adjustable supply. The ASL3417SHN buck driver gives a flexible system design which can be used to drive three LED strings with the same architecture.

The ASL3417SHN provides an SPI interface for extensive control and diagnostic communication with an external microcontroller. Furthermore, the ASL3417SHN integrates a customer programmable Limp-home mode. It allows configurable operation in Limp-home mode in case SPI communication with the microcontroller has failed.

The ASL3417SHN offers an adjustable hysteresis for optimizing external components as well as minimizing LED current ripple.

In addition, the ASL3417SHN provides an output voltage of up to 70 V. It has a measurement capability that can be used to identify LED open or short circuit conditions. The microcontroller can read this voltage and use it to detect open or short circuit conditions. There are also additional diagnostic features such as current reached status.

Additional features include input under-voltage lockout and thermal shutdown when the junction temperature of the ASL3417SHN exceeds +175 °C.

It is housed in a very small HVQFN32 pin package with an exposed thermal pad and is designed to meet the stringent requirements of automotive applications. It is fully AEC Q100 grade 1 qualified. It operates over the ambient automotive temperature range of −40 °C to +125 °C.

1. The ASL3417 provides an accurate current over a 1 : 12.5 range. This range can be scaled up or down using external components. Depending on the operating conditions and component choices, output currents of min 30 mA and more than 3 A can be achieved.

3. Features and benefits

- The ASL3417SHN is an automotive grade product that is AEC-Q100 grade 1 qualified.
- Operating ambient temperature range of –40 °C to +125 °C
- Wide operating input voltage range from +10 V to +80 V
- Able to drive up to 20 LEDs, wide operating LED voltage range regulated from 2.5 V to 70 V
- Output current of up to and above 1.5 A with high LED current accuracy of ±5 % over the complete operating temperature range
- Output current programmable via SPI interface
- Read back programmed current via SPI
- Customer programmable Limp-home mode.
- Two output current ranges, programmable via SPI interface with 5 % accuracy
- Hysteretic converter
- Fast gate drive for high efficiency
- Programmable internal gate driver voltage regulator
- Support logic level and standard level FETs
- Integrated bootstrap diode
- PWM inputs for individual dimming of each channel
- Low Electro Magnetic Emission (EME) and high Electro Magnetic Immunity (EMI)
- Input voltage monitoring and input under voltage protection
- Output voltage monitoring
- Control signal to enable the device
- Junction temperature monitoring via SPI
- Small package outline HVQFN32
- Low quiescent current < 5 μA at 25 °C when EN = 0
- Short-circuit and open-circuit output protection

4. Applications

- Automotive LED lighting
  - Daytime running lights
  - Position or park light
  - Low beam
  - High beam
  - Turn indicator
  - Fog light
  - Cornering light
  - Advanced front lighting

5. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
ASL3417SHN	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-12

6. Block diagram

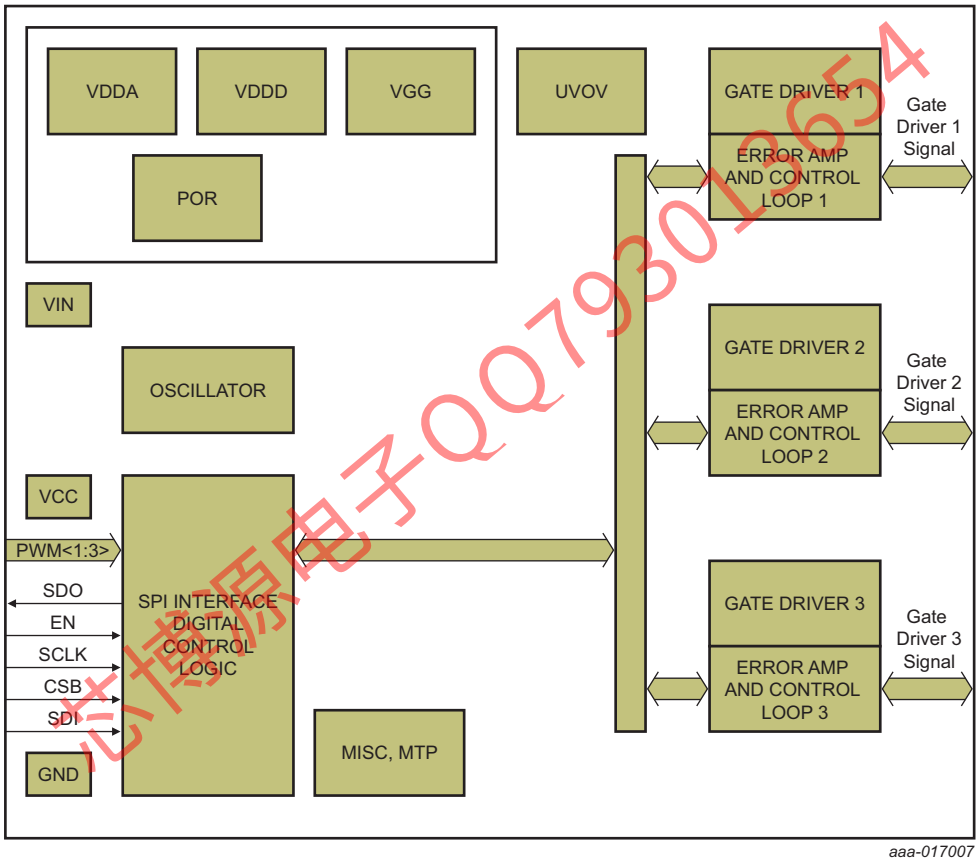


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

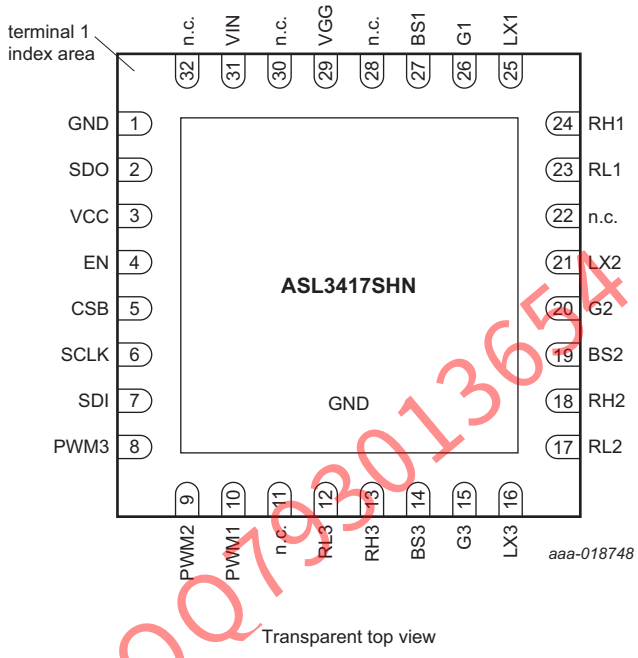


Fig 2. Pin configuration

7.2 Pin description

Table 2. Pin description[1]

Symbol	Pin	Description
GND	1	chip ground
SDO	2	SPI data out
VCC	3	external 5 V supply
EN	4	enable signal
CSB	5	SPI chip select
SCLK	6	SPI clock
SDI	7	SPI data input
PWM3	8	external PWM signal channel 3
PWM2	9	external PWM signal channel 2
PWM1	10	external PWM signal channel 1
n.c.	11	not connected
RL3	12	sense resistor low side channel 3
RH3	13	sense resistor high side channel 3
BS3	14	boot supply channel 3
G3	15	channel 3 gate driver
LX3	16	inductor connection to switching FET channel 3

Table 2. Pin description[1] *...continued*

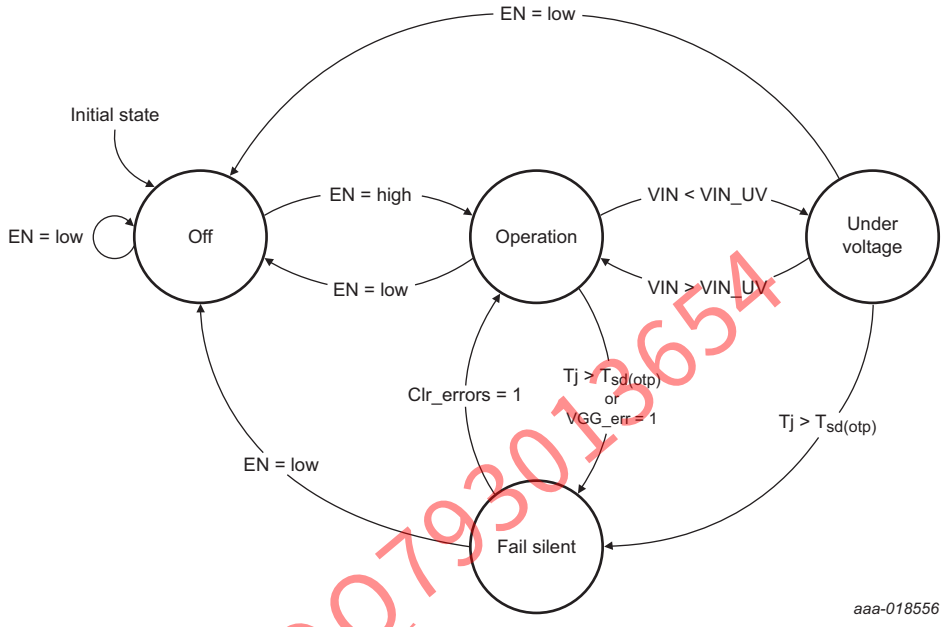
Symbol	Pin	Description
RL2	17	sense resistor low side channel 2
RH2	18	sense resistor high side channel 2
BS2	19	boot supply channel 2
G2	20	channel 2 gate driver
LX2	21	inductor connection to switching FET channel 2
n.c.	22	not connected
RL1	23	sense resistor low side channel 1
RH1	24	sense resistor high side channel 1
LX1	25	inductor connection to switching FET channel 1
G1	26	channel 1 gate driver
BS1	27	boot supply channel 1
n.c.	28	not connected
VGG	29	gate driver supply
n.c.	30	not connected
VIN	31	input voltage
n.c.	32	not connected

[1] Not connected (n.c.) pins are internally not connected and must be left floating to maintain high-voltage separation.

For enhanced thermal and electrical performance, the exposed center pad of the package should be soldered to board ground (and not to any other voltage level).

8. Functional description

8.1 Operating modes



Note: All outputs should be turned off at least 200 ns before the transition from operation to off mode is executed

Fig 3. State diagram

8.1.1 Off mode

If the EN pin goes low, the ASL3417SHN switches to off mode.

In Off mode, the SPI interface and all outputs are turned off. Before off mode is entered, all channels should be turned off.

8.1.2 Operation mode

The ASL3417SHN switches from Off mode to Operation mode when the input voltage is above the power-on detection threshold ($V_{th(det)off}$) and the EN pin is high. In operation mode, all outputs are available as configured via the SPI interface.

8.1.3 Under voltage mode

The ASL3417SHN switches from operation mode to under voltage mode as soon as the input voltage drops below the programmed voltage. In under voltage mode, all outputs, including the gate voltage supply are off.

8.1.4 Fail silent mode

The ASL3417SHN switches from Operation mode to Fail silent mode, when the junction temperature exceeds the over temperature shutdown threshold or a VGG error is detected.

In Fail silent mode, all outputs are turned off and only the SPI interface remains operational.

8.2 Buck converter

The ASL3417SHN is a buck converter IC delivering constant current to the LEDs. It is a hysteretic controller that regulates the inductor current. It switches off the external FET when the inductor current rises above the upper threshold current. It switches on when the current falls below the lower threshold. The width of the hysteresis window can be programmed via SPI to keep the switching frequency between bounds. The anode of the LED string is connected to the driver, while the cathode of the LED string is connected to ground. This arrangement helps to reduce the total number of connections to the LEDs.

8.3 Input voltage measurement

The ASL3417SHN measures the supply voltage of the device and makes this measurement available via the SPI interface.

Table 3. VIN voltage measurement register, address 0x38h[1]

Bit	Symbol	Description	Value	Function
7:0	V_VIN[7:0]	VIN voltage measurement	0x00h	voltage measurement not available
			...	VIN voltage = 0.3548 × V_VIN[7:0] − 0.56 V

[1] A write to the VIN voltage measurement register does not set the SPI error bit high.

8.4 Input under voltage detection

The ASL3417SHN offers a variable undervoltage detection threshold.

When the supply voltage is above the under voltage detection threshold, the bit VIN_stat is high, when the supply voltage is below, the bit is low.

For effects of this bit on the functionality of the device, see Section 8.12.1.1.

Table 4. Undervoltage threshold register, address 0x0Fh

Bit	Symbol	Description	Value	Function
7:0	V_VIN_UV[7:0]	undervoltage threshold	0x00h	undervoltage detection threshold = 0 V
			...	undervoltage detection threshold = 0.3548 × V_VIN_UV[7:0] − 0.56 V

8.5 Output current programmability

The ASL3417SHN provides the possibility to program the LED current and LED current hysteresis via the SPI interface.

8.5.1 Output target current programming

The ASL3417SHN target output current, can be programmed via the LED current range registers and the LED current registers of channel 1, 2 and 3. The sense voltage that is set via SPI, and the value of the external sense resistor, determine the actual level.

$$I_{LED} = \frac{V_{LEDcurrent}}{R_{sense}} \quad (1)$$

Table 5. LED current range register, address 0x05h

Bit	Symbol	Description	Value	Function
7:3		reserved	000000	reserved; keep clear for future use
2	I_CH3	LED current range bit channel 3	0	maximum sense voltage is approximately 300 mV
			1	maximum sense voltage is approximately 120 mV
1	I_CH2	LED current range bit channel 2	0	maximum sense voltage is approximately 300 mV
			1	maximum sense voltage is approximately 120 mV
0	I_CH1	LED current range bit channel 1	0	maximum sense voltage is approximately 300 mV
			1	maximum sense voltage is approximately 120 mV

Table 6. LED current channel 1 register, address 0x02h

Bit	Symbol	Description	Value	Function
7:0	I_LED_CH1[7:0]	LED current channel 1	0x00h; 0xF6h...0xFFh	not recommended
			...	When I_CH1 is 0: 1.179 mV × I_LED_CH1 + 0.74 mV
				When I_CH1 is 1: 0.47882 mV × I_LED_CH1 − 0.6 mV

Table 7. LED current channel 2 register, address 0x03h

Bit	Symbol	Description	Value	Function
7:0	I_LED_CH2[7:0]	LED current channel 2	0x00h; 0xF6h...0xFFh	not recommended
			...	When I_CH2 is 0: 1.179 mV × I_LED_CH2 + 0.74 mV
				When I_CH2 is 1: 0.47882 mV × I_LED_CH2 − 0.6 mV

Table 8. LED current channel 3 register, address 0x04h

Bit	Symbol	Description	Value	Function
7:0	I_LED_CH3[7:0]	LED current channel 3	0x00h; 0xF6h...0xFFh	not recommended
			...	When I_CH3 is 0: 1.179 mV × I_LED_CH3 + 0.74 mV
				When I_CH3 is 1: 0.47882 mV × I_LED_CH3 − 0.6 mV

The LED current is the result of the voltage drop across the R_{sense} resistor in mV.

Example:

To achieve an output current of e.g. 300 mA with 200 mΩ R_{sense} resistor on channel 1, two settings are possible:

1. Set bit I_CH1 to 1 and the LED current channel 1 register to 0x7Eh
2. Set bit I_CH1 to 0 and the LED current channel 1 register to 0x32h

For higher granularity and higher accuracy, use setting 1. When the LED current is dynamically adjusted to higher levels than offered when bit I_CHx = 1, deviations are possible.

8.5.2 Hysteresis programming via SPI

ASL3417SHN provides an option to program the level of hysteresis via the SPI interface. The hysteresis setting is independent of the I_CH1, I_CH2 and I_CH3 bits in LED current range registers.

The hysteresis voltage that is set via SPI, and the value of the external sense resistor, determine the actual level.

$$I_{Hyst} = \frac{V_{Hyst}}{R_{sense}} \quad (2)$$

Depending on the hysteresis level, the values of the external components, the input and the output voltage, and the switching frequency varies.

The ASL3417SHN is specified for switching frequencies from 100 kHz to 2 MHz.

Note: For all hysteresis settings, the hysteresis, specified in mV, corresponds with the lowest average LED current in the static characteristics section.

Table 9. Hysteresis channel 1 register, address 0x0Bh

Bit	Symbol	Description	Value	Function
7:2		reserved	000000	reserved; keep clear for future use
1:0	HCH1[1:0]	hysteresis channel 1	00	setting 0
			01	setting 1
			10	setting 2
			11	setting 3

Table 10. Hysteresis channel 2 register, address 0x0Ch

Bit	Symbol	Description	Value	Function
7:2		reserved	000000	reserved; keep clear for future use
1:0	HCH2[1:0]	hysteresis channel 2	00	setting 0
			01	setting 1
			10	setting 2
			11	setting 3

Table 11. Hysteresis channel 3 register, address 0x0Dh

Bit	Symbol	Description	Value	Function
7:2		reserved	000000	reserved; keep clear for future use
1:0	HCH3[1:0]	hysteresis channel 3	00	setting 0
			01	setting 1
			10	setting 2
			11	setting 3

By increasing the hysteresis level, the switching frequency is reduced, leading to less switching events and lower overall switching losses. However, the ripple of the LED current increases.

Calculation example:

A system has 40 V input voltage, an LED voltage of 15 V, a 200 mΩ R_{sense}, and an inductor of 220 µH. It operates with a hysteresis of 20 mV at:

$$f = \frac{1}{T} = \frac{1}{T_{on} + T_{off}} = \frac{1}{I_{Hyst} \cdot \frac{L}{V_{IN} - V_{LED}} + I_{Hyst} \cdot \frac{L}{V_{LED}}} = \frac{V_{IN} \cdot V_{LED} - V_{LED}^{2}}{I_{Hyst} \cdot L \cdot V_{IN}} \approx 426\ \text{kHz} \quad (3)$$

Remarks:

The calculation above does not account for delays in the switching. Due to these delays, the measured switching frequency is lower than calculated here.

To avoid that the device is operating with undesired settings, pull the PWM pin high only when a channel is completely configured.

In case the PWM functionality is not needed, it is possible to connect the PWM pin directly to pin VCC. In this case, the PWM pin control bits can be used to enable or disable the channel. To avoid operation at an undesired frequency, the hysteresis for the channel should be set before the LED current register is set.

The hysteresis and LED current level can be adapted during operation of the device to enable smooth fade-in/fade-out scenarios down to very low output currents. It does it in combination with the PWM inputs.

8.5.3 Overcurrent protection

The ASL3417SHN offers an overcurrent protection feature in addition to the set trip points to protect the system. If the output voltage suddenly changes very fast, the upper and lower hysteretic thresholds may deviate from actual target values. In case the deviation is too large the built-in overcurrent protection feature prevents the system from excessive current build-up.

In case such an event is detected, the gate driver will immediately be turned off for approximately 16 ms after which the system is restarted.

8.5.4 Output diagnostics

The diagnostic options for the outputs are:

- measurement of the output voltages during the LED on and off state - details can be found in Section 8.6
- indication that the target LED current is reached - details can be found in Section 8.11
- indication that a channel is operating with low voltage headroom - details can be found in Section 8.12.3.1

8.6 Output voltage measurement

The ASL3417SHN measures the output voltage of all channels every tmeas_per. On a transition from the PWM pin of a channel, the measurement results are stored in the corresponding registers. The registers V_LEDx_on, contain the voltage information when the PWM input of the channel is high. The registers V_LEDx_off, contain the voltage information when the PWM input is low. It ensures that the registers contain the latest

measured value of the individual channels with respect to the status of the PWM pin. If the PWM input of one channel stays constant for TLEDmeas_stat, the V_LEDx_on voltage register and the V_LEDx_off voltage register of this channel are updated.

Table 12. LED on voltage channel 1 register, address 0x20h

Bit	Symbol	Description	Value	Function
7:0	V_LED1_on[7:0]	LED on voltage channel 1	0x00h	LED on voltage = 0 V
			...	LED on voltage = 0.3548 × V_LED1_on[7:0] – 0.56 V

Table 13. LED off voltage channel 1 register, address 0x21h

Bit	Symbol	Description	Value	Function
7:0	V_LED1_off[7:0]	LED off voltage channel 1	0x00h	LED off voltage = 0 V
			...	LED off voltage = 0.3548 × V_LED1_off[7:0] – 0.56 V

Table 14. LED on voltage channel 2 register, address 0x22h

Bit	Symbol	Description	Value	Function
7:0	V_LED2_on[7:0]	LED on voltage channel 2	0x00h	LED on voltage = 0 V
			...	LED on voltage = 0.3548 × V_LED2_on[7:0] – 0.56 V

Table 15. LED off voltage channel 2 register, address 0x23h

Bit	Symbol	Description	Value	Function
7:0	V_LED2_off[7:0]	LED off voltage channel 2	0x00h	LED off voltage = 0 V
			...	LED on voltage = 0.3548 × V_LED2_off[7:0] – 0.56 V

Table 16. LED on voltage channel 3 register, address 0x24h

Bit	Symbol	Description	Value	Function
7:0	V_LED3_on[7:0]	LED on voltage channel 3	0x00h	LED on voltage = 0 V
			...	LED on voltage = 0.3548 × V_LED3_on[7:0] – 0.56 V

Table 17. LED off voltage channel 3 register, address 0x25h

Bit	Symbol	Description	Value	Function
7:0	V_LED3_off[7:0]	LED off voltage channel 3	0x00h	LED off voltage = 0 V
			...	LED on voltage = 0.3548 × V_LED3_off[7:0] – 0.56 V

8.7 External PWM input

The ASL3417SHN provides a dedicated PWM input for each of the three channels. It allows full control over the PWM frequency and duty cycle and allows phase shifting of the PWM cycles to balance the input current variations.

Pin PWM1 controls channel 1, pin PWM2 controls channel 2 and PWM3 controls channel 3. A high level at the pins represents that the corresponding channel is turned on and the configured current is delivered to the output.

As soon as the pin is pulled high, pin Gx of the corresponding channel starts toggling. It switches the MOSFET attached to the pin on and off and the system starts to deliver the configured output current.

As soon as the pin is pulled low, pin Gx of the corresponding channel is no longer turned on. The MOSFET stays off and no current is delivered to the output of the corresponding channel.

8.7.1 Control for PWM pins

The ASL3417SHN provides the option to disable the PWM input for each of the three channels individually. In case the PWM input of one channel is disabled, this channel stays off, independent of any other conditions.

The bits to disable the PWM inputs are located in the function control register (refer to Section 8.8 for details of the function control register).

8.7.2 Diagnostics for PWM functionality

The diagnostic options for the PWM functionality comprise the toggle information for the individual PWM pins. Details of the functionality can be found in Section 8.8.

8.8 Function control register

To monitor the status of the SPI interface, use the function control register. It allows a reset of the fail silent mode and offers the control of the PWM inputs.

After enabling the device, the SPI_status bit should be set. When a query returns that the bit is set, the SPI interface is operational and the device can be configured. Configuration of the device is not permitted before this bit is set.

When the device enters fail silent mode due to an error condition, bit Clr_error can be set to bring the device back into operation mode. Once the error bits are cleared, the device clears the Clr_error bit automatically. If the Clr_error bit is set, when no error is present, the Clr_error bit remains set, until an error occurs. This error is cleared automatically.

The functionality of bits PWMctrl1, PWMctrl2 and PWMctrl3, is described in Section 8.7.1.

Table 18. Function control register, address 0x00h

Bit	Symbol	Description	Value	Function
7	SPI_status	SPI status bit	0	SPI is not available
			1	SPI is operating
6	Clr_error	clear error bits	0	no pending clear request
			1	request to clear error bits and reset fail silent mode pending
5:4		reserved	0	reserved; keep clear for future use
3	PWMctrl3	PWM control for pin PWM3	0	PWM3 is disabled, channel stays off
			1	PWM3 is enabled, LED current depends on PWM state and Register settings
2	PWMctrl2	PWM control for pin PWM2	0	PWM2 is disabled, channel stays off
			1	PWM2 is enabled, LED current depends on PWM state and Register settings
1	PWMctrl1	PWM control for pin PWM1	0	PWM1 is disabled, channel stays off
			1	PWM1 is enabled, LED current depends on PWM state and Register settings
0		reserved	0	reserved; keep clear for future use

8.9 Gate voltage supply

The ASL3417SHN has an integrated linear regulator to generate the supply voltage of the gate drivers. The voltage generated by the linear regulator can be set via the VGG control register.

Table 19. VGG control register, address 0x01h

Bit	Symbol	Description	Value	Function
7:0	VGG[7:0]	VGG control	0x00h	not allowed
			...	not allowed
			0x5Dh	maximum output voltage = 10.20 V
			...	16.1 V − VGG[7:0] × 63.4 mV
			0xA6h	minimum output voltage = 5.58 V
			...	not allowed
			0xFFh	not allowed

The actual value of VGG can deviate from the target setting due to the tolerances of the VGG regulation loop (see $V_{o(reg)acc}$ in Table 42).

When a setting between 0x00h and 0x5Dh is used, the resulting gate driver target voltage exceeds the limiting values of the IC. The limiting values of the VGG pin can also be violated with target settings of 0xA6h to 0x5Dh due to these tolerances. A violation of the limiting values with the actual VGG voltage must be avoided. To ensure that only allowed settings are used for the gate driver target voltage, an immediate read back of the programmed value is required after setting the registers.

If a setting between 0xFFh and 0xA6h is used, the device may shut down and signal a BS_UV error. If the device operates, parameters of VGG are not guaranteed.

8.9.1 Gate voltage supply diagnostics

The diagnostic options for the gate voltage supply are:

- VGG available. Details can be found in Section 8.12
- VGG overload protection active. Details can be found in Section 8.12

8.10 Junction temperature information

The ASL3417SHN provides a measurement of the IC junction temperature. The measurement information is available in the junction temperature register.

Table 20. Junction temperature register, address 0x26h

Bit	Symbol	Description	Value	Function
7:0	T_junction[7:0]	junction temperature	0xD8h	device junction temperature = –40 °C
			...	device junction temperature = (256 – T_juction[7:0]) °C
			0xFFh	device junction temperature = –1 °C
			0x00h	device junction temperature = 0 °C
			0x01h	device junction temperature = 1 °C
			...	device junction temperature = T_juction[7:0]* °C
			0xAFh	device junction temperature = 175 °C

The reading of the junction temperature register should be in the range as given in Table 20. If not, the Tj_err bit (Bit 5 in diagnostic register 1, address 0x37h) can be used to indicate whether the temperature is below 175 °C (Tj_err = Low) or above 175 °C (Tj_err = High).

8.11 Bootstrap recharge mechanism

The gate drivers and current delivered to the gate pins of the ASL3417SHN is supplied by the bootstrap capacitors. These capacitors are attached between the LXx and the BSx pins of the device. To allow a proper drive of the external FET, the voltage across this capacitor must remain near the target level of the gate drive voltage.

During device operation, if the external FET switches periodically at relatively high frequency, the bootstrap capacitor is charged when the Lx node is low. It is the case when the external FET is off and the converter coil is delivering current to the output.

When the external FET is not switching periodically, the bootstrap capacitor is recharged regularly every t_{period} when:

- the PWM pin is low for more than $T_{LEDmeas\_stat}$
- the PWM is high and the CR0 bit is low

8.11.1 Bootstrap charge maintaining

There is an additional mechanism to maintain the bootstrap charge. This mechanism avoids a discharge of the bootstrap capacitors when the system is operated with long PWM off times and short PWM on times.

The ASL3417SHN compensates for the current consumption of the IC on the BS pins. As a result, the BS cap no longer discharges, but slowly settles around VBS-LX.

The compensating mechanism is enabled when the gate driver is enabled, the PWM is low, and no bootstrap undervoltage or low voltage headroom condition is detected.

8.12 Diagnostic information

Diagnostic registers contain useful information for diagnostic purposes. Details of each bit can be found in the following subchapters.

8.12.1 Diagnostic Register 1

The diagnostic register 1 contains information about the operational status of the ASL3417SHN.

Table 21. Diagnostic register 1, address 0x37h

Bit	Symbol	Description	Value	Function
7	VIN_stat	VIN status	0	VIN below under voltage detection threshold
			1	VIN above under voltage detection threshold
6	SPI_err	SPI error	0	last SPI command was executed correctly
			1	last SPI command was erroneous and has been discarded
5	Tj_err	device temperature is too high	0	device temperature below 175 °C
			1	device temperature above 175 °C

Table 21. Diagnostic register 1, address 0x37h

Bit	Symbol	Description	Value	Function
4	VGG_err	VGG error	0	VGG overload protection not active
			1	VGG overload protection has turned on and VGG is deactivated
3	VGG_ok	VGG regulation ok	0	VGG is not available
			1	VGG is available
2	I-CH3	target current reached on channel 3	0	target current was not reached during last PWM cycle
			1	target current was reached during last PWM cycle
1	I-CH2	target current reached on channel 2	0	target current was not reached during last PWM cycle
			1	target current was reached during last PWM cycle
0	I-CH1	target current reached on channel 1	0	target current was not reached during last PWM cycle
			1	target current was reached during last PWM cycle

8.12.1.1 Bit VIN_stat

The bit VIN_stat indicates the VIN voltage status of the device. This bit is set once the VIN voltage is higher than programmed under voltage threshold value. When VIN is less than the programmed under voltage threshold value, the bit is cleared (see Section 8.4 for details about the input under voltage detection functionality).

When the bit is high, the gate pins start switching. The device starts to deliver the output current as requested via the PWM inputs of the corresponding channels. The bits VGG_ok and VGG_err indicate the functional status of VGG.

When the bit is low, the VGG regulator and gate drivers are turned off. The gate pins stop switching, resulting in a turn-off of the output currents. The bit VGG_ok is reset, the bit VGG_err is not changed and the VLED measurement registers are no longer updated.

Table 22. Effect of VIN_stat on device functionality

Status of VIN	VIN_stat	VGG_ok	VGG_err	Output current	VLED measurement
below under voltage detection threshold	0	reset	cannot be set	disabled	no update
above under voltage detection threshold	1	no influence	no influence	enabled	updated when VGG_ok is 1

8.12.1.2 Bit SPI_err

The bit SPI_err indicates if some error has occurred during the last SPI transfer. When this bit is set after a write access to the device, the device discards the command. When the bit is set after a read command, the microcontroller should discard the information delivered by the device. The SPI_err bit is set in the following cases:

- SPI write is attempted to a read-only location or reserved location
- SPI read is attempted from a reserved location
- SPI command does not consist of a multiple of 16 clock counts

The SPI_err bit is cleared on a write to the diagnostic register 1.

In case a SPI_error has been detected, the device will return the diagnostic register 1 (default read) and diagnostic register 2 for the next SPI access.

8.12.1.3 Bit Tj_err

When the junction temperature rises above the maximum allowable temperature ($T_{sd(otp)}$), bit Tj_err is set high. It turns off the gate driver and the gate driver voltage regulator, and clears bit VGG_ok. If VGG_ok was already set high, bit VGG_err is set. The output current is no longer delivered. Only the SPI remains operational.

Bit Tj_err must only be cleared with the Clr_errors command when the junction temperature is below the maximum allowable temperature threshold again. Bit VGG_err, that is set together with bit Tj_err, is cleared together with bit Tj_err.

8.12.1.4 Bit VGG_err

The bit VGG_err is set when VGG cannot be regulated to its target value. During start-up, the device waits for 12 ms until the bit gets set, during normal operation the device waits only 1 ms. Once the bit is set, it turns off the gate driver, VGG voltage regulator and clears the bit VGG_ok. Consequently, output current can no longer be delivered. Only the SPI remains operational.

In case the VGG_err bit is set, the LED voltage measurement is no longer updated.

To reset the bit, the bit Clr_errors in the function control register can be set. Alternatively, the device must be set to off mode, e.g. by EN going low, or a power-on reset.

8.12.1.5 Bit VGG_ok

The bit VGG_ok is set, as soon as the VGG output is regulated to the target value. The bit is cleared on an under voltage condition at VIN, or an error on VGG.

8.12.1.6 Bit I-Ch1, I-CH2 and I-CH3

The bits I-CH1, I-CH2 and I-CH3 indicate, whether the targeted output current was reached or not in the last PWM cycle. Reasons for not reaching the target current can be e.g. an open LED string or a too low input voltage.

The bits are updated for a:

- falling edge of the PWM
- write of the CR copy pulse bit

The bits are cleared for a:

- VIN undervoltage event
- low voltage headroom event on the representative channel

8.12.1.7 CR copy pulse

The bits CCH1, CCH2 and CCH3 can be used to force an update of the LED current reached information. Setting a bit high, initiates an update of the I-CHx bit in the diagnostic register 1 and clears the CR0_CHx bit. The device automatically clears the bit that was set high, after the update.

Table 23. CR copy pulse register, address 0x06h

Bit	Symbol	Description	Value	Function
7:3		reserved	000000	reserved; keep clear for future use
2	CCH3	update request for bit I-CH3	0	no pending update request
			1	update request for bit I-CH3
1	CCH2	update request for bit I-CH2	0	no pending update request
			1	update request for bit I-CH2
0	CCH1	update request for bit I-CH1	0	no pending update request
			1	update request for bit I-CH1

8.12.2 Diagnostic register 2

The diagnostic register 2 contains the PWM toggle information of the ASL3417SHN.

Table 24. Diagnostic register 2, address 0x36h

Bit	Symbol	Description	Value	Function
7		reserved	0	reserved; keep clear for future use
6		reserved	1	reserved; keep clear for future use
5		reserved	000	reserved; keep clear for future use
4	NVM_fail	NVM_access failed	0	no NVM access failed
			1	NVM access failed
3	NVM_ok	NVM_access completed	0	no NVM access completed
			1	NVM access completed
2	PWM3	toggle information for pin PWM3	0	PWM3 has not toggled since last time the register was read
			1	PWM3 has toggled since last time the register was read
1	PWM2	toggle information for pin PWM2	0	PWM2 has not toggled since last time the register was read
			1	PWM2 has toggled since last time the register was read
0	PWM1	toggle information for pin PWM1	0	PWM1 has not toggled since last time the register was read
			1	PWM1 has toggled since last time the register was read

8.12.2.1 Bit NVM_fail

When the ASL3417SHN rejects the write to the particular NVM address location, bit NVM_fail is set. The bit is reset on a write to diagnostic register 2.

8.12.2.2 Bit NVM_ok

When the ASL3417SHN accepts the write/read to/from the particular NVM address location and the write/read process is completed, the NVM_ok bit is set. The bit is reset on a write to diagnostic register 2.

8.12.2.3 PWM toggle information (bits PWM1, PWM2 and PWM3)

To allow the detection of errors in the control of the PWM pins, the ASL3417SHN allows some diagnostics of the PWM inputs via diagnostic register 2. This register contains the toggle information of the PWM inputs.

The bits are set when a change in the level of the pin is detected. The bits are reset on a write to diagnostic register 2.

8.12.3 Diagnostic register 3

Diagnostic register 3 contains the low voltage headroom warning information and the output current state bits.

8.12.3.1 Low voltage headroom warning

When the ASL3417SHN operates with low voltage headroom, it could lead to very high duty cycles. Subsequent long on-times for the external FET, could result in low switching frequencies. To avoid long on-times of the external FET, the supply voltage and output voltages are continuously monitored while the channel is on and VIN_stat is high. Once the output voltage is measured to be above V_{in} minus V_{Head_low}, the gate pin is pulled low. It results in the FET being turned off. At the same moment in time, the low voltage headroom bit (LV_CHx in diagnostic register 3) for the corresponding channel is set.

If the voltage difference is again above V_{Head_low}, the device starts to operate again.

Bits LV_CH1, LV_CH2 and LV_CH3 remain set until a write to the diagnostic register 3 is performed. If the bits are cleared while the channels are turned off or VIN_stat is low, the bits might be set again if the last sampled voltage indicates a low voltage headroom condition.

8.12.3.2 Output current state

Diagnostic register 3 also contains bits CR0_CH1, CR0_CH2 and CR0_CH3. The bits indicate the target current reached information of the individual channels for the current PWM cycle.

The bits are set as soon as the target current of the channel is reached.

The bits are cleared under the following conditions:

- a falling edge on the PWM pin
- a VIN under voltage event
- a CR0 copy pulse request via SPI
- the gate is driven high for more than 1 ms while PWM is high

8.12.3.3 Register content

Table 25. Diagnostic register 3, address 0x35h

Bit	Symbol	Description	Value	Function
7:6		reserved	00	reserved; keep clear for future use
5	CR0_CH3	current reached CH3	0	output current is not reached
			1	output current is reached
4	CR0_CH2	current reached CH2	0	output current is not reached
			1	output current is reached
3	CR0_CH1	current reached CH1	0	output current is not reached
			1	output current is reached
2	LV_CH3	low voltage headroom in CH3	0	no low headroom event occurred
			1	at least one low headroom event occurred

Table 25. Diagnostic register 3, address 0x35h

Bit	Symbol	Description	Value	Function
1	LV_CH2	low voltage headroom in CH2	0	no low headroom event occurred
			1	at least one low headroom event occurred
0	LV_CH1	low voltage headroom in CH1	0	no low headroom event occurred
			1	at least one low headroom event occurred

8.12.4 Diagnostic register 4

Diagnostic register 4 contains the BS undervoltage detection bits.

8.12.4.1 Bootstrap undervoltage detection

The integrated bootstrap undervoltage detection monitors the voltage between the BS and the LX pins during the off time of the LX pin. If the voltage drops below VBS_UV, the ASL3417SHN prevents the gate from being turned-on and prevent the MOSFET being driven at a low voltage.

When this condition is detected on a channel, the channel is turned off and the appropriate error bit is set. A write command to the device clears the error bit and any bits to be cleared are set high. Once the error is cleared, the channel is enabled again.

Table 26. BS_UV register - read access, address 0x34h

Bit	Symbol	Description	Value	Function
7:3		reserved	00000	reserved; keep clear for future use
2	BS_UV3	low BS warning CH3	0	no low BS event occurred
			1	at least one low BS event occurred
1	BS_UV2	low BS warning CH2	0	no low BS event occurred
			1	at least one low BS event occurred
0	BS_UV1	low BS warning CH1	0	no low BS event occurred
			1	at least one low BS event occurred

Table 27. BS_UV register - write access, address 0x34h

Bit	Symbol	Description	Value	Function
7:3		reserved	00000	reserved; keep clear for future use
2	BS_UV3	low BS warning CH3	0	no action
			1	clear low BS warning for channel 3
1	BS_UV2	low BS warning CH2	0	no action
			1	clear low BS warning for channel 2
0	BS_UV1	low BS warning CH1	0	no action
			1	clear low BS warning for channel 1

8.13 Limp-home mode

The ASL3417SHN offers a Limp-home mode and the detection of a loss of SPI communication, activates it. In Limp-home mode, the outputs are operating according to a pre-defined condition stored in a non-volatile memory (NVM). Figure 4 shows the operation state diagram of the Limp-home mode and Table 28 gives an overview of the behavior of the ASL3417SHN in the states.

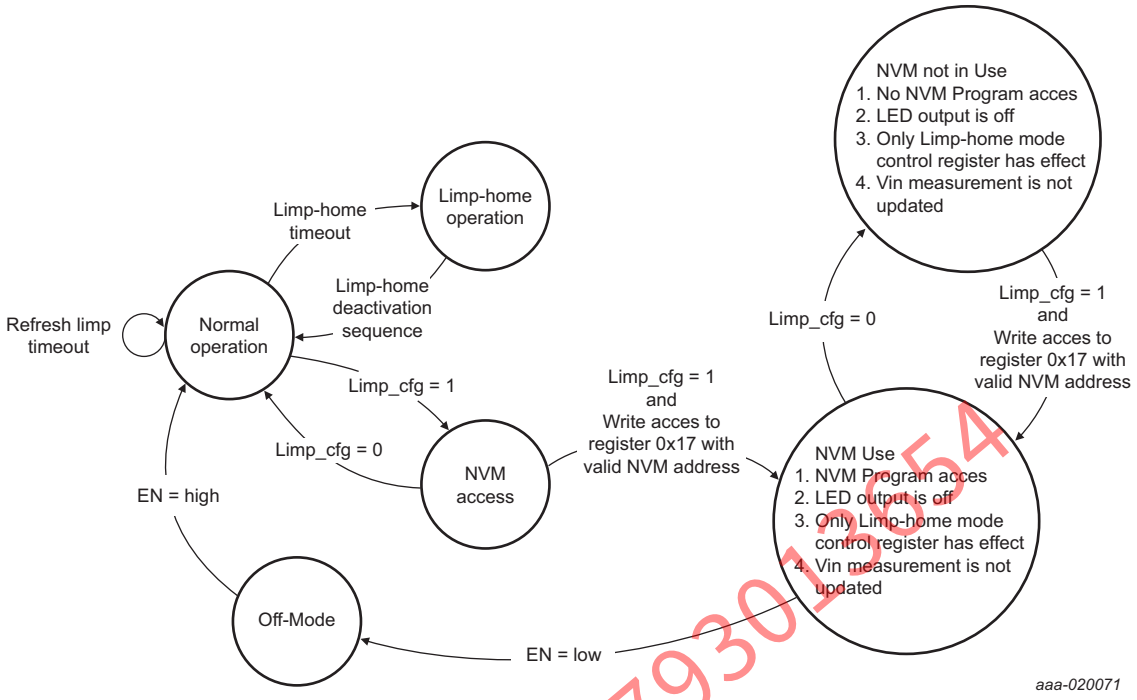


Fig 4. Limp-home state diagram

Table 28. Limp-home state overview

Mode	Outputs	Register access	MTP access	Remark
Normal operation	as defined via registers and PWM input	full access to SPI registers	no	normal operation consists of operation, undervoltage and fail silent mode (see Figure 3)
Limp-home operation	as defined per limp-home configuration	write to limp home control register allowed; other control registers are set to the NVM values.	no	limp-home operation offers same states as normal operation mode
NVM access	as defined via registers and PWM input	full access to SPI registers	no	once NVM access mode is entered, the limp-home refresh timer is stopped.
NVM Use	outputs disabled	SPI registers are programmable but values have no effect	read/write	to restart it, a power-on reset via EN is required
NVM not in use	outputs disabled	SPI registers are programmable but values have no effect	no	the use of this state is not recommended

The settings with which the device operates in limp-home settings can be configured in NVM Use mode. In NVM Use mode, the outputs are disabled. After configuration, the limp-home settings will be permanently stored. Once the ASL3417SHN detects a loss of the communication, the device populates these settings into the registers and operates according to them.

In case the system recovers from the error, Limp-home mode can be left via the exit Limp-home mode sequence. With the completion of the exit sequence, the device already operates according to the applied levels on the PWM pin inputs. The configuration registers are open for write configuration again.

Limp-home and normal mode operation offer the same operational behavior. It includes the undervoltage behavior as well as the fails silent behavior. When the fail silent mode is entered, the system cannot execute an automatic recovery in either the normal operation mode or the Limp-home mode.

8.13.1 Limp-home mode activation

Limp-home mode is automatically entered if no write to the Limp-home mode exit bits (register 0x33h, bits 6:4) with data 111, is executed for the time-out time. The time-out time is defined in the Limp-home mode control register.

8.13.2 Limp-home mode operation

Once the system has entered Limp-home mode, the ASL3417SHN switches to the configuration as defined in the NVM memory for Limp-home mode. The ASL3417SHN modifies the control registers accordingly. During Limp-home mode operation, the SPI interface remains functional, but only the Limp-home mode control register can be written. The other registers offer only read access.

8.13.3 Limp-home mode deactivation

To deactivate Limp-home mode, a dedicated Limp-home mode deactivation sequence must be written to the Limp-home mode control register.

Table 29. Limp-home mode deactivation sequence

Deactivation step	Data to Limp_exit [2:0]
step 1	001
step 2	010
step 3	100

Once the deactivation sequence is completed, the ASL3417SHN immediately starts to react on the PWM inputs. The registers remain as set for the Limp-home mode. As the system is now back to operation mode, all registers are accessible as defined for operation mode again.

8.13.4 Limp-home mode control register

The Limp-home mode control register allows control of the Limp-home mode.

Table 30. Limp-home mode control register, address 0x33h

Bit	Symbol	Description	Value	Function
7	Limp_status	Limp-home mode status	0	device is not in limp-home mode
			1	device is in limp-home mode
6:4	Limp_exit	Limp-home mode exit bits[1]	...	bits for limp home mode deactivation sequence and SPI time-out trigger

Table 30. Limp-home mode control register, address 0x33h *...continued*

Bit	Symbol	Description	Value	Function
3:1	Limp_timeout	time-out setting for activation of limp-home mode[2]	000	Limp-home time-out setting 1
			001	Limp-home time-out setting 2
			010	Limp-home time-out setting 3
			011	Limp-home time-out setting 4
			100	Limp-home time-out setting 5
			101	Limp-home time-out setting 6
			110	Limp-home time-out setting 7
			111	Limp-home time-out setting 8
0	Limp_cfg	Limp-home mode configuration mode	0	not in limp-home mode configuration mode
			1	system in limp-home mode configuration mode

[1] When refreshing the time-out timer, the limp home mode time-out setting must be written as well

[2] When changing the limp home mode time-out setting, the limp_exit bits should be set to 111 to refresh the time-out timer

8.13.5 NVM Write Sequence

The limp home configuration of the ASL3417SHN can be stored in a non-volatile-memory (NVM). In NVM Use mode, data can be written to the NVM using the following sequence:

1. Clear the previous NVM bits by writing the Diagnostic Summary Register 2 (address 0x36h) with any data.
2. Write required NVM data [7:0] into SPI register 0x18h.
3. Write required NVM data [15:8] into SPI register 0x19h.
4. Finally, to start the programming process, write the NVM address into SPI register 0x17h with bit NVM_write set high.
   a. If access to the NVM is allowed at these address locations, the ASL3417SHN programs the NVM memory. After programming, the bit NVM_ok is set.
   b. If access to the NVM is not allowed at these address locations, the ASL3417SHN does not modify the NVM memory and set bit NVM_fail high.
5. The next operation can be initiated after the NVM write is completed.

8.13.6 NVM read sequence

The limp-home configuration of the ASL3417SHN can be stored in a non-volatile-memory (NVM). To read data to the NVM, use the following sequence:

1. Clear the previous NVM bits by writing the Diagnostic Summary Register 2 (address 0x36h) with any data.
2. To start the read process, write the NVM address into SPI register 0x17h with bit NVM_read set high.
3. Obtain the read completion status by reading the Diagnostic Summary Register 2 (0x36h).
4. NVM data [7:0] is now available via SPI register 0x28h.
5. NVM data [15:8] is now available via SPI register 0x29h.
6. The next operation can be initiated after the NVM read is completed.

8.13.7 NVM register map

The ASL3417SHN allows limp home values for all control registers that can be configured during normal operation to be set. Table 31 links the NVM addresses to the register addresses.

Table 31. Mapping of NVM registers to control registers

NVM address linked to SPI register 0x17h [4:0]	NVM data linked to SPI register 0x19h [15:8][1]	NVM data linked to SPI register 0x18h [7:0][1]
0x10h	LED current channel 2 (SPI register address 0x03h) default: 0x00h	LED current channel 1 (SPI Register Address 0x02h) default: 0x00h
0x11h	VGG control (SPI register address 0x01h), default: 0x96h	LED current channel 3 (SPI Register Address 0x04h) default: 0x00h
0x12h	NVM_Hyst, default: 0x00h (see Table 32)	Under voltage threshold (SPI Register Address 0x0Fh) default: 0x00h
0x13h	-	NVM_PWM_ctrl, default: 0x2Ah (see Table 32)

[1] Register 0x18h and 0x19h are used for write to NVM and register 0x28h and 0x29h are used for read from NVM.

The content NVM Data fields that contain more than just one register are shown in Table 32.

Table 32. Overview of multi-content NVM data fields

NVM_ Address	Name	7	6	5	4	3	2	1	0
0x12h; Data[15:8]	NVM_Hyst	LED current range _CH2 (SPI register address 0x05h bit 1)	LED current range _CH1 (SPI register address 0x05h bit 0)	[4:5] Hysteresis channel 3 (SPI register address 0x0Dh)		[2:3] Hysteresis channel 2 (SPI register address 0x0Ch)		[1:0] Hysteresis channel 1 (SPI register address 0x0Bh)	
0x13h; Data[7:0]	NVM_PWM _ctrl	-	NVM_PWM3[1:0] (see Table 33)		NVM_PWM2[1:0] (see Table 33)		NVM_PWM1[1:0] (see Table 33)		LED Current Range _CH3 (SPI Register Address 0x05h bit 2)

In Limp-home mode, the ASL3417SHN offers the option to override the PWM input to turn channels individually ON, OFF, or allow them to react to pin PWM. Table 33 shows the possible configurations of the channels during Limp-home mode.

Table 33. NVM_PWMx bits

NVM_PWMx[1:0]	Channel reaction
00	Channel x is turned off in limp home mode
01	Channel x reacts to PWMx in limp home mode
10	Channel x is turned on in limp home mode
11	Channel x reacts to PWMx in limp home mode

8.14 SPI

The ASL3417SHN uses an SPI interface to communicate with an external microcontroller. The SPI interface can be used for setting the LEDs current, reading and writing the control register.

8.14.1 Introduction

The Serial Peripheral Interface (SPI) provides the communication link with the microcontroller, supporting multi-slave operations. The SPI is configured for full duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing the application to read back the registers without changing the register content.

The SPI uses four interface signals for synchronization and data transfer:

- CSB - SPI chip select; active LOW
- SCLK - SPI clock - default level is LOW due to low-power concept
- SDI - SPI data input
- SDO - SPI data output - floating when pin CSB is HIGH

Bit sampling is performed on the falling clock edge and data is shifted on the rising clock edge as illustrated in Figure 5.

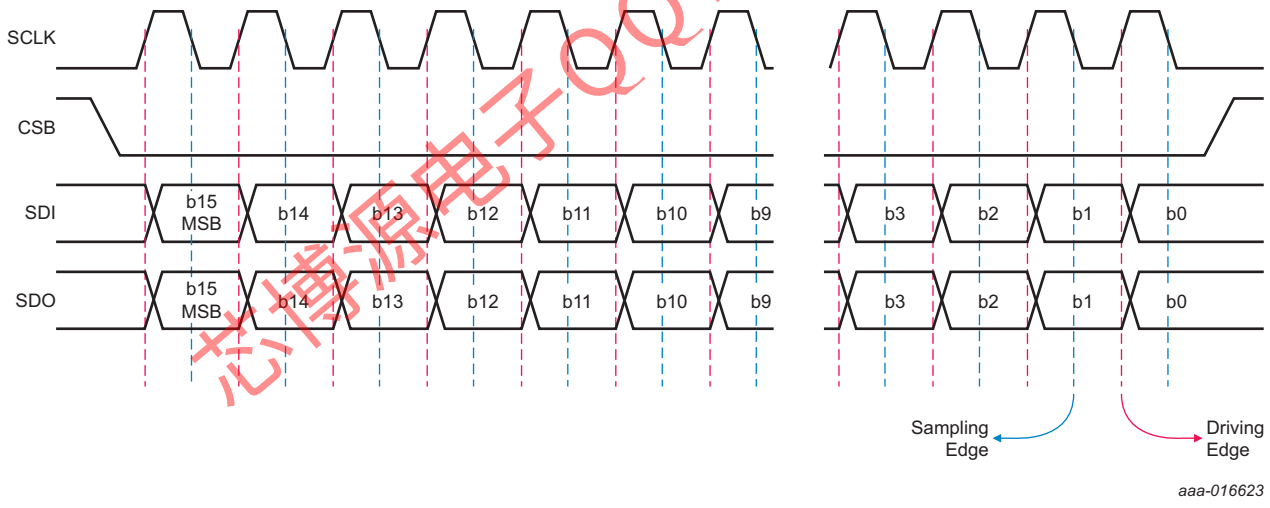


Fig 5. SPI timing protocol

The data bits of the ASL3417SHN are arranged in registers of 1 byte length. Each register is assigned to a 7-bit address. For writing into a register, 2 bytes must be sent to the LED driver. The first byte is an identifier byte that consists of the 7-bit address and one read-only bit. For writing, the read-only bit must be set to “0”. The second byte is the data that shall be written into the register. So an SPI access consists of at least 16 bits.

Figure 6 together with Table 34 and Table 35 demonstrate the SPI frame format.

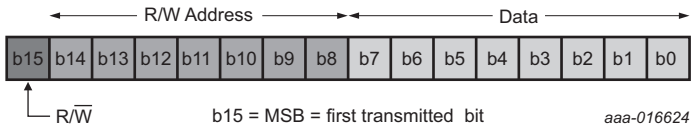


Fig 6. SPI frame format

Table 34. SPI frame format for a transition to the device

Bit	Symbol	Description	Value	Function
15	b15	R/W bits	0	write access
			1	read access
14:8	b14:8	address bits	...	selected address
7:0	b7:0	data bits	...	transmitted data

Table 35. SPI frame format for a transition from the device

Bit	Symbol	Description	Value	Function
15:8	b15:8	diagnostic register 1	...	content of diagnostic register 1
7:0	b7:0	data bits	...	when previous command was a valid read command, content of the register that is supposed to be read
			...	When previous command was a valid write command, new content of the register that was supposed to be written

Note: The first SPI command after a leaving of off mode returns 0x00h.

The Master initiates the command sequence. The sequence begins with CSB pin pulled low and lasts until it is asserted high.

The ASL3417SHN also tolerates SPI accesses with a multiple of 16 bits. It allows a daisy chain configuration of the SPI.

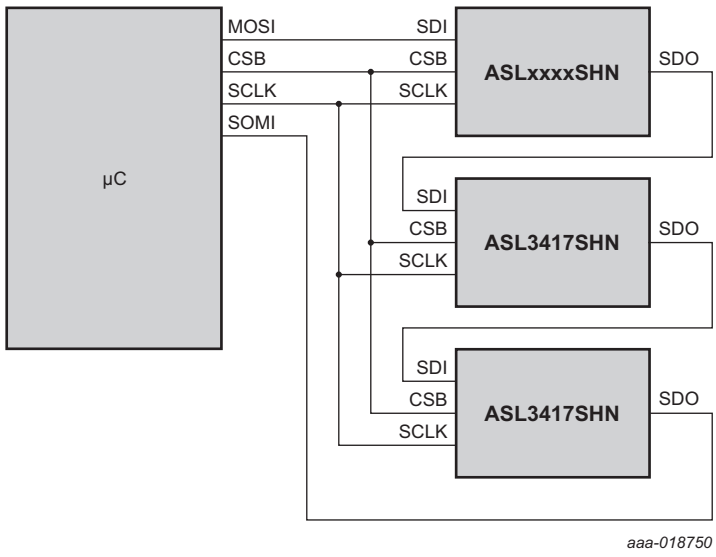


Fig 7. Daisy chain configuration

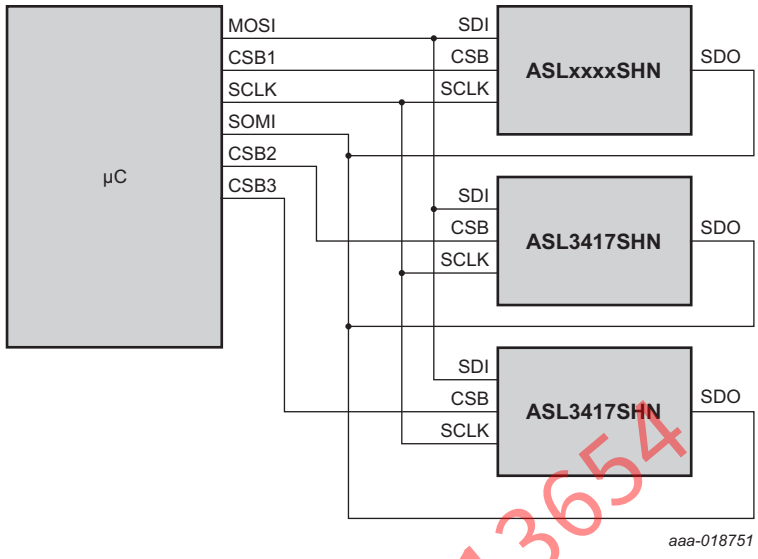


Fig 8. Physical parallel slave connection

During the SPI data transfer, the identifier byte and the actual content of the addressed registers is returned via the SDO pin. The same happens for pure read accesses. Here the read-only bit must be set to 1. The content of the data bytes that are transmitted to the ASL3417SHN is ignored.

The ASL3417SHN monitors the number of data bits that are transmitted. If the number is not 16, or a multiple of 16, then a write access is ignored and the SPI error indication bit is set.

8.14.2 Typical use case illustration (write/read)

Consider a daisy chain scheme with one master connected to 4 slaves in Daisy chain fashion. The following commands are performed during one sequence (first sequence).

- write data 0xFF to register 0x1A slave 1
- read from register 0x02 of slave 2
- write data 0xAF to register 0x2F of slave 3
- read from register 0x44 of slave 4

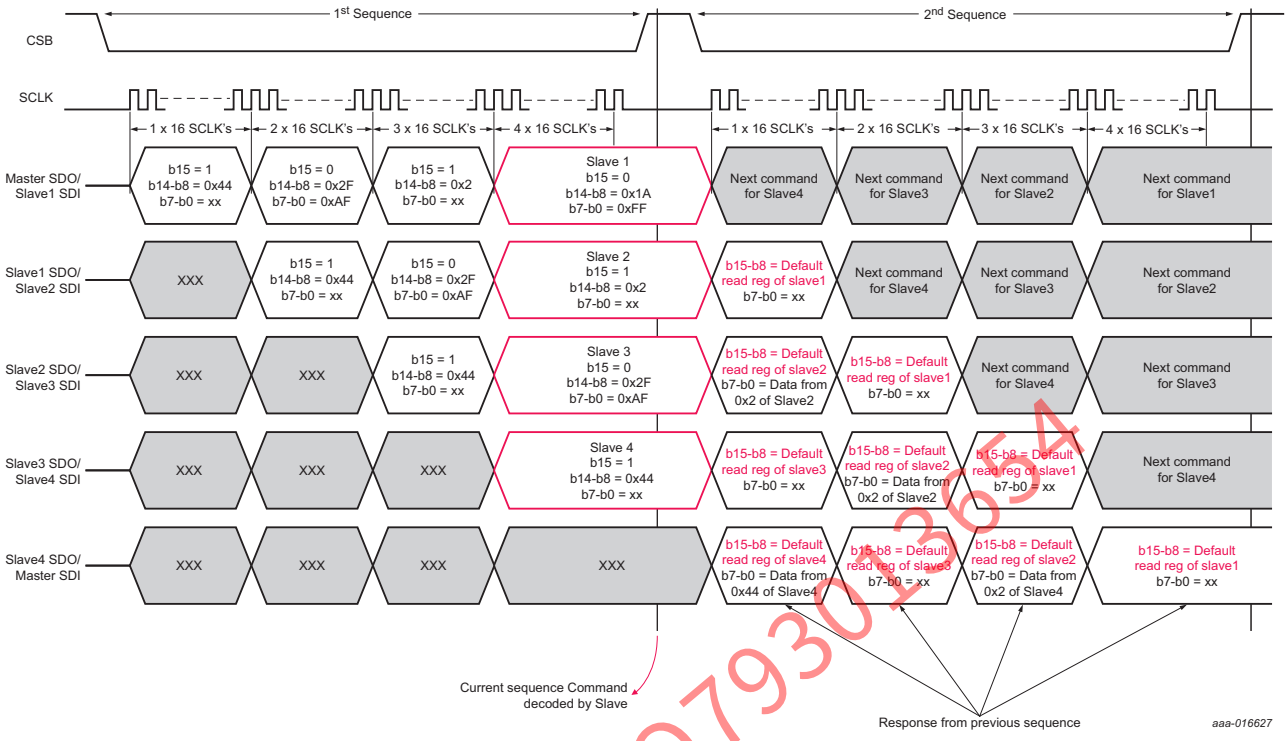


Fig 9. SPI frame format

8.14.3 Diagnostics for the SPI interface

The diagnostic options for the SPI interface are Error during last SPI transfer. For details, refer to Section 8.11.

8.14.4 Register map

The addressable register space amounts to 128 registers from 0x00 to 0x7F. They are separated in two groups as shown in Table 36. The register mapping is shown in Table 37 and Table 38. The functional description of each bit can be found in the dedicated chapter.

Table 36. Grouping of the register space

Address range	Description	Content
0x00 ... 0x1F	control registers	thresholds, LED currents
0x20 ... 0x7F	diagnostic registers	LED voltages, PWM toggle information

8.14.4.1 Control registers

Table 37 provides an overview of the control registers and their reset state.

Table 37. Control register group overview

Address	Name	Reset value	7	6	5	4	3	2	1	0
0x00h	function control	0x0Eh	SPI_status	Clr_errors	-	-	PWMctrl 3	PWMctrl 2	PWMctrl 1	-
0x01h	VGG control	0x96h	VGG[7:0]							
0x02h	LED current channel 1	0x00h	I_LED_CH1[7:0]							

Table 37. Control register group overview *...continued*

Address	Name	Reset value	7	6	5	4	3	2	1	0
0x03h	LED current channel 2	0x00h	I_LED_CH2[7:0]							
0x04h	LED current channel 3	0x00h	I_LED_CH3[7:0]							
0x05h	LED current range	0x07h	-	-	-	-	-	I_CH3	I_CH2	I_CH1
0x06h	CR copy pulse	0x00h	-	-	-	-	-	CCH3	CCH2	CCH1
0x0Bh	hysteresis channel 1	0x03h	-	-	-	-	-	-	HCH1[1:0]	
0x0Ch	hysteresis channel 2	0x03h	-	-	-	-	-	-	HCH2[1:0]	
0x0Dh	hysteresis channel 3	0x03h	-	-	-	-	-	-	HCH3[1:0]	
0x0Fh	undervoltage threshold	0xFFh	V_VIN_UV[7:0]							
0x33h	limp-home control	0x0Eh	limp_status	limp_exit[2:0]			Limp_timeout[0:2]			limp_cfg

8.14.4.2 Diagnostic registers

Table 38 provides an overview of the diagnostic registers. As the device continuously updates these registers, they do not have a default value.

Table 38. Diagnostic register group overview

Address	Name	7	6	5	4	3	2	1	0
0x20h	LED on voltage channel 1	V_LED1_on[7:0]							
0x21h	LED off voltage channel 1	V_LED1_off[7:0]							
0x22h	LED on voltage channel 2	V_LED2_on[7:0]							
0x23h	LED off voltage channel 2	V_LED2_off[7:0]							
0x24h	LED on voltage channel 3	V_LED3_on[7:0]							
0x25h	LED off voltage channel 3	V_LED3_off[7:0]							
0x26h	junction temperature	T_junction[7:0]							
0x34h	diagnostic register 4	-	-	-	-	-	BS_UV3	BS_UV2	BS_UV1
0x35h	diagnostic register 3	-	-	CR0_CH 3	CR0_CH 2	CR0_CH 1	LV_CH3	LV_CH2	LV_CH1
0x36h	diagnostic register 2	-	1	-	NVM_fail	NWM_ok	PWM3	PWM2	PWM1
0x37h	diagnostic register 1 (default read register)	VIN_Stat	SPI_er	Tj_er	VGG_er	VGG_ok	I-CH3	I-CH2	I-CH1
0x38h	VIN voltage measurement[1]	V_VIN[7:0]							

[1] A write to the VIN voltage measurement register sets the SPI error bit high.

8.14.4.3 NVM registers

Table 39 provides an overview of the registers that control the NVM.

Table 39. NVM register group overview

Address	Name	7	6	5	4	3	2	1	0
0x17h	NVM control	NVM_read	NVM_write	-	NVM_adress				
0x18h	NVM write data 1	NVM Data1[7:0]							
0x19h	NVM write data 2	NVM Data2[7:0]							
0x28h	NVM read data 1	NVM Data1[7:0]							
0x29h	NVM read data 2	NVM Data2[7:0]							

9. Limiting values

Table 40. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	voltage on pin VIN	EN = low	−0.3	+80	V
		EN = high	10	80	V
V_{VCC}	voltage on pin VCC		−0.3	+5.5	V
$V_{I(dig)}$	digital input voltage	voltage on pins SDO, SDI, CSB, SCLK, EN, PWM1, PWM2 and PWM3	−0.3	+5.5	V
V_{VGG}	voltage on pin VGG		−0.3	+10	V
V_{LX}	voltage on pin LX	LX1, LX2 and LX3	−1.0	+80	V
$SR_{f(max)}$	maximum falling edge slew rate	on pins LX1, LX2 and LX3; at maximum input voltage	-	5.0	V/ns
V_{sense}	sense voltage	voltage on sense pins RH1, RL1, RH2, RL2, RH3 and RL3	−1.0[1]	+70[2]	V
$V_{RH-RL(max)}$	maximum voltage drop between pins RH and RL	maximum drop between the RH and RL pins of one channel	−0.3	+0.8	V
V_{BSx}	voltage on bootstrap pins	BS1, BS2 and BS3	−0.3	+90	V
V_{Gx}	voltage on gate pins	G1, G2 and G3	−1.0	+90	V
ΔV_{max}	maximum voltage difference	between pins G and LX of one channel	-	12	V
		between pins BS and LX of one channel	-	12	V
T_j	junction temperature		−40	+175	°C
		during programming of NVM	0	+85	°C
T_{stg}	storage temperature		−55	+175	°C
$N_{endu(W\_ER)}$	write or erase endurance	number of NVM programming cycles	-	200	
V_{ESD}	electrostatic discharge voltage	HBM[3]			
		at any pin	−2	+2	kV
		at pins RLx with 100 nF at pin	−6	+6	kV
		IEC 61000-4-2[4]			
		at pins RLx with 100 nF at pin	−6	+6	kV
		CDM[5]			
		at any pin	−500	+500	V

[1] The limitation of the slew rate is an IC constraint. When the IC is operating in an application circuit, the external circuitry influences the slew rate capability. An example guideline for some specific MOSFET parameters to be considered when selecting the appropriate resistor values, can be found in the table below. Nonetheless, each application should be validated to determine the final solution when considering EMC performance and correct gate driver operation.

[2] 76 V for $t \leq 10$ seconds guaranteed by design.

[3] Human Body Model (HBM): according to AEC-Q100-002 (100 pF, 1.5 kΩ).

[4] IEC 61000-4-2 (150 pF, 330 Ω).

[5] Charged Device Model (CDM): according to AEC-Q100-011 (field Induced charge; 4 pF).

9.1 External circuitry

Table 41. Guideline for external circuitry

Symbol	Component	MOSFET configuration typical values			Unit
		Config. 1	Config. 2	Config. 3	
R_G	[1]	1.0	4.7	1.7	Ω
Q_{GS}	[1]	0.6	1.2	0.8	nC
Q_{GD}	[1]	0.9	1.8	1.2	nC
R_{DSon}	[1]	175	80	72	mΩ
R_{gate}	gate resistor	33	15	33	Ω
RLx	sense resistor low side channel	10	10	10	Ω
C5		1	1	1	µF

[1] MOSFET M5

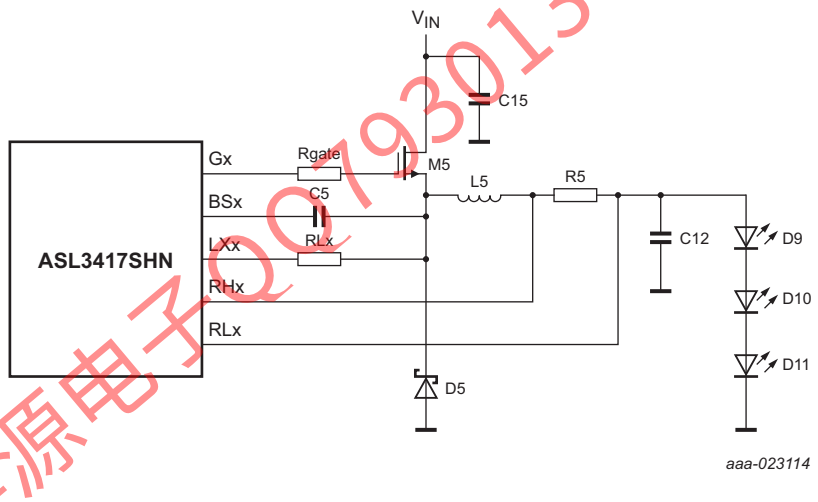


Fig 10. External components

10. Thermal characteristics

10.1 Thermal model of the ASL3417SHN

The ASL3417SHN has several power sources on the die, but for thermal modeling they can be simplified to one generic power source.

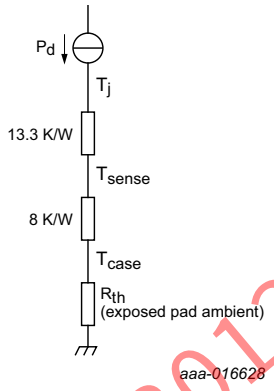


Fig 11. Thermal model of the ASL3417SHN

The power can be calculated using Equation 4 and Equation 5:

$$I_{gates} = fsw1 \times Qg1 + fsw2 \times Qg2 + fsw3 \times Qg3 \quad (4)$$

$$P_d = V_{Vin} \times (3.5\ mA + 1.3\ mA \times \#channels\_active + I_{gates}) + V_{VCC} \times 10\ mA \quad (5)$$

Note, the T_{sense} is the location of the IC internal temperature measurement. The location of the sensor, makes it possible that the junction temperature has already exceeded 175 °C, even though the temperature measurement returns a value lower than 175 °C.

11. Static characteristics

Table 42. Static characteristics

Min and Max values are specified for the following conditions: V_{VIN} = 10 V to 80 V, V_{EN} = 4.5 V to 5.5 V, V_{VCC} = 4.5 V to 5.5 V and T_j = −40 °C to +175 °C.[1] All voltages are defined with respect to ground, positive currents flow into the IC. Typical values are given at V_{VIN} = 40 V. V_{EN} = 5 V, V_{VCC} = 5 V and T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	supply current	on pin VIN; operating no load on gate and VGG not set	-	3.5	10	mA
		current on pin EN when EN = high	-	-	150	µA
I_{off}	off-state current	EN = low; V_{IN} < 12 V	-	-	5	µA
Supply pin VCC						
I_{VCC}	supply current on pin VCC	EN = high; CSB = low	-	10	15	mA
$V_{UVLO(VCC)}$	undervoltage lockout on pin VCC	[2]	3.7	-	4.4	V
Enable pin EN						
$V_{UVLO(EN)}$	undervoltage lockout on pin EN	[2]	3.7	-	4.4	V
LED output characteristics						
$V_{O(LED)}$	LED output voltage	LED1; $V_{IN} \geq V_{O(LED)} + V_{hr(low)}$	2.5	-	70	V
		LED2; $V_{IN} \geq V_{O(LED)} + V_{hr(low)}$	2.5	-	70	V
		LED3; $V_{IN} \geq V_{O(LED)} + V_{hr(low)}$	2.5	-	70	V
$V_{O(min)}$	minimum output voltage	average values				
		setting 0	5	-	11	mV
		setting 1	13	-	21	mV
		setting 2	22	-	31	mV
		setting 3	32	-	42	mV
$I_{O(LED)}$	LED output current	nominal average; $V_{O(LED)}$ = 2.5 V to 70 V; $V_{IN} \geq V_{O(LED)} + V_{off(hr)low}$; R_{sense} = 200 mΩ	$V_{O(min)}/R_{sense}$	-	1500	mA
$V_{sense(AV)acc}$	average sense voltage accuracy	I_CHx = 1; $V_{sense(AV)} \geq$ 24 mV [3]	−4	-	+4	%
		I_CHx = 0; $V_{sense(AV)} \geq$ 120 mV [3]	−4	-	+4	%
$V_{O(acc)}$	output voltage accuracy	related to currently applied value	$-0.02 \times V_{LEDx} - 1.0644$ V	-	$+0.02 \times V_{LEDx} + 1.0644$ V	%
			$-0.02 \times V_{VIN} - 1.0644$ V	-	$+0.02 \times V_{VIN} + 1.0644$ V	%
$V_{off(hr)low}$	low headroom turn-off voltage	$V_{IN} - V_{O(LED)}$	5	-	7	V
V_{ocp}	overcurrent protection voltage		-	400	-	mV
VGG output characteristics (C_{VGG} = 1 µF, ESR ≤ 0.1 Ω)						
$V_{O(reg)}$	regulator output voltage		4.5	-	10.04	V
$V_{O(reg)acc}$	regulator output voltage accuracy		−5	-	+5	%
$V_{do(reg)}$	regulator dropout voltage	$I_{reg} \leq$ 50 mA; regulator in saturation	-	0.5	1.0	V
		$I_{reg} \leq$ 160 mA; regulator in saturation	-	1.6	3.2	V

Table 42. Static characteristics *...continued*

Min and Max values are specified for the following conditions: V_{VIN} = 10 V to 80 V, V_{EN} = 4.5 V to 5.5 V, V_{VCC} = 4.5 V to 5.5 V and T_j = −40 °C to +175 °C.[1] All voltages are defined with respect to ground, positive currents flow into the IC. Typical values are given at V_{VIN} = 40 V. V_{EN} = 5 V, V_{VCC} = 5 V and T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bootstrap characteristics; pins BS1, BS2 and BS3 (capacitance between BS and LX pins = 1 µF)						
$V_{d(bs)}$	bootstrap diode voltage	$I_{bs} \leq 100$ mA	-	-	1.5	V
I_{bs}	bootstrap current	current consumption of gate driver; output is turned on	-	300	-	µA
$V_{th(bs)OV}$	bootstrap overvoltage detection threshold		5.5	-	8	V
$V_{th(bs)UV}$	bootstrap undervoltage detection threshold		3.5	4.5	5.3	V
PWM inputs; pins PWM1, PWM2 and PWM3						
$V_{th(sw)}$	switching threshold voltage		0.7	-	3.5	V
$R_{pd(int)}$	internal pull-down resistance		50	-	130	kΩ
Serial peripheral interface inputs; pins SDI, SCLK and CSB						
$V_{th(sw)}$	switching threshold voltage		0.7	-	3.5	V
$V_{th(sw)hys}$	switching threshold voltage hysteresis		0.1	-	1.1	V
I_{IL}	LOW-level input current		−10	-	+10	µA
I_{IH}	HIGH-level input current		15	40	110	µA
$R_{pd(int)SCLK}$	internal pull-down resistance on pin SCLK		50	-	130	kΩ
$R_{pd(int)CSB}$	internal pull-down resistance on pin CSB		50	-	130	kΩ
$R_{pd(int)SDI}$	internal pull-down resistance on pin SDI		50	-	130	kΩ
Serial peripheral interface data output; pin SDO						
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	0.9 × V_{VCC}	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.1 × V_{VCC}	V
I_{OH}	HIGH-level output current		−30.0	-	−1.6	mA
I_{OL}	LOW-level output current		1.6	-	30.0	mA
I_{LOZ}	OFF-state output leakage current	$V_{CSB} = V_{VCC}$; V_O = 0 V to V_{VCC}	−5	-	+5	µA
Temperature protection						
$T_{sd(otp)}$	overtemperature protection shutdown temperature		165	175	185	°C
ΔT_j	junction temperature deviation	T_j = 130 °C; measurement provided via register 0x26h [4]	−5	-	+5	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Undervoltage lockout pulls the gate pins low but the other functions of the IC remain operational.

[3] Excluding influence of load and line regulation due to total delay of gate driver and comparators of hysteretic converter.

[4] Guaranteed by wafer testing at 125 °C.

12. Dynamic characteristics

Table 43. Dynamic characteristics

Min and Max values are specified for the following conditions: V_{VIN} = 10 V to 80 V, V_{EN} = 4.5 V to 5.5 V, V_{VCC} = 4.5 V to 5.5 V and T_j = −40 °C to +175 °C. All voltages are defined with respect to ground, positive currents flow into the IC. Typical values are given at V_{VIN} = 40 V. V_{EN} = 5 V and V_{VCC} = 5 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PWM}	PWM frequency		100	-	1000	Hz
Δ_{PWM}	PWM duty cycle		0	-	100	%
$t_{d(on)PWM}$	PWM turn-on delay time	90 % of LED current	-	-	100	µs
$t_{d(off)PWM}$	PWM turn-off delay time	10 % of LED current	-	-	100	µs
$t_{d(i)PWM}$	PWM input delay time	including start-up time of the boost	-	20	-	ms
f_{DCDC}	DC-to-DC frequency		100	-	2000	kHz
$t_{on(max)drv(G)}$	maximum on time of one gate driver		-	1	-	ms
$t_{d(drv)G}$	gate driver delay time	total delay of gate driver and comparators of hysteretic converter [1]	25	-	75	ns
		total delay of gate driver and comparators of hysteretic converter [2]	10	-	75	ns
t_{blank}	blanking time	of sense amplifier after switching	70	-	130	ns
$t_{off(drv)G(min)}$	minimum off time of one gate driver		-	125	-	ns
Serial peripheral interface timing; pins CSB, SCLK, SDI and SDO						
$t_{cy(clk)}$	clock cycle time		285	-	-	ns
$t_{SPILEAD}$	SPI enable lead time		140	-	-	ns
t_{SPILAG}	SPI enable lag time		140	-	-	ns
$t_{clk(H)}$	clock HIGH time		140	-	-	ns
$t_{clk(L)}$	clock LOW time		140	-	-	ns
$t_{su(D)}$	data input setup time		50	-	-	ns
$t_{h(D)}$	data input hold time		50	-	-	ns
$t_{v(Q)}$	data output valid time	pin SDO; CL = 50 pF	-	-	130	ns
$t_{WH(S)}$	chip select pulse width HIGH		285	-	-	ns
$t_{d(SPI)}$	SPI delay time	after leaving OFF mode; EN = 0 V –> 5 V	-	-	100	µs
$t_{rst(reg)}$	register reset time	time to reset all registers to default value; EN = 0 V –> 5 V	-	-	400	µs
Gate driver characteristics for pins G1, G2 and G3						
$t_{ch(G)}$	gate charge time	20 % to 80 %; V_{bsx} - LXx = 10 V; CG = 1000 pF	-	-	50	ns
$t_{dch(G)}$	gate discharge time	20 % to 80 %; V_{bsx} - LXx = 10 V; CG = 1000 pF	-	-	25	ns
t_p	pulse duration	applies to BS pins				
		recharge pulse time	-	80	-	µs
		period for recharge pulses	-	360	-	µs

Table 43. Dynamic characteristics *...continued*

Min and Max values are specified for the following conditions: V_{VIN} = 10 V to 80 V, V_{EN} = 4.5 V to 5.5 V, V_{VCC} = 4.5 V to 5.5 V and T_j = −40 °C to +175 °C. All voltages are defined with respect to ground, positive currents flow into the IC. Typical values are given at V_{VIN} = 40 V. V_{EN} = 5 V and V_{VCC} = 5 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage measurements						
t_{meas}	measurement time	period for voltage measurements at VIN	-	15	-	µs
		period for voltage measurements at outputs	-	80	-	µs
		period for sampling low headroom detection at outputs	-	8	-	µs
$t_{meas(LED)}$	LED measurement time	period for the LED voltage measurement update when the PWM pin is static	-	16	-	ms
VGG characteristics						
$t_{err(startup)}$	start-up error time	time to detect an error on VGG at start-up	-	20.2	-	ms
$t_{err(oper)}$	operation error time	time to detect an error on VGG during operation	-	200	-	µs
Limp-home mode timing						
$t_{to(limp)}$	limp time-out time	Limp-home mode time-out time				
		setting 1	4.72	5.02	5.3	ms
		setting 2	9.53	10	10.6	ms
		setting 3	19.1	20.2	21.2	ms
		setting 4	38.3	40.4	42.5	ms
		setting 5	76.7	80.9	84.9	ms
		setting 6	153	162	170	ms
		setting 7	307	324	340	ms
		setting 8	614	647	680	ms

[1] Lower hysteresis trip point until external FET is turned on.

[2] Higher hysteresis trip point until external FET is turned off.

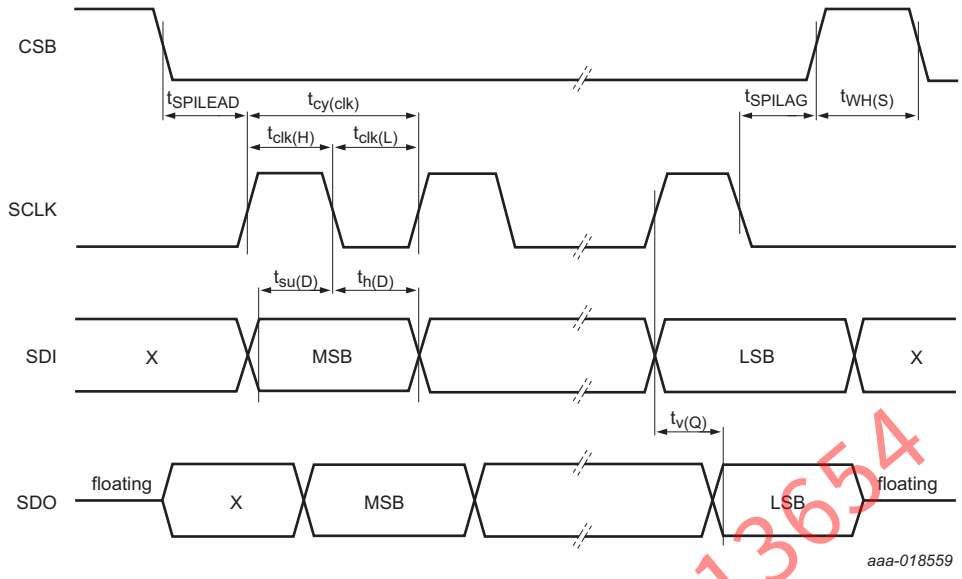


Fig 12. SPI timing diagram

13. Application information

Figure 13 provides an example for the ASL3417SHN in a typical external front lighting application driving 3 independent LED strings.

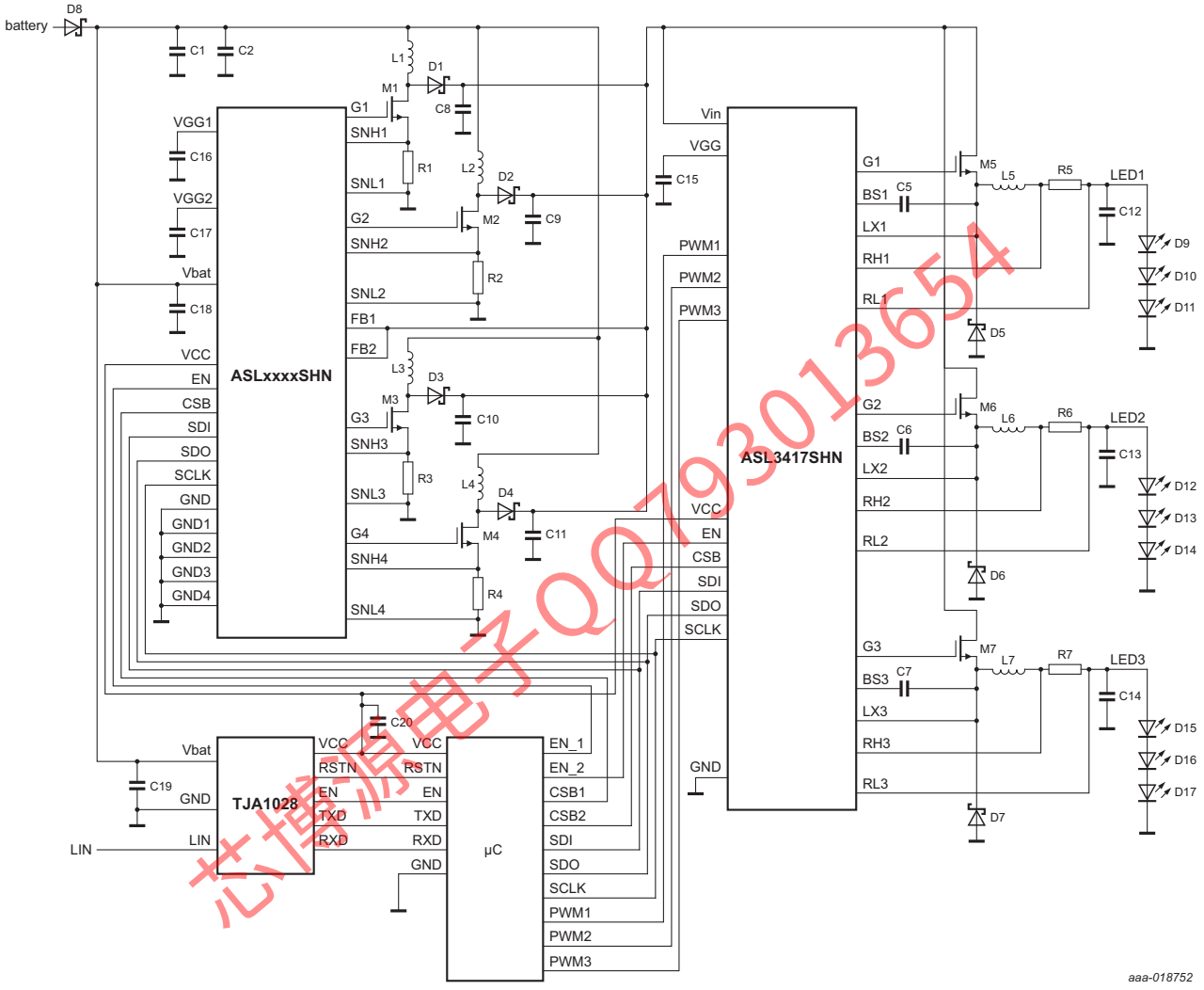


Fig 13. Application example in a typical external front lighting

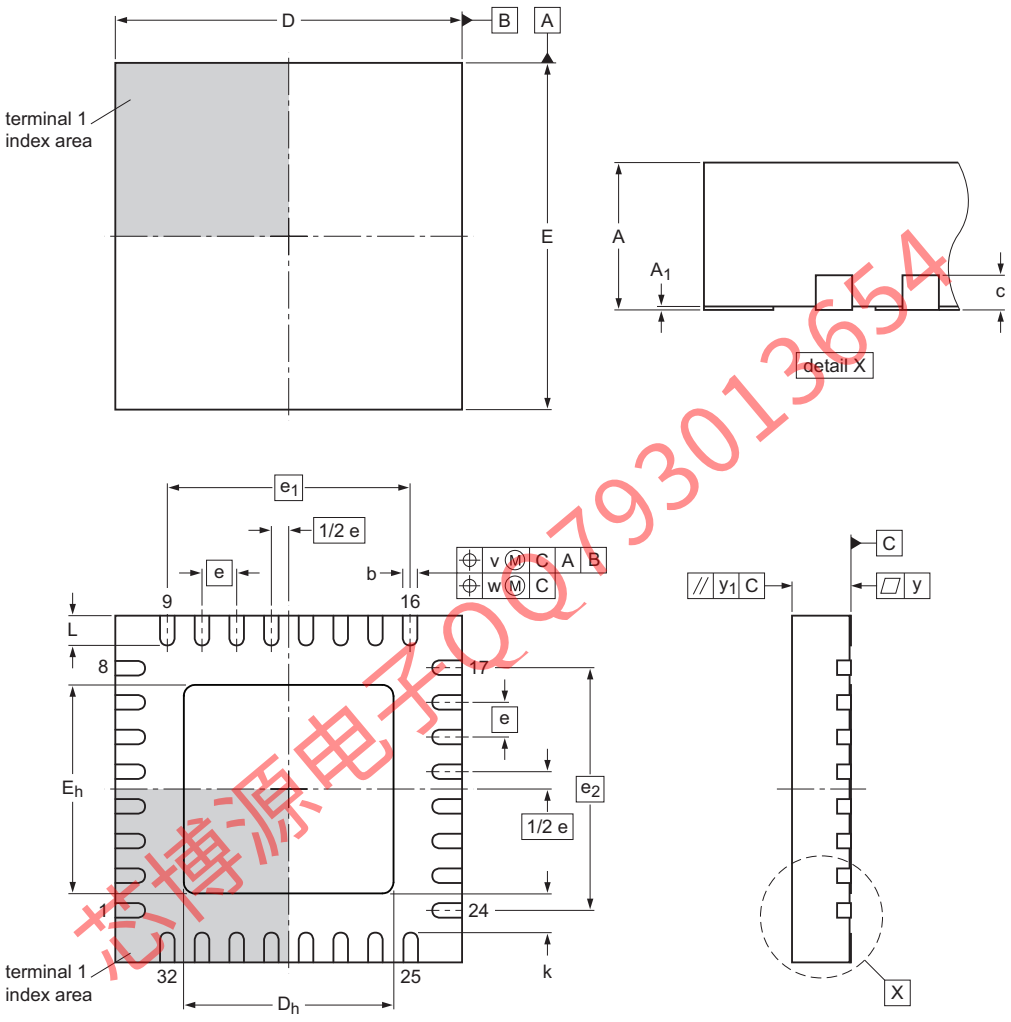
14. Test information

14.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 - Failure mechanism-based stress test qualification for integrated circuits. It is suitable for use in automotive applications.

15. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-12**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	k	L	v	w	y	y_1
	max	1.00	0.05	0.30		5.1	3.1	5.1	3.1					0.50				
mm	nom	0.85	0.02	0.21	0.2	5.0	3.0	5.0	3.0	0.5	3.5	3.5		0.44	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		4.9	2.9	4.9	2.9				0.5	0.30				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot617-12_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT617-12		MO-220				~~13-10-14~~ 13-11-05

Fig 14. Package outline HVQFN32

16. Revision history

Table 44. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ASL3417SHN v.4	20190916	Product data sheet	-	ASL3417SHN v.3
Modifications:	• Section 8.5.1: corrected results in calculation example • Table 19: changed formula for VGG setting • Table 37: adapt reset values for a more robust start of the limp-home functionality • Table 42: clarified minimum LED output current			
ASL3417SHN v.3	20171026	Product data sheet	-	ASL3417SHN v.2
Modifications:	• Section 8.13.6: the SPI register address changed in list item 4 and list item 5 • Section 8.9: clarified exceeding of limiting values			
ASL3417SHN v.2	20170222	Product data sheet	-	ASL3417SHN v.1
Modifications:	• Formula for voltage conversion updated • Figure 11: updated • Equation 4 and Equation 5: updated • Table 42: maximum value for low headroom turn-off voltage changed			
ASL3417SHN v.1	20160603	Product data sheet	-	-

19. Tables

20. Figures

21. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

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