TPS7A7100 1A、快速瞬态响应、低压降稳压器

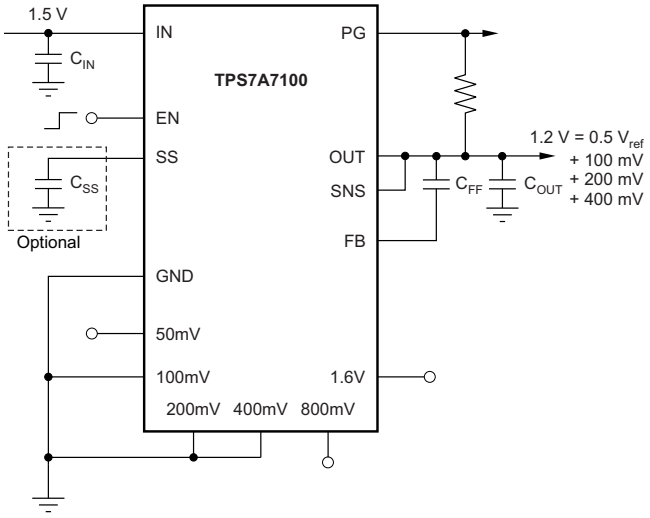
1 特性

- 低压降：1A 时为 140mV
- V_{IN} 范围：1.5V 至 6.5V
- 可配置的固定 V_{OUT} 范围：0.9V 至 3.5V
- 可调节的 V_{OUT} 范围：0.9V 至 5V
- 非常出色的负载和线路瞬态响应
- 与陶瓷输出电容一起工作时保持稳定
- 1.5%
- 可编程软启动
- 电源正常 (PG) 输出
- 3mm × 3mm QFN-16 和 5mm × 5mm QFN-20 封装

2 应用

- 无线基础设施：串行解串器 (SerDes)、现场可编程门阵列 (FPGA)、 数字信号处理器 (DSP)™
- 射频 (RF) 组件：压控振荡器 (VCO)、数模转换器 (ADC)、模数转换器 (DAC)、低压差分信号 (LVDS)
- 机顶盒：放大器、ADC、DAC、 FPGA、DSP
- 无线局域网 (LAN)， *Bluetooth*®
- 个人电脑 (PC) 和打印机
- 音频和视频

典型应用电路



3 说明

TPS7A7100 低压降 (LDO) 稳压器设计用于追求极低压降特性的 应用 （1A 时为 140mV），此类应用的输入电压介于 1.5V 至 6.5V 之间。TPS7A7100 提供一种创新的、用户可配置的输出电压设置，范围介于 0.9V 至 3.5V 之间，从而免除了对外部电阻的需要并消除了任何与之相关的误差。

TPS7A7100具有极快的负载瞬态响应，与陶瓷输出电容器一起工作时保持稳定，并且在线路、负载、和温度上所支持的精度优于 2%。一个软启动引脚使得应用能够减少到负载的涌入电流。此外，一个开漏、电源正常信号可实现电源轨排序。

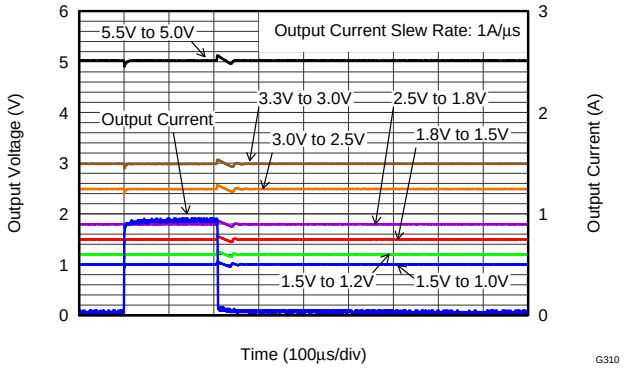
TPS7A7100 提供 3mm × 3mm、16 引脚 VQFN 和 5mm × 5mm、20 引脚 VQFN 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS7A7100	VQFN (16)	3.00mm × 3.00mm
	超薄四方扁平无引线封装 (VQFN) (20)	5.00mm x 5.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

负载瞬态响应（7 种不同输出）：
1.5 V_{IN} 至 1 V_{OUT}，1.5 V_{IN} 至 1.2 V_{OUT}，1.8 V_{IN} 至 1.5 V_{OUT}，2.5 V_{IN} 至 1.8V_{OUT}，3 V_{IN} 至 2.5 V_{OUT}，3.3 V_{IN} 至 3 V_{OUT} 以及 5.5 V_{IN} 至 5 V_{OUT}



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (September 2013) to Revision F **Page**

- 已添加 *ESD 额定值表*，*特性 描述* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- Changed name of section from *Enable and Shutdown the Device* to *Enable* ... 21

Changes from Revision C (May 2012) to Revision D **Page**

- 将 C_{FF}电容器添加到首页方框图中 ... 1
- Added text to FB pin description ... 4
- Added C_{FF} test condition and table note to *Electrical Characteristics* ... 7
- Deleted maximum value for Output Current Limit parameter in *Electrical Characteristics* ... 7
- Added C_{FF} capacitor to Figure 22 ... 13
- Added C_{FF} capacitor to Figure 23 ... 14
- Added C_{FF} capacitor to Figure 24 ... 15
- Added C_{FF} capacitor to Figure 25 ... 16
- Added C_{FF} capacitor to Figure 26 ... 17
- Added C_{FF} capacitor to Figure 27 ... 18
- Added C_{FF} capacitor to Figure 28 ... 20
- Added C_{FF} capacitor to front page block diagram ... 23
- Changed capacitor values in first sentence of *Output Capacitor Requirements* section ... 24

Changes from Revision B (April 2012) to Revision C **Page**

- Added RGT package to Figure 42 ... 28
- Added RGT package to Figure 44 ... 30

Changes from Revision A (March 2012) to Revision B **Page**

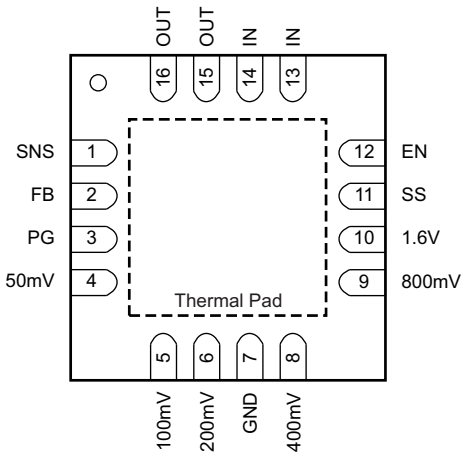
- 已更改*精度*特性要点 1
- 已添加 RGT (QFN-16) 封装至 特性 1
- Added RGT package pinout drawing 4
- Added RGT package to Pin Descriptions table 4
- Added RGT (QFN-16) package to *Thermal Information* table 6
- Added test conditions for RGT package to *Output Voltage Accuracy* parameter 7

Changes from Original (March 2012) to Revision A **Page**

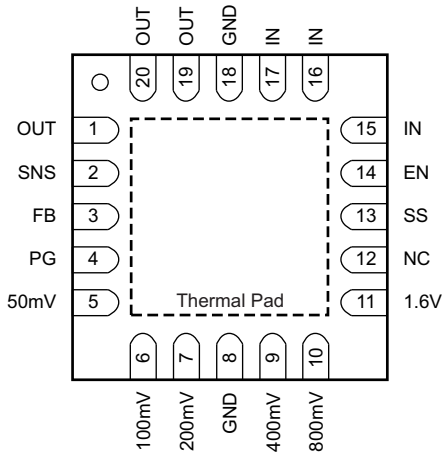
- 已从“产品预览”改为“量产数据” 1

5 Pin Configurations

RGT Package
16-Pin VQFN
Top View



RGW Package
20-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	RGW	RGT		
50mV, 100mV, 200mV, 400mV, 800mV, 1.6V	5, 6, 7, 9, 10, 11	4, 5, 6, 8, 9, 10	I	Output voltage setting pins. These pins must be connected to ground or left floating. Connecting these pins to ground increases the output voltage by the value of the pin name; multiple pins can be simultaneously connected to GND to select the desired output voltage. Leave these pins floating (open) when not in use. See the *User-Configurable Output Voltage* section for more details.
EN	14	12	I	Enable pin. Driving this pin to logic high enables the device; driving the pin to logic low disables the device. See the *Enable* section for more details.
FB	3	2	I	Output voltage feedback pin. Connected to the error amplifier. See the *User-Configurable Output Voltage* and *Traditional Adjustable Configuration* sections for more details. TI highly recommends connecting a 220-pF ceramic capacitor from FB pin to OUT.
GND	8, 18	7	—	Ground pin.
IN	15, 16, 17	13, 14	I	Unregulated supply voltage pin. TI recommends connecting an input capacitor to this pin. See *Input Capacitor Requirements* for more details.
NC	12	—	—	Not internally connected. The NC pin is not connected to any electrical node. TI strongly recommends connecting this pin and the thermal pad to a large-area ground plane. See the *Power Dissipation* section for more details.
OUT	1, 19, 20	15, 16	O	Regulated output pin. A 4.7-µF or larger capacitance is required for stability. See *Output Capacitor Requirements* for more details.
PG	4	3	O	Active-high power good pin. An open-drain output that indicates when the output voltage reaches 90% of the target. See *Power Good* for more details.
SNS	2	1	I	Output voltage sense input pin. See the *User-Configurable Output Voltage* and *Traditional Adjustable Configuration* sections for more details.
SS	13	11	—	Soft-start pin. Leaving this pin open provides soft start of the default setting. Connecting an external capacitor between this pin and the ground enables the soft-start function by forming an RC-delay circuit in combination with the integrated resistance on the silicon. See the *Soft-Start* section for more details.
Thermal Pad			—	TI strongly recommends connecting the thermal pad to a large-area ground plane. If available, connect an electrically-floating, dedicated thermal plane to the thermal pad as well.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
Voltage	IN, PG, EN	–0.3	7	V
	SS, FB, SNS, OUT	–0.3	V_{IN} + 0.3(2)	V
	50 mV, 100 mV, 200 mV, 400 mV, 800 mV, 1.6 V	–0.3	V_{OUT} + 0.3(2)	V
Current	OUT	Internally limited		A
	PG (sink current into IC)		5	mA
Temperature	Operating virtual junction, T_J	–55	160	°C
	Storage, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or +7 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage	1.425		6.5	V
V_{OUT}	Output voltage	0.9		5	V
V_{EN}	Enable voltage	0		6.5	V
V_{PG}	Pullup voltage	0		6.5	V
50 mV, 100 mV, 200 mV, 400 mV, 800 mV, 1.6 V	Any-out voltage	0		V_{OUT}	
I_{OUT}	Output current	0		1	A
C_{OUT}	Output capacitance	4.7		200(1)	µF
C_{FF}	Feedforward capacitance	0		100	nF
T_J	Junction temperature	–40		125	°C

(1) For output capacitors larger than 47 µF a feedforward capacitor of at least 220 pF must be used.

6.4 Thermal Information

THERMAL METRIC[1][2]		TPS7A7100[3]		UNIT
		RGW (VQFN)	RGT (VQFN)	
		20 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[4]	35.7	44.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance[5]	33.6	54.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance[6]	15.2	17.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter[7]	0.4	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter[8]	15.4	17.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance[9]	3.8	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on printed-circuit-board (PCB) copper area, see the TI PCB Thermal Calculator.
(3) Thermal data for the RGW package is derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
(a) i. RGW: The exposed pad is connected to the PCB ground layer through a 4 × 4 thermal via array.
ii. RGT: The exposed pad is connected to the PCB ground layer through a 2 × 2 thermal via array.
(b) i. RGW: Both the top and bottom copper layers have a dedicated pattern for 4% copper coverage.
ii .RGT: Both the top and bottom copper layers have a dedicated pattern for 5% copper coverage.
(c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3-inch × 3-inch copper area. To understand the effects of the copper area on thermal performance, see the *Power Dissipation* and *Estimating Junction Temperature* sections.
(4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(5) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(6) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(7) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(8) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(9) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Electrical Characteristics

Over operating temperature range (T_J = –40°C to +125°C), 1.425 V ≤ V_{IN} ≤ 6.5 V, V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V or V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.5 V(1)(2), OUT connected to 50 Ω to GND(3), V_{EN} = 1.1 V, C_{OUT} = 10 µF, C_{SS} = 10 nF, C_{FF} = 0 pF (RGW package), C_{FF} = 220 pF (RGT package)(4), and PG pin pulled up to V_{IN} with 100 kΩ, 27 kΩ ≤ R2 ≤ 33 kΩ for adjustable configuration(5), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		1.425		6.5	V
$V_{(SS)}$	SS pin voltage			0.5		V
V_{OUT}	Output voltage	Adjustable with external feedback resistors	0.9		5	V
		Fixed with voltage setting pins	0.9		3.5	
	Output voltage accuracy(6)(7)	RGT package only, adjustable, –40°C ≤ T_A ≤ 85°C, 25 mA ≤ I_{OUT} ≤ 1 A	–1.5%		1.5%	
		RGT package only, fixed, –40°C ≤ T_A ≤ 85°C, 25 mA ≤ I_{OUT} ≤ 1 A	–2%		2%	
		Adjustable, 25 mA ≤ I_{OUT} ≤ 1 A	–2%		2%	
		Fixed, 25 mA ≤ I_{OUT} ≤ 1 A	–3%		3%	
$\Delta V_{O(\Delta VI)}$	Line regulation	I_{OUT} = 25 mA		0.01		%/V
$\Delta V_{O(\Delta IO)}$	Load regulation	25 mA ≤ I_{OUT} ≤ 1 A		0.1		%/A
$V_{(DO)}$	Dropout voltage (8)	V_{OUT} ≤ 3.3 V, I_{OUT} = 1 A, $V_{(FB)}$ = GND			140	mV
		3.3 V < V_{OUT}, I_{OUT} = 1 A, $V_{(FB)}$ = GND			350	mV
$I_{(LIM)}$	Output current limit	V_{OUT} forced at 0.9 × $V_{OUT(TARGET)}$, V_{IN} = 3.3 V, $V_{OUT(TARGET)}$ = 0.9 V	1.1	1.6		A
$I_{(GND)}$	GND pin current	Full load, I_{OUT} = 1 A		1.8		mA
		Minimum load, V_{IN} = 6.5 V, $V_{OUT(TARGET)}$ = 0.9 V, I_{OUT} = 25 mA			4	mA
		Shutdown, PG = (open), V_{IN} = 6.5 V, $V_{OUT(TARGET)}$ = 0.9 V, $V_{(EN)}$ < 0.5 V		0.1	5	µA
$I_{(EN)}$	EN pin current	V_{IN} = 6.5 V, $V_{(EN)}$ = 0 V and 6.5 V			±0.1	µA
$V_{IL(EN)}$	EN pin low-level input voltage (disable device)		0		0.5	V
$V_{IH(EN)}$	EN pin high-level input voltage (enable device)		1.1		6.5	V
$V_{IT(PG)}$	PG pin threshold	For the direction PG↓ with decreasing V_{OUT}	0.85V_{OUT}	0.9V_{OUT}	0.96V_{OUT}	V
$V_{hys(PG)}$	PG pin hysteresis	For PG↑		0.02V_{OUT}		V
$V_{OL(PG)}$	PG pin low-level output voltage	V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1 mA (current into device)			0.4	V
$I_{lkg(PG)}$	PG pin leakage current	V_{OUT} > $V_{IT(PG)}$, $V_{(PG)}$ = 6.5 V			1	µA
$I_{(SS)}$	SS pin charging current	$V_{(SS)}$ = GND, V_{IN} = 3.3 V	3.5	5.1	7.2	µA
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 1.5 V, V_{OUT} = 1.2 V, I_{OUT} = 1 A		39.57		μV_{RMS}
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		°C
T_J	Operating junction temperature		–40		125	°C

(1) When V_{OUT} ≤ 3.5 V, V_{IN} ≥ (V_{OUT} + 0.3 V) or 1.425 V, whichever is greater; when V_{OUT} > 3.5 V, V_{IN} ≥ (V_{OUT} + 0.5 V).
(2) $V_{OUT(TARGET)}$ is the calculated target V_{OUT} value from the output voltage setting pins: 50 mV, 100 mV, 200 mV, 400 mV, 800 mV, and 1.6 V in fixed configuration, or the expected V_{OUT} value set by external feedback resistors in adjustable configuration.
(3) This 50-Ω load is disconnected when the test conditions specify an I_{OUT} value.
(4) C_{FF} is the capacitor between FB pin and OUT.
(5) R2 is the bottom-side of the feedback resistor between the FB pin and GND. See for details.
(6) When the TPS7A7100 is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.
(7) The TPS7A7100 is not tested at V_{OUT} = 0.9 V, 2.7 V ≤ V_{IN} ≤ 6.5 V, and 500 mA ≤ I_{OUT} ≤ 1 A because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package.
(8) $V_{(DO)}$ is not defined for output voltage settings less than 1.2 V.

6.6 Typical Characteristics

At T_J = 25°C, V_{IN} = $V_{OUT(TARGET)}$ + 0.3 V, I_{OUT} = 25 mA, $V_{(EN)}$ = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{(SS)}$ = 10 nF, and the PG pin pulled up to V_{IN} with 100-kΩ pullup resistor, unless otherwise noted.

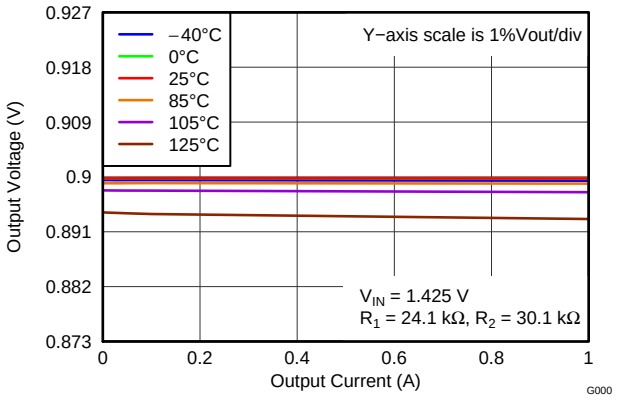


Figure 1. Load Regulation (0.9 V, Adjustable)

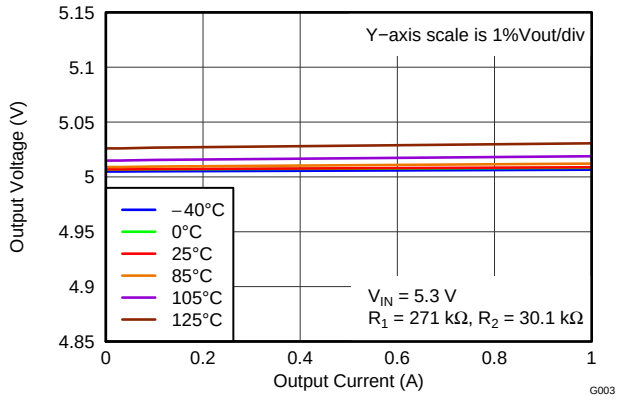


Figure 2. Load Regulation (5 V, Adjustable)

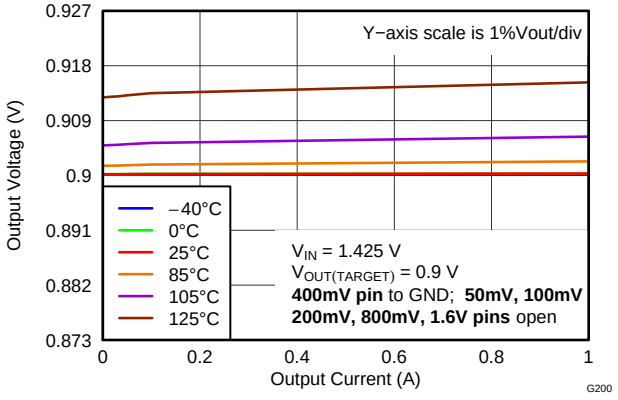


Figure 3. Load Regulation (0.9 V, Fixed By Setting Pins)

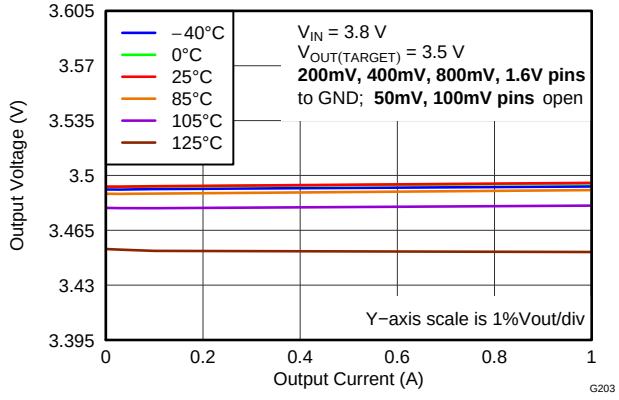


Figure 4. Load Regulation (3.5 V, Fixed By Setting Pins)

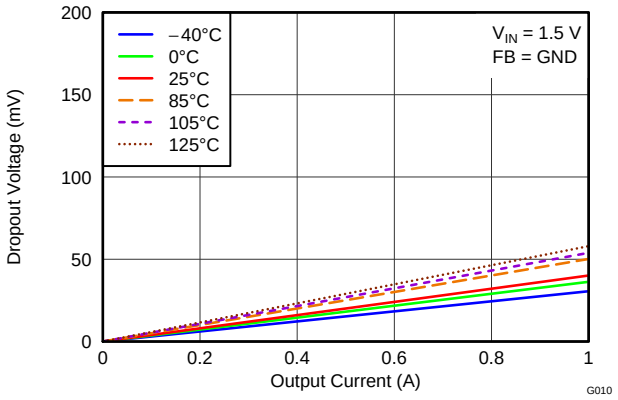


Figure 5. Dropout Voltage vs Output Current

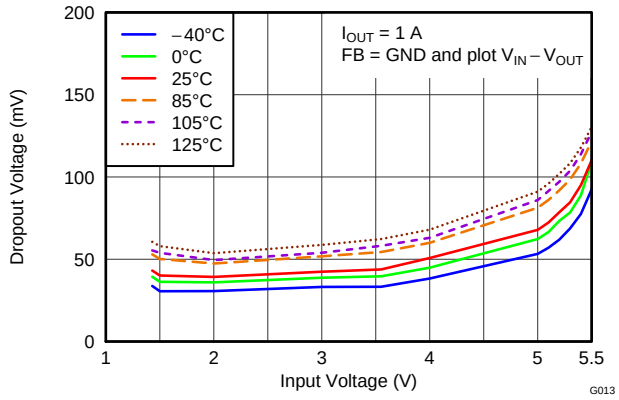


Figure 6. Dropout Voltage vs Temperature

Typical Characteristics (continued)

At T_J = 25°C, V_{IN} = $V_{OUT(TARGET)}$ + 0.3 V, I_{OUT} = 25 mA, $V_{(EN)}$ = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{(SS)}$ = 10 nF, and the PG pin pulled up to V_{IN} with 100-kΩ pullup resistor, unless otherwise noted.

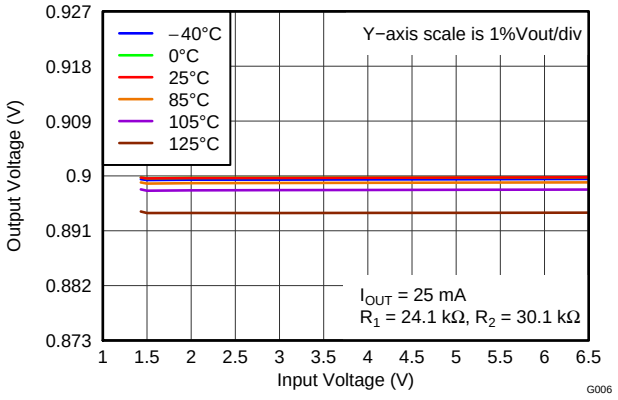


Figure 7. Line Regulation (0.9 V, Adjustable)

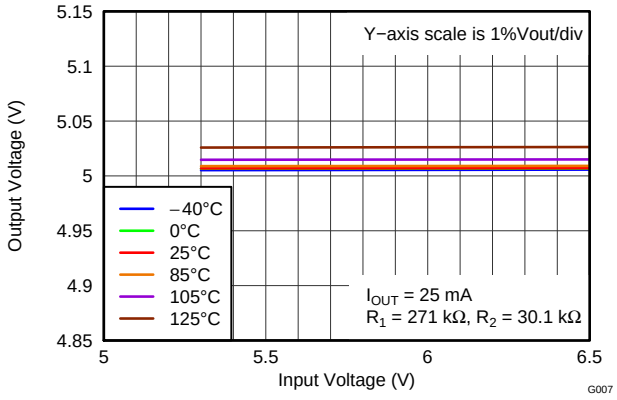


Figure 8. Line Regulation (5 V, Adjustable)

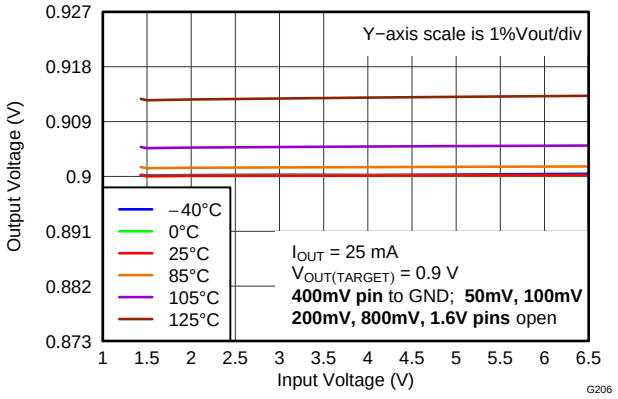


Figure 9. Line Regulation (0.9 V, Fixed By Setting Pins)

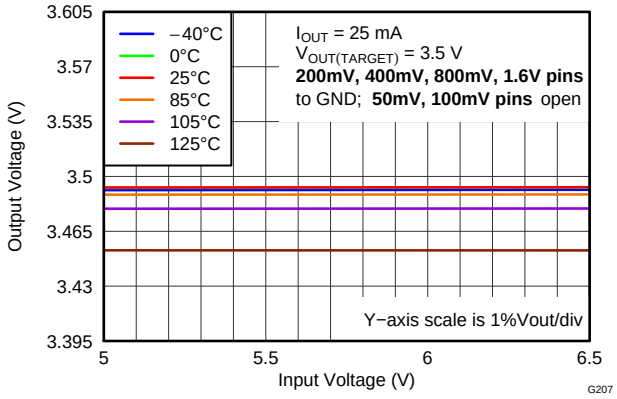


Figure 10. Line Regulation (3.5 V, Fixed By Setting Pins)

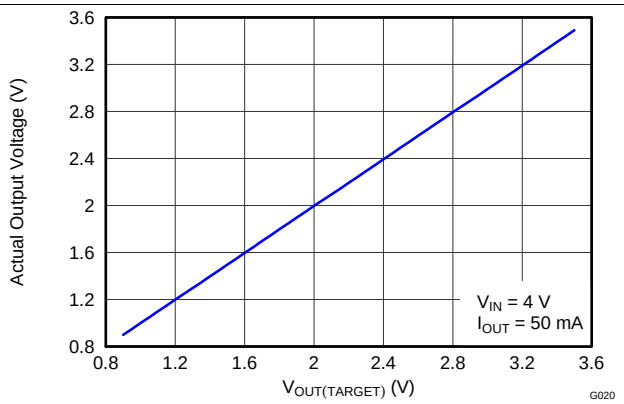


Figure 11. Measured Output Voltage vs Pin-Setting

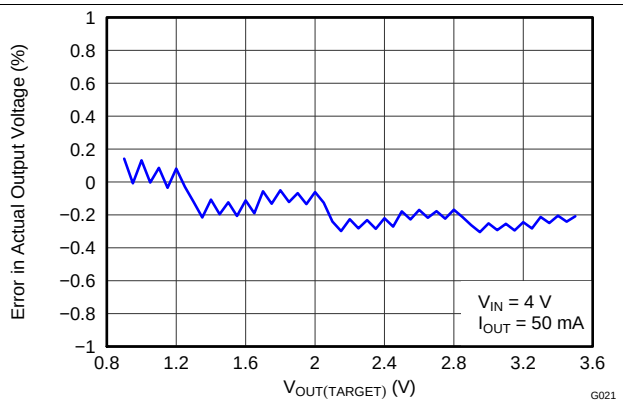


Figure 12. Accuracy vs Pin-Setting

Typical Characteristics (continued)

At T_J = 25°C, V_{IN} = $V_{OUT(TARGET)}$ + 0.3 V, I_{OUT} = 25 mA, $V_{(EN)}$ = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{(SS)}$ = 10 nF, and the PG pin pulled up to V_{IN} with 100-kΩ pullup resistor, unless otherwise noted.

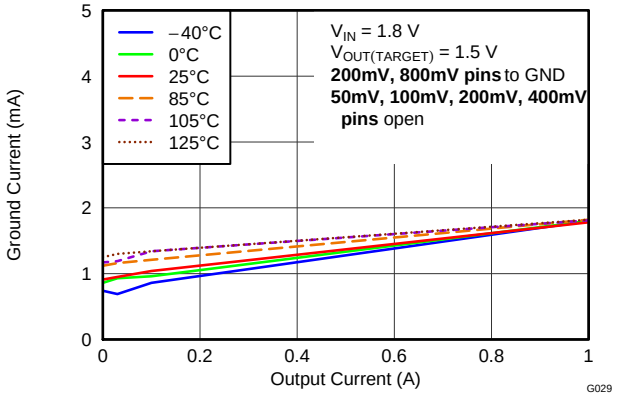


Figure 13. GND Pin Current vs Output Current

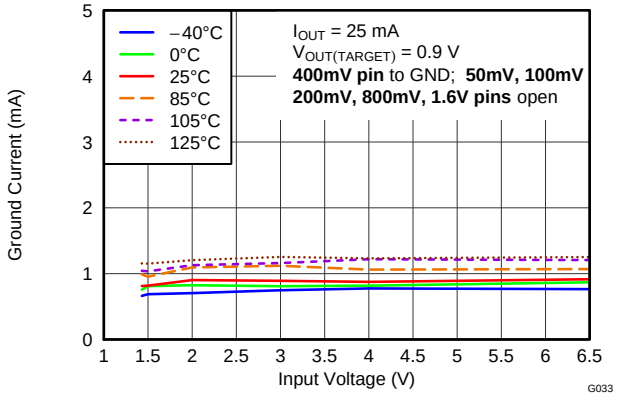


Figure 14. GND Pin Current vs Input Voltage

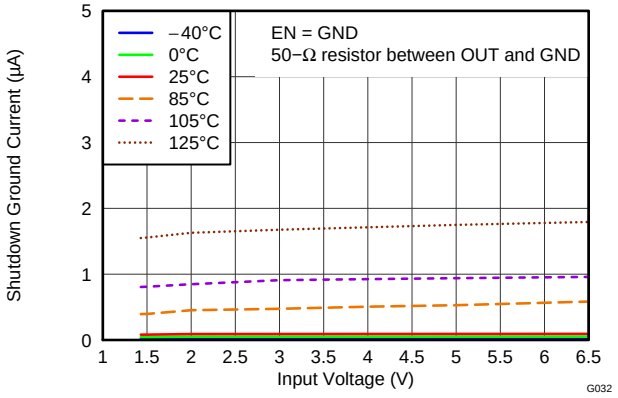


Figure 15. GND Pin Current In Shutdown vs Temperature

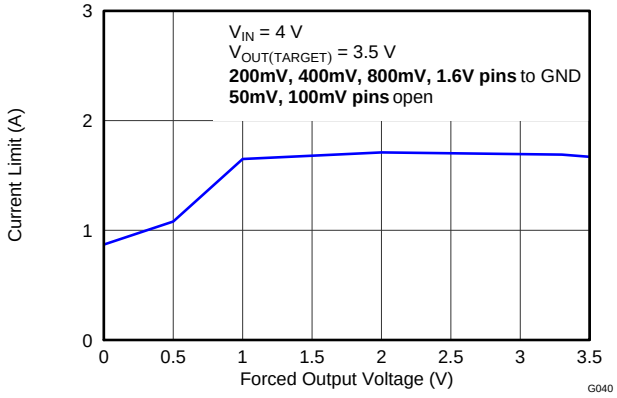


Figure 16. Current Limit vs Output Voltage (Foldback)

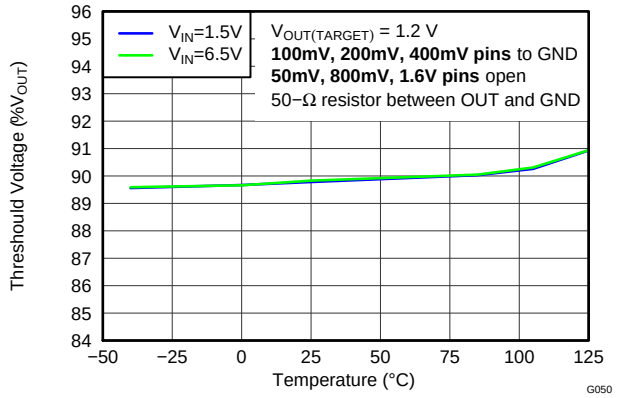


Figure 17. Power-Good Threshold Voltage vs Temperature

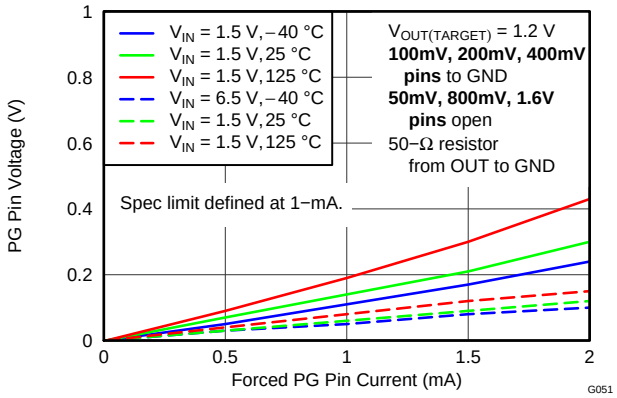


Figure 18. Power-Good Pin Drive Capability

Typical Characteristics (continued)

At T_J = 25°C, V_{IN} = $V_{OUT(TARGET)}$ + 0.3 V, I_{OUT} = 25 mA, $V_{(EN)}$ = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{(SS)}$ = 10 nF, and the PG pin pulled up to V_{IN} with 100-kΩ pullup resistor, unless otherwise noted.

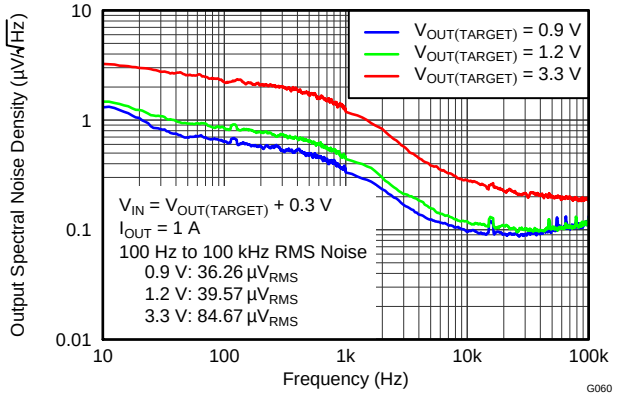


Figure 19. Noise Spectral Density By Output Voltage

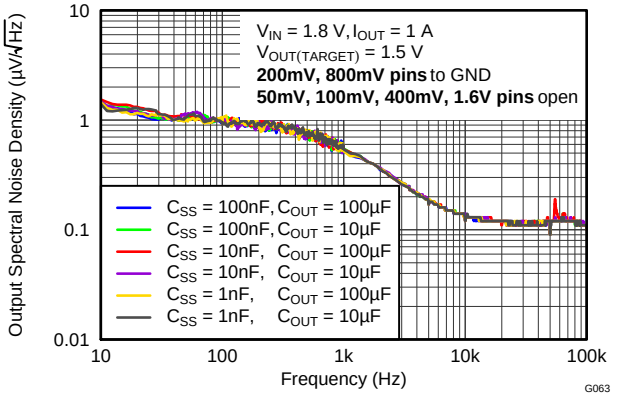


Figure 20. Noise Spectral Density By External Capacitors

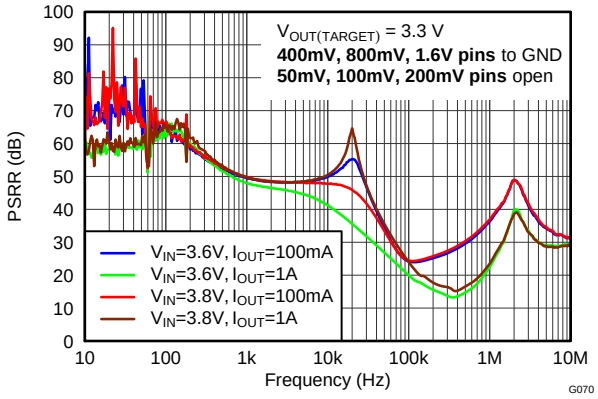


Figure 21. Power-Supply Ripple Rejection vs Frequency

7 Detailed Description

7.1 Overview

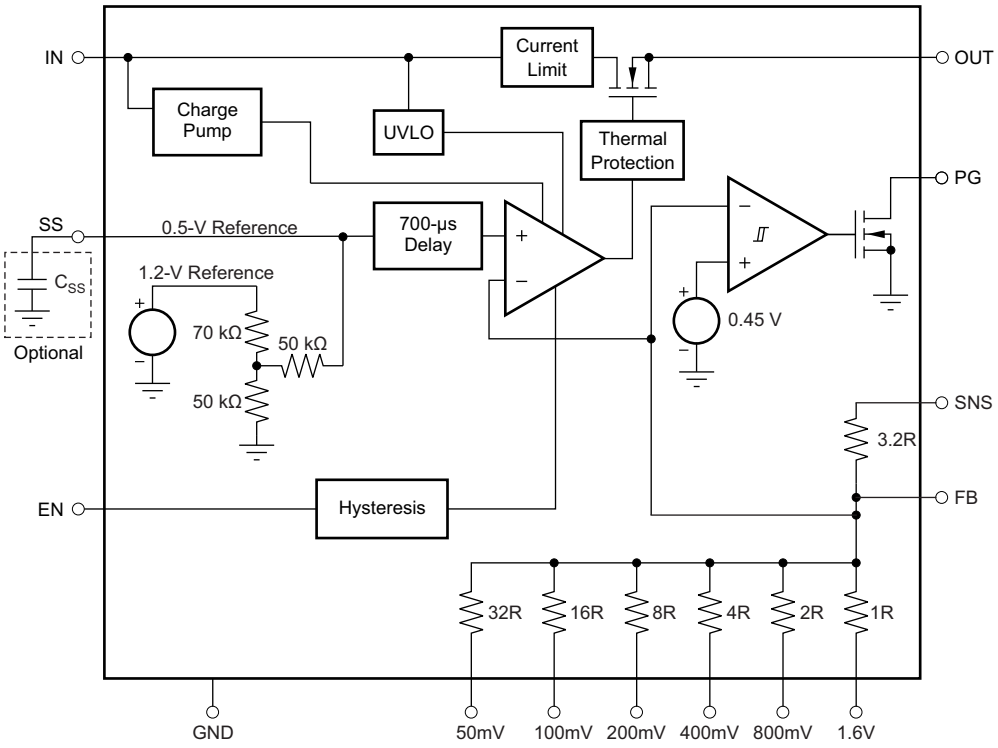
The TPS7A7100 belongs to a family of new-generation LDO regulators that uses innovative circuitry to offer very low dropout voltage along with the flexibility of a programmable output voltage.

The dropout voltage for this LDO regulator family is 0.14 V at 1 A. This voltage is ideal for making the TPS7A7100 into a point-of-load (POL) regulator because 0.14 V at 1 A is lower than any voltage gap among the most common voltage rails: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3 V, and 3.3 V. This device offers a fully user-configurable output voltage setting method. The TPS7A7100 output voltage can be programmed to any target value from 0.9 V to 3.5 V in 50-mV steps.

Another big advantage of using the TPS7A7100 is the wide range of available operating input voltages: from 1.5 V to 6.5 V. The TPS7A7100 also has very good line and load transient response. All these features allow the TPS7A7100 to meet most voltage-regulator needs for under 6-V applications, using only one device so less time is spent on inventory control.

Texas Instruments also offers different output current ratings with other family devices: the TPS7A7200 (2 A) and TPS7A7300 (3 A).

7.2 Functional Block Diagram



NOTE: 32R = 1.024 MΩ (that is, 1R = 32 kΩ).

7.3 Feature Description

7.3.1 User-Configurable Output Voltage

Unlike traditional LDO devices, the TPS7A7100 comes with only one orderable part number. There is no adjustable or fixed output voltage option. The output voltage of the TPS7A7100 is selectable in accordance with the names given to the output voltage setting pins: 50 mV, 100 mV, 200 mV, 400 mV, 800 mV, and 1.6 V. For each pin connected to the ground, the output voltage setting increases by the value associated with that pin name, starting from the value of the reference voltage of 0.5 V. Floating the pins has no effect on the output voltage. Figure 22 through Figure 27 show examples of how to program the output voltages.

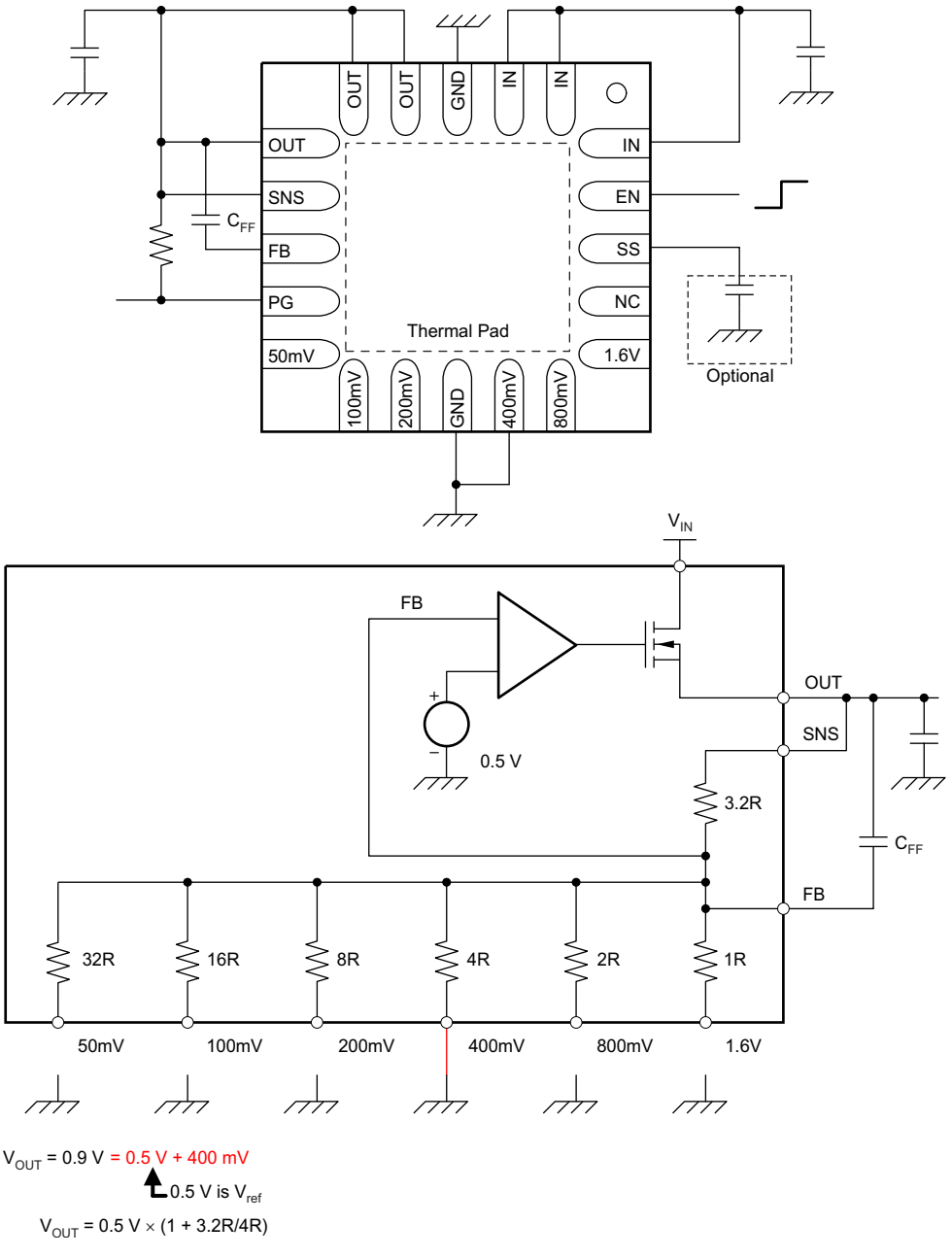
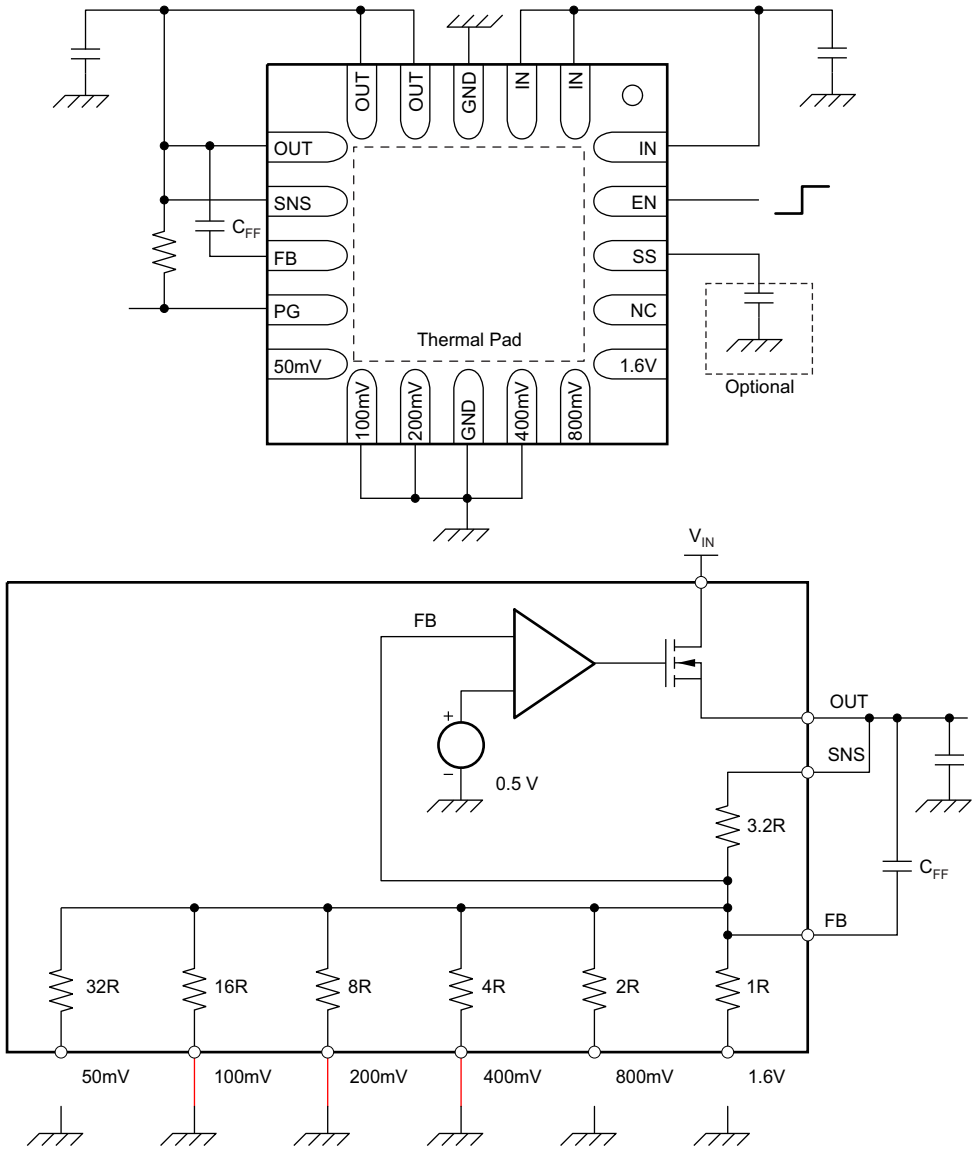


Figure 22. 0.9-V Configuration

Feature Description (continued)



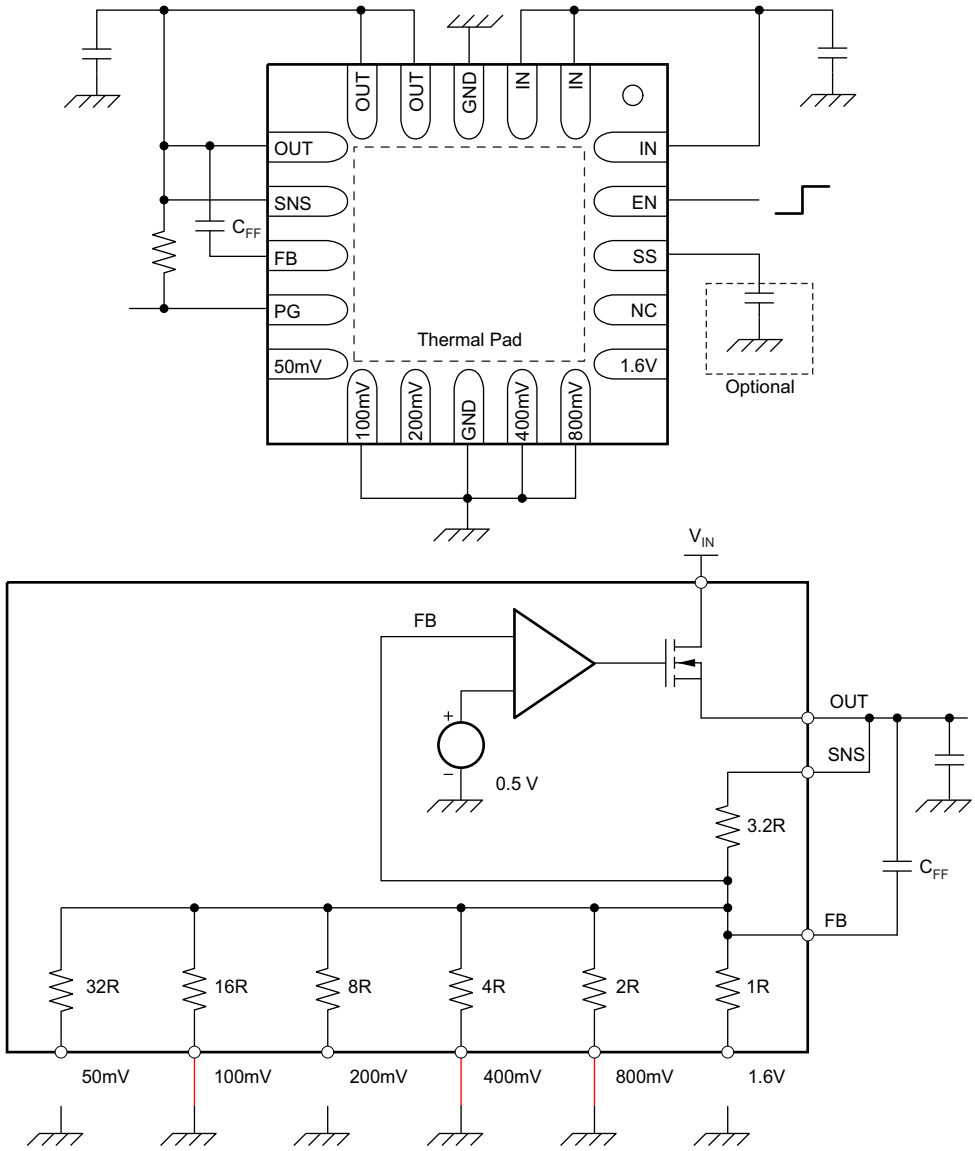
V_{OUT} = 1.2 V = 0.5 V + 100 mV + 200 mV + 400 mV

0.5 V is V_{ref}

$V_{OUT} = 0.5\ V \times (1 + 3.2R/2.29R)$ 2.29R is parallel resistance of 16R, 8R, and 4R.

Figure 23. 1.2-V Configuration

Feature Description (continued)



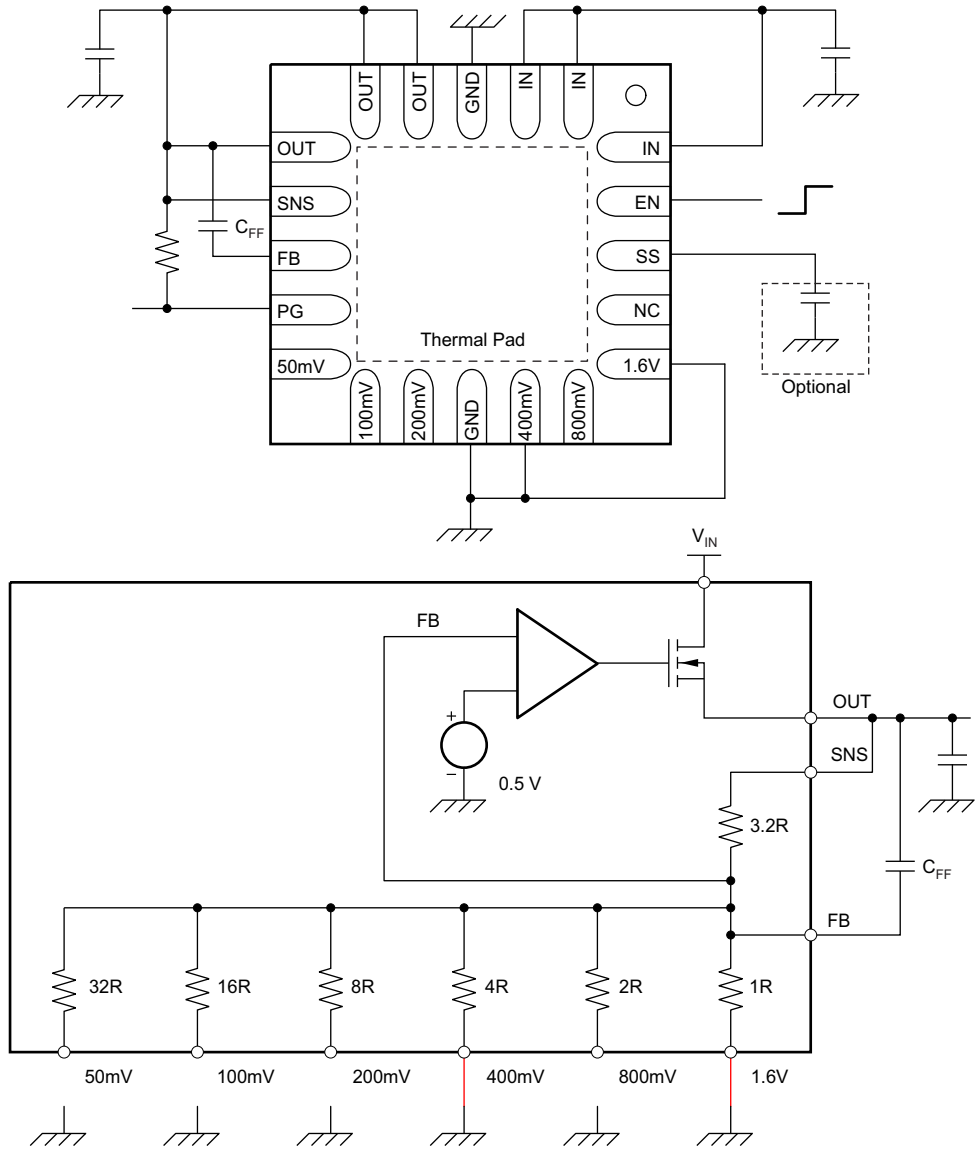
V_{OUT} = 1.8 V = 0.5 V + 100 mV + 400 mV + 800 mV

0.5 V is V_{ref}

$V_{OUT} = 0.5\ V \times (1 + 3.2R/1.23R)$ 1.23R is parallel resistance of 16R, 4R, and 2R.

Figure 24. 1.8-V Configuration

Feature Description (continued)



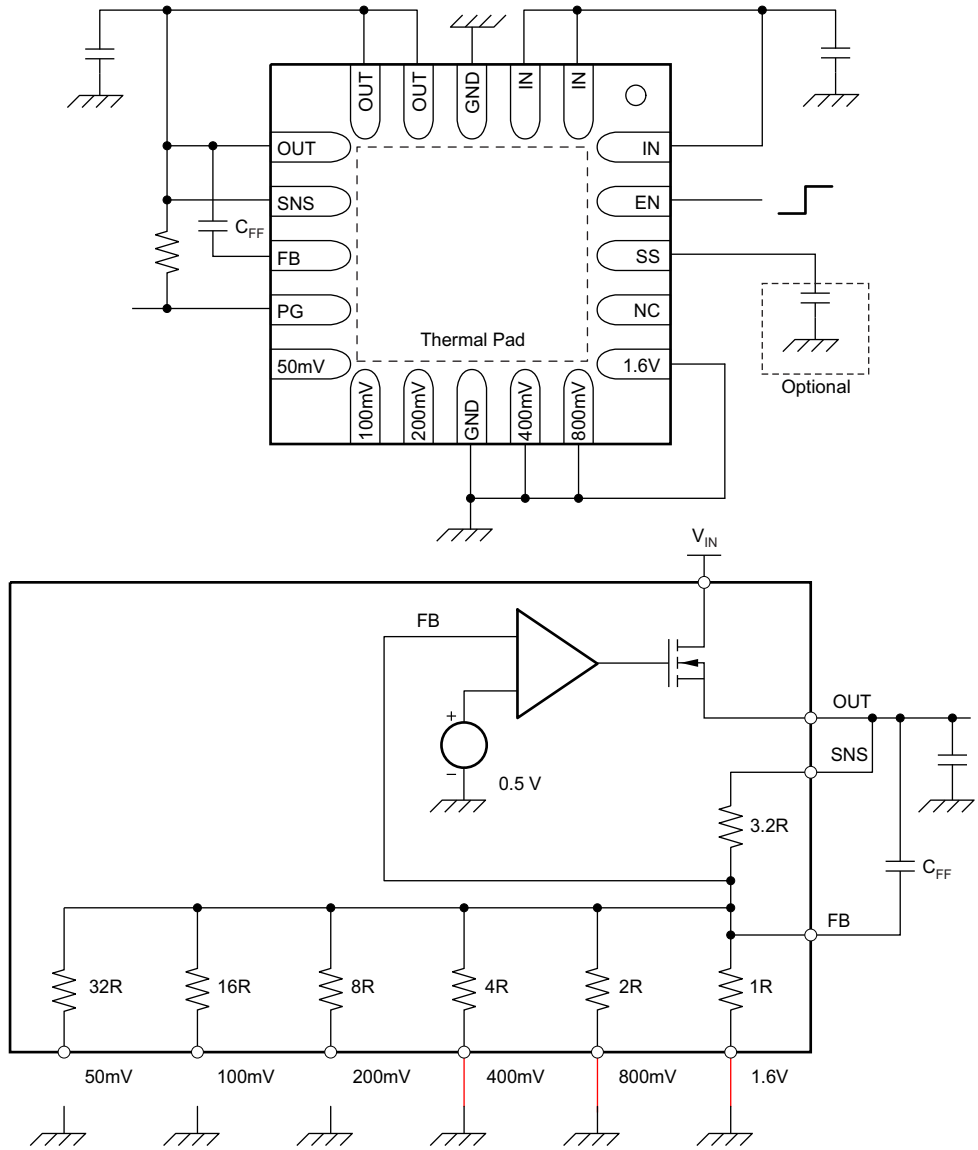
V_{OUT} = 2.5 V = 0.5 V + 400 mV + 1.6 V

0.5 V is V_{ref}

$V_{OUT} = 0.5\ V \times (1 + 3.2R/0.8R)$ 0.8R is parallel resistance of 4R and 1R.

Figure 25. 2.5-V Configuration

Feature Description (continued)



V_{OUT} = 3.3 V = 0.5 V + 400 mV + 800 mV + 1.6 V

0.5 V is V_{ref}

$V_{OUT} = 0.5\ V \times (1 + 3.2R/0.571R)$ 0.571R is parallel resistance of 4R, 2R, and 1R.

Figure 26. 3.3-V Configuration

Feature Description (continued)

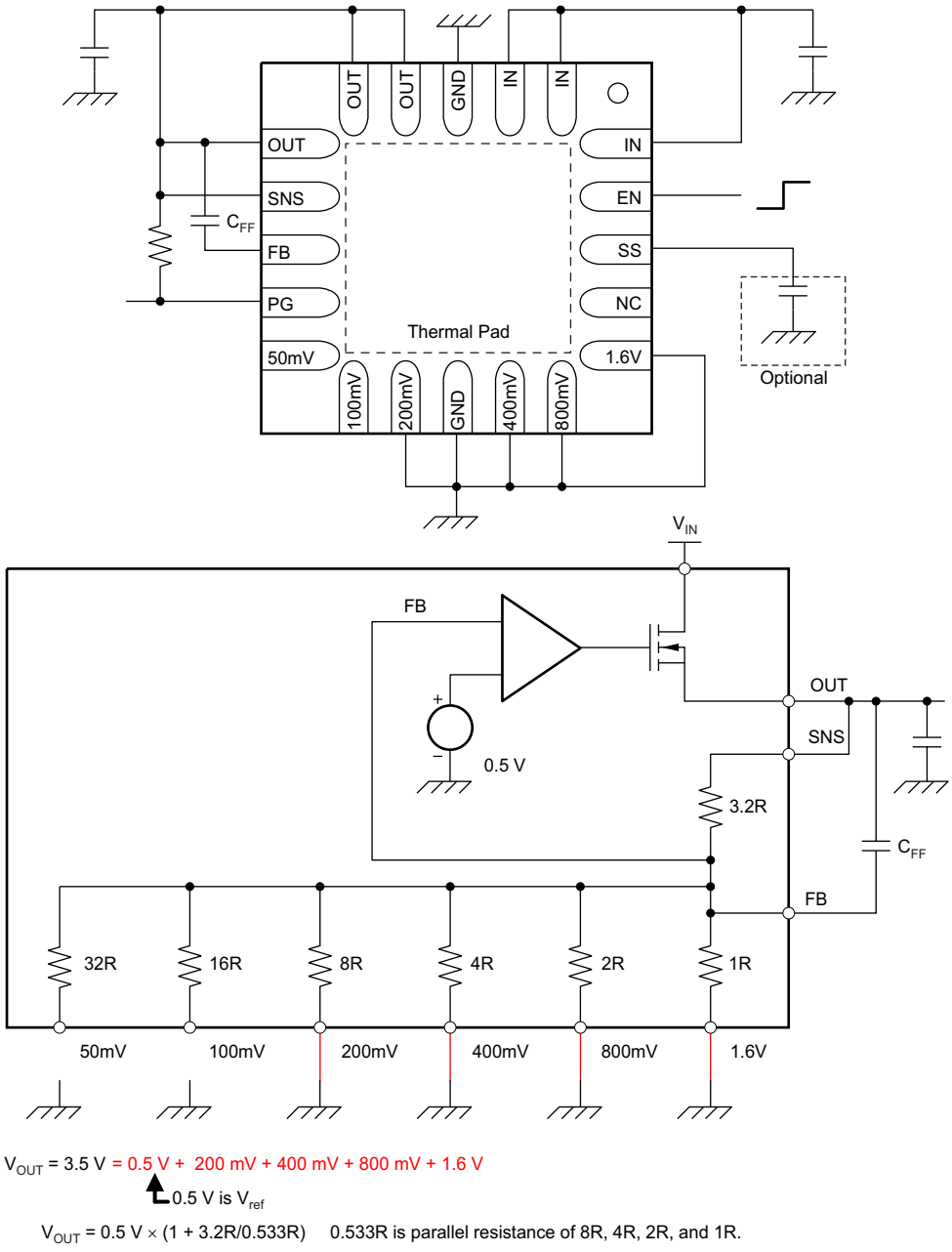


Figure 27. 3.5-V Configuration

See Table 1 for a full list of target output voltages and corresponding pin settings. The voltage setting pins have a binary weight; therefore, the output voltage can be programmed to any value from 0.9 V to 3.5 V in 50-mV steps.

Figure 11 and Figure 12 show this output voltage programming performance.

Feature Description (continued)

NOTE

Any output voltage setting that is not listed in Table 1 is not covered in . For output voltages greater than 3.5 V, use a traditional adjustable configuration (see the *Traditional Adjustable Configuration* section).

Table 1. User Configurable Output Voltage Setting

$V_{OUT(TARGET)}$ (V)	50 mV	100 mV	200 mV	400 mV	800 mV	1.6 V	$V_{OUT(TARGET)}$ (V)	50 mV	100 mV	200 mV	400 mV	800 mV	1.6 V
0.9	open	open	open	GND	open	open	2.25	GND	GND	open	open	open	GND
0.95	GND	open	open	GND	open	open	2.3	open	open	GND	open	open	GND
1	open	GND	open	GND	open	open	2.35	GND	open	GND	open	open	GND
1.05	GND	GND	open	GND	open	open	2.4	open	GND	GND	open	open	GND
1.1	open	open	GND	GND	open	open	2.45	GND	GND	GND	open	open	GND
1.15	GND	open	GND	GND	open	open	2.5	open	open	open	GND	open	GND
1.2	open	GND	GND	GND	open	open	2.55	GND	open	open	GND	open	GND
1.25	GND	GND	GND	GND	open	open	2.6	open	GND	open	GND	open	GND
1.3	open	open	open	open	GND	open	2.65	GND	GND	open	GND	open	GND
1.35	GND	open	open	open	GND	open	2.7	open	open	GND	GND	open	GND
1.4	open	GND	open	open	GND	open	2.75	GND	open	GND	GND	open	GND
1.45	GND	GND	open	open	GND	open	2.8	open	GND	GND	GND	open	GND
1.5	open	open	GND	open	GND	open	2.85	GND	GND	GND	GND	open	GND
1.55	GND	open	GND	open	GND	open	2.9	open	open	open	open	GND	GND
1.6	open	GND	GND	open	GND	open	2.95	GND	open	open	open	GND	GND
1.65	GND	GND	GND	open	GND	open	3	open	GND	open	open	GND	GND
1.7	open	open	open	GND	GND	open	3.05	GND	GND	open	open	GND	GND
1.75	GND	open	open	GND	GND	open	3.1	open	open	GND	open	GND	GND
1.8	open	GND	open	GND	GND	open	3.15	GND	open	GND	open	GND	GND
1.85	GND	GND	open	GND	GND	open	3.2	open	GND	GND	open	GND	GND
1.9	open	open	GND	GND	GND	open	3.25	GND	GND	GND	open	GND	GND
1.95	GND	open	GND	GND	GND	open	3.3	open	open	open	GND	GND	GND
2	open	GND	GND	GND	GND	open	3.35	GND	open	open	GND	GND	GND
2.05	GND	GND	GND	GND	GND	open	3.4	open	GND	open	GND	GND	GND
2.1	open	open	open	open	open	GND	3.45	GND	GND	open	GND	GND	GND
2.15	GND	open	open	open	open	GND	3.5	open	open	GND	GND	GND	GND
2.2	open	GND	open	open	open	GND							

7.3.2 Traditional Adjustable Configuration

For any output voltage target that is not supported in the *User-Configurable Output Voltage* section, a traditional adjustable configuration with external-feedback resistors can be used with the TPS7A7100. shows how to configure the TPS7A7100 as an adjustable regulator with an equation and Table 2 lists recommended pairs of feedback resistor values.

NOTE

The bottom side of feedback resistor R2 in must be in the range of 27 kΩ to 33 kΩ to maintain the specified regulation accuracy.

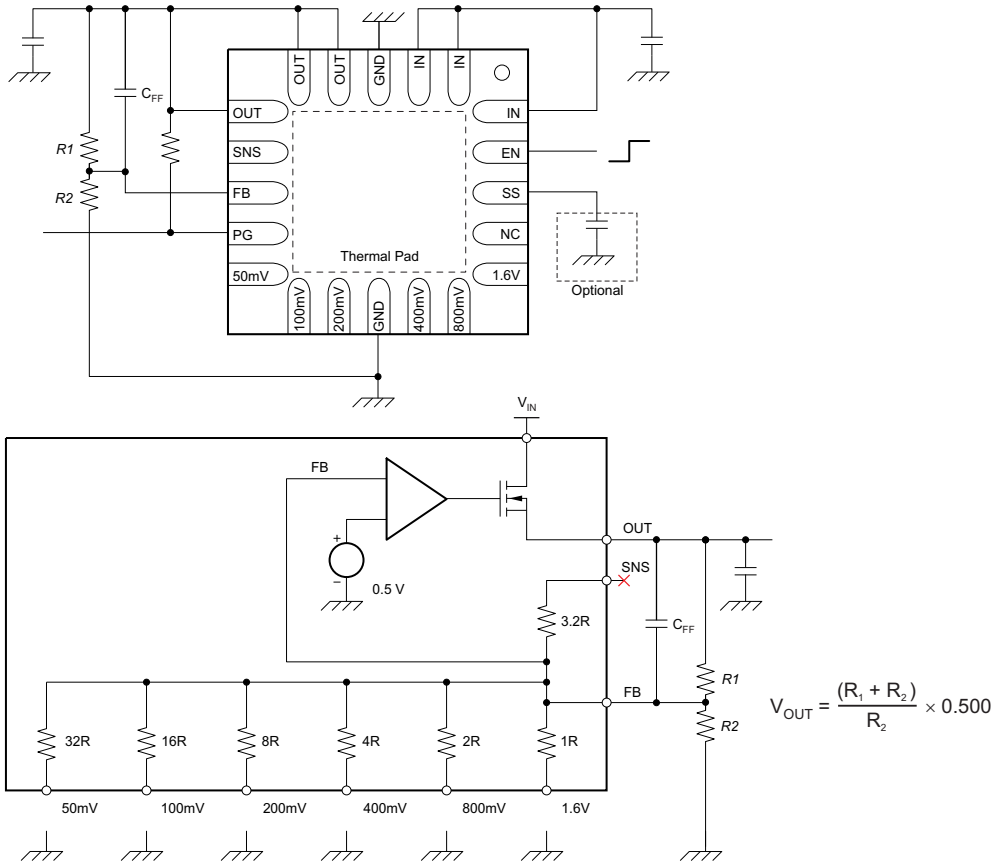


Figure 28. Traditional Adjustable Configuration With External Resistors

Table 2. Recommended Feedback-Resistor Values

$V_{OUT(TARGET)}$ (V)	E96 SERIES		R40 SERIES	
	R1 (kΩ)	R2 (kΩ)	R1 (kΩ)	R2 (kΩ)
1	30.1	30.1	30	30
1.2	39.2	28	43.7	31.5
1.5	61.9	30.9	60	30
1.8	80.6	30.9	80	30.7
1.9	86.6	30.9	87.5	31.5
2.5	115	28.7	112	28
3	147	29.4	150	30
3.3	165	29.4	175	31.5
5	280	30.9	243	27.2

7.3.3 Undervoltage Lockout (UVLO)

The TPS7A7100 uses an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a deglitch feature that typically ignores undershoot of the input voltage upon the event of device start-up. Still, a poor input line impedance may cause a severe input voltage drop when the device powers on. As explained in the *Input Capacitor Requirements* section, the input line impedance must be well-designed.

7.3.4 Soft-Start

The TPS7A7100 has an SS pin that provides a soft-start (slow start) function.

By leaving the SS pin open, the TPS7A7100 performs a soft-start by its default setting.

As shown in *Functional Block Diagram*, by connecting a capacitor between the SS pin and the ground, the C_{SS} capacitor forms an RC pair together with the integrated 50-kΩ resistor. The RC pair operates as an RC-delay circuit for the soft-start together with the internal 700-µs delay circuit.

The relationship between C_{SS} and the soft-start time is shown in through .

7.3.5 Current Limit

The TPS7A7100 internal current limit circuitry protects the regulator during fault conditions. During a current limit event, the output sources a fixed amount of current that is mostly independent of the output voltage. The current limit function is provided as a fail-safe mechanism and is not intended to be used regularly. Do **not** design any applications to use this current limit function as a part of expected normal operation. Extended periods of current limit operation degrade device reliability.

Powering on the device with the enable pin, or increasing the input voltage above the minimum operating voltage while a low-impedance short exists on the output of the device, may result in a sequence of high-current pulses from the input to the output of the device. The energy consumed by the device is minimal during these events; therefore, there is no failure risk. Additional input capacitance helps to mitigate the load transient requirement of the upstream supply during these events.

7.3.6 Enable

The EN pin switches the enable and disable (shutdown) states of the TPS7A7100. A logic high input at the EN pin enables the device; a logic low input disables the device. When disabled, the device current consumption is reduced.

7.3.7 Power Good

The TPS7A7100 has a power good function that works with the PG output pin. When the output voltage undershoots the threshold voltage $V_{IT(PG)}$ during normal operation, the PG open-drain output turns from a high-impedance state to a low-impedance state. When the output voltage exceeds the $V_{IT(PG)}$ threshold by an amount greater than the PG hysteresis, $V_{hys(PG)}$, the PG open-drain output turns from a low-impedance state to high-impedance state. By connecting a pullup resistor (usually between OUT and PG pins), any downstream device can receive an active-high enable logic signal.

When setting the output voltage to less than 1.8 V and using a pullup resistor between OUT and PG pins, depending on the downstream device specifications, the downstream device may not accept the PG output as a valid high-level logic voltage. In such cases, place a pullup resistor between IN and PG pins, not between OUT and PG pins.

Figure 18 shows the open-drain output drive capability. The on-resistance of the open-drain transistor is calculated using Figure 18, and is approximately 200 Ω. Any pullup resistor greater than 10 kΩ works fine for this purpose.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(MIN)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device (such as a bipolar junction transistor, or BJT) is in saturation and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 3 lists the conditions that lead to the different modes of operation.

Table 3. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(NOM)} + V_{DO}$ and $V_{IN} > V_{IN(MIN)}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{(LIM)}$	$T_J < 125°C$
Dropout mode	$V_{IN} < V_{OUT(NOM)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	—	$V_{EN} < V_{IL(EN)}$	—	$T_J > 160°C$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A7100 is a very-low dropout LDO with very fast load transient response. The TPS7A7100 provides a number of features such as a power good signal for output monitoring, a soft-start pin to reduce inrush currents during start-up, and it is suitable for applications that require up to 3 A of output current.

8.2 Typical Application

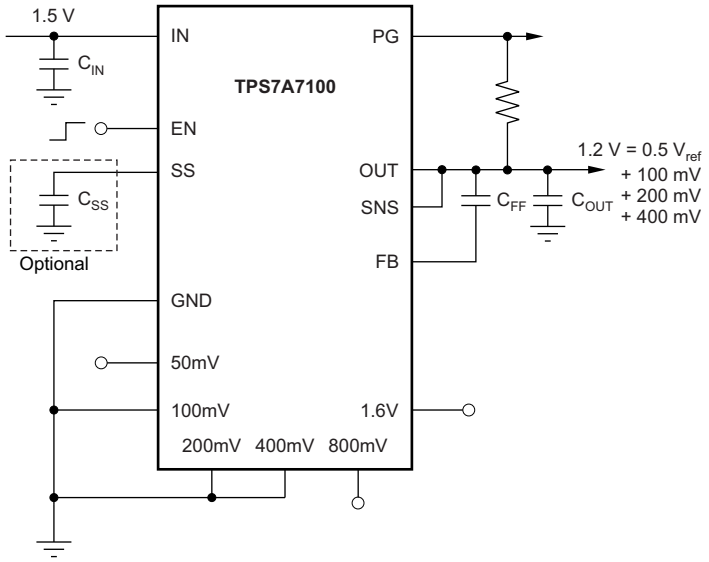


Figure 29. 1.2-V Output Using ANY-OUT Pins

8.2.1 Design Requirements

Table 4 lists the design parameters for this example.

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.425 V to 6.5 V
Output voltage	1.2 V
Output current rating	3 A
Output capacitor range	4.7 µF to 200 µF
feedforward capacitor range	220 pF to 100 nF
Soft-Start capacitor range	0 to 1 µF

8.2.2 Detailed Design Procedure

8.2.2.1 ANY-OUT Programmable Output Voltage

For ANY-OUT operation, the TPS7A7001 does not use any external resistors to set the output voltage, but uses device pins labeled 50 mV, 100 mV, 200 mV, 400 mV, 800 mV, and 1.6 V to set the regulated output voltage. Each pin is either connected to ground (active) or is left open (floating). The ANY-OUT programming is set as the sum of the internal reference voltage ($V_{(SS)}$ = 0.5 V) plus the sum of the respective voltages assigned to each active pin. By leaving all ANY-OUT pins open, or floating, the output is set to the minimum possible output voltage equal to $V_{(SS)}$. By grounding all of the ANY-OUT pins, the output is set to 3.65 V.

When using the ANY-OUT pins, the SNS pin must always be connected between the OUT and FB pins. However, the feedforward capacitor must be connected to the FB pin, not the SNS pin.

8.2.2.2 Traditional Adjustable Output Voltage

For applications that need the regulated output voltage to be greater than 3.65 V (or those that require more resolution than the 50 mV that the ANY-OUT pins provide), the TPS7A7100 can also be use the traditional adjustable method of setting the regulated output.

When using the traditional method of setting the output, the FB pin must be connected to the node connecting the top and bottom resistors of the resistor divider. The SNS pin must be left floating.

8.2.2.3 Input Capacitor Requirements

As a result of its very fast transient response and low-dropout operation support, it is necessary to reduce the line impedance at the input pin of the TPS7A7100. The line impedance depends heavily on various factors, such as wire (PCB trace) resistance, wire inductance, and output impedance of the upstream voltage supply (power supply to the TPS7A7100). Therefore, a specific value for the input capacitance cannot be recommended until the previously listed factors are finalized.

In addition, simple usage of large input capacitance can form an unwanted LC resonance in combination with input wire inductance. For example, a 5-nH inductor and a 10-µF input capacitor form an LC filter that has a resonance at 712 kHz. This value of 712 kHz is well inside the bandwidth of the TPS7A7100 control loop.

The best guideline is to use a capacitor of up to 1 µF with well-designed wire connections (PCB layout) to the upstream supply. If it is difficult to optimize the input line, use a large tantalum capacitor in combination with a good-quality, low-ESR, 1-µF ceramic capacitor.

8.2.2.4 Output Capacitor Requirements

The TPS7A7100 is designed to be stable with standard ceramic capacitors with capacitance values from 4.7 µF to 47 µF without a feedforward capacitor. For output capacitors from 47 µF to 200 µF a feedforward capacitor of at least 220 pF must be used. The TPS7A7100 is evaluated using an X5R-type, 10-µF ceramic capacitor. TI highly recommends the X5R- and X7R-type capacitors because they have minimal variation in value and ESR over temperature. Maximum ESR must be less than 1 Ω.

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude, but increases duration of the transient response.

8.2.3 Application Curves

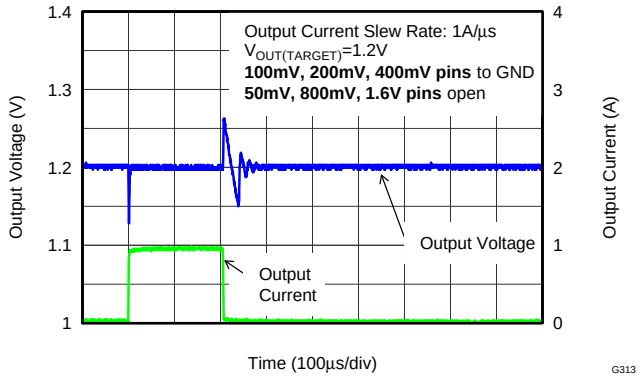


Figure 30. Load Transient Response (V_{OUT} = 1.2 V)

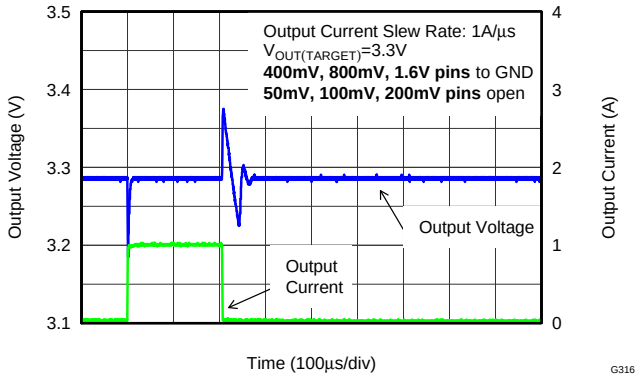


Figure 31. Load Transient Response (V_{OUT} = 3.3 V)

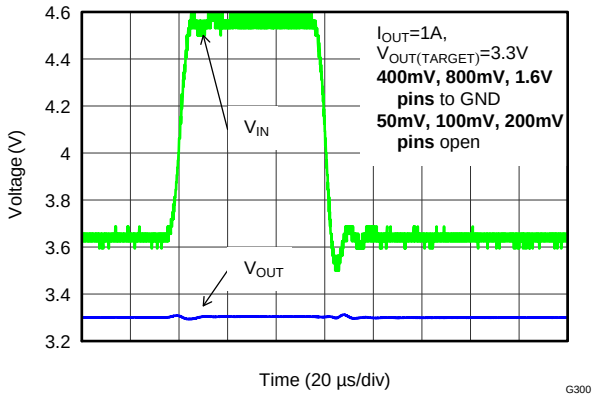


Figure 32. Line Transient Response

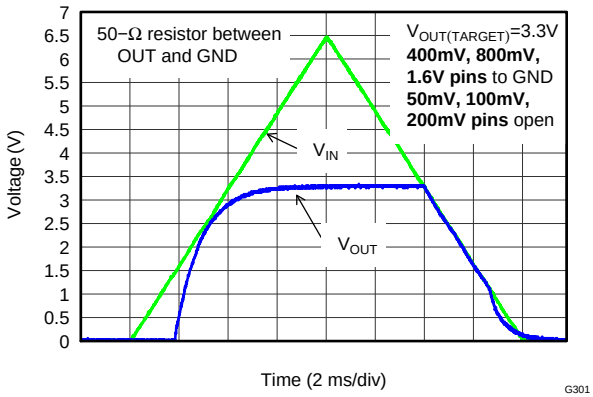


Figure 33. Power Up and Power Down (IN = EN)

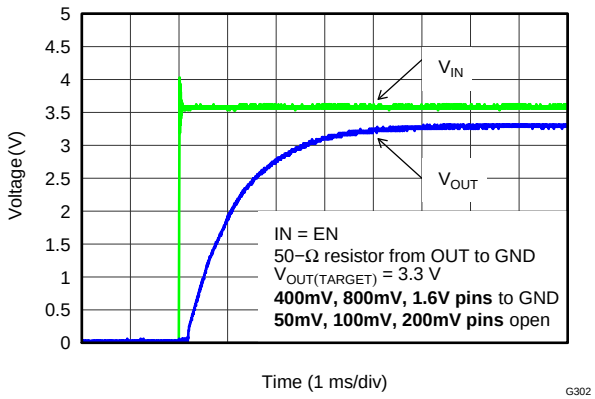


Figure 34. Turnon Response (IN = EN)

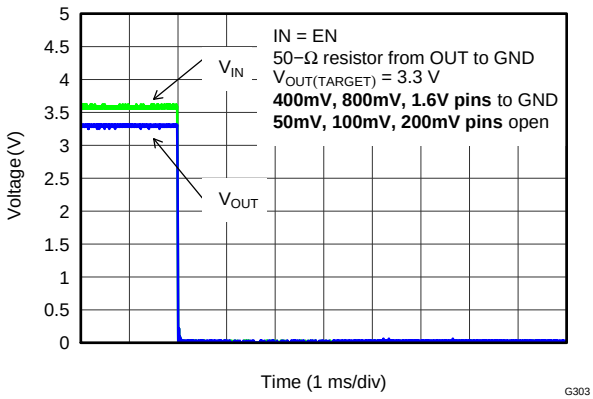


Figure 35. Turnoff Response (IN = EN)

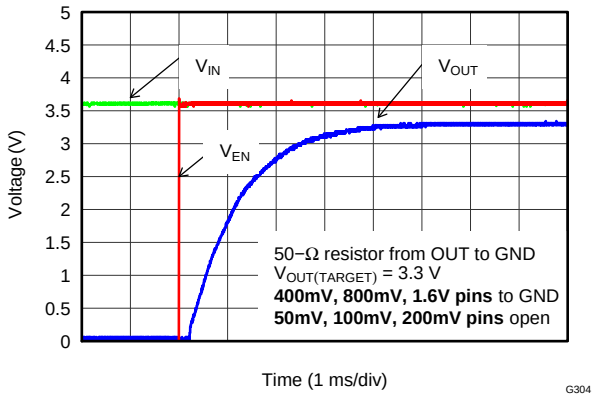


Figure 36. EN Pulse On Response (Over Stable V_{IN})

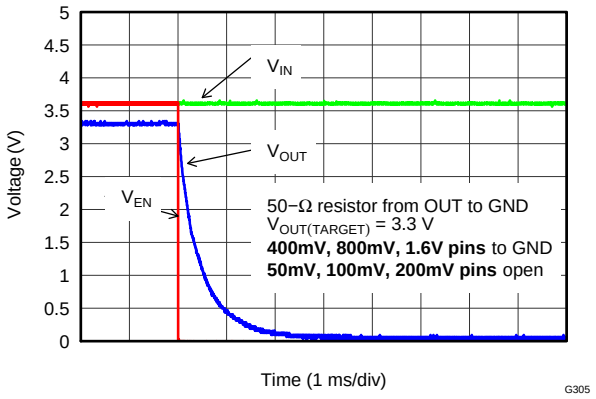


Figure 37. EN Pulse Off Response (Over Stable V_{IN})

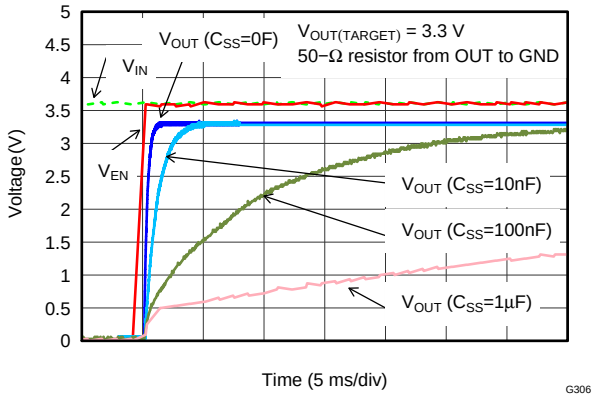


Figure 38. Soft-Start Delay vs C_{SS} (Enlarged View)

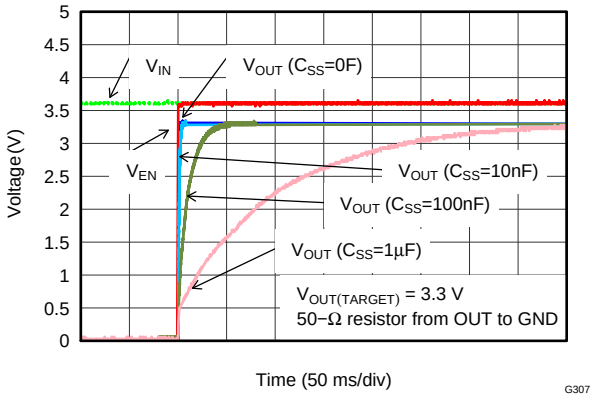


Figure 39. Soft-Start Delay vs C_{SS} (Reduced View)

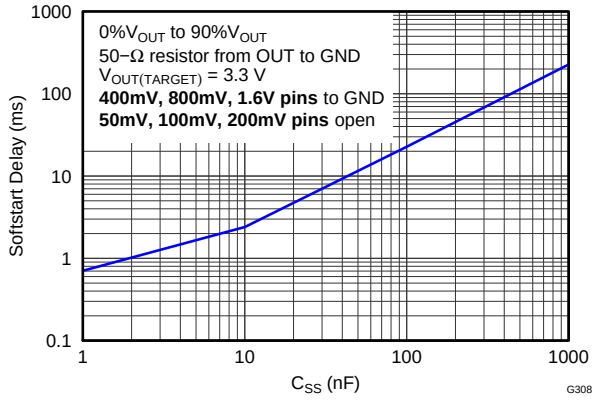


Figure 40. Soft-Start Delay vs C_{SS}

9 Power Supply Recommendations

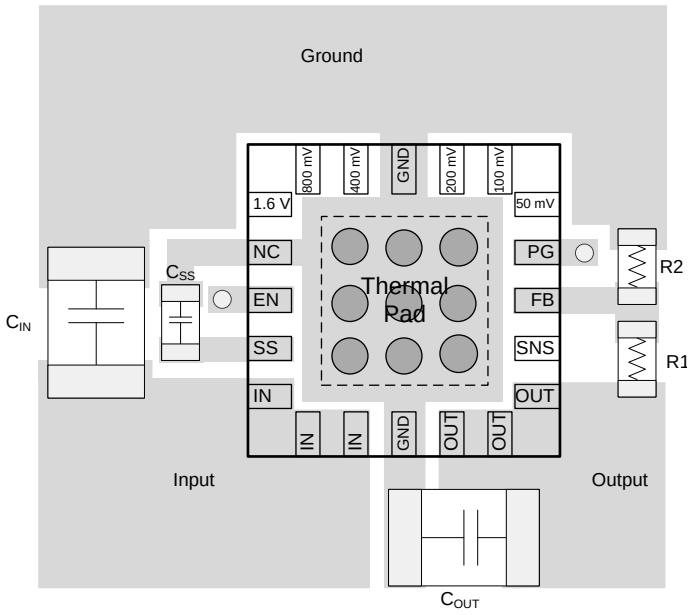
This device is designed for operation from an input voltage supply ranging from 1.425 V to 6.5 V. This input supply must be well regulated. The TPS7A7100 family of fast-transient, low-dropout linear regulators achieve stability with a minimum output capacitance of 4.7 μF; however, TI recommends using 10-μF ceramic capacitors for both the input and output to maximize AC performance.

10 Layout

10.1 Layout Guidelines

- To improve AC performance such as PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device.
- In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.
- Equivalent series inductance (ESL) and ESR must be minimized to maximize performance and ensure stability.
- Every capacitor must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.
- Do **not** place any of the capacitors on the opposite side of the PCB from where the regulator is installed.
- The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.
- If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for the TPS7A7100 evaluation board, SLAU430.

10.2 Layout Example



Notes: C_{in} and C_{out} are 0805 packages
C_{SS}, R_1, and R_2 are 0402 packages
R_1 and R_2 only needed for adjustable operation
○Denotes a via to a connection made on another layer

Figure 41. TPS7A7100 Recommended Layout

10.3 Thermal Considerations

The thermal protection feature disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal-protection circuit may cycle on and off. This thermal limit protects the device from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest-expected ambient temperature and worst-case load.

The internal-protection circuitry of the TPS7A7100 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A7100 into thermal shutdown degrades device reliability.

10.4 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 1:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{1}$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the VQFN (RGW or RGT) package, the primary conduction path for heat is through the exposed pad to the PCB. The pad can be connected to ground or be left floating; however, it must be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 2:

$$R_{\theta JA} = \left(\frac{+125°C - T_A}{P_D} \right) \tag{2}$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 42.

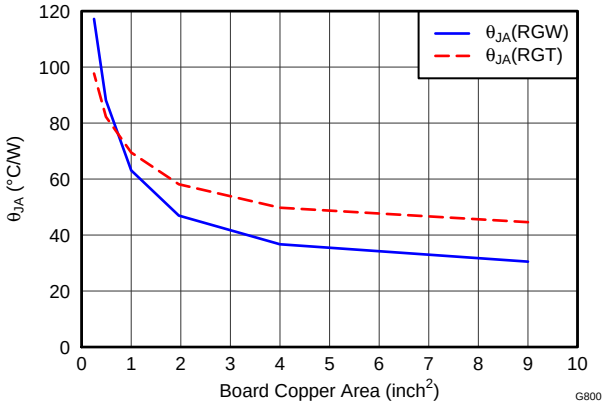


Figure 42. θ_{JA} vs Board Size

Power Dissipation (continued)

Figure 42 shows the variation of θ_{JA} as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and must not be used to estimate actual thermal performance in real application environments.

NOTE

When the device is mounted on an application PCB, TI strongly recommends using Ψ_{JT} and Ψ_{JB}, as explained in the *Estimating Junction Temperature* section.

10.5 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 3). For backwards compatibility, an older $\theta_{JC,}$*Top* parameter is listed as well.

Ψ_{JT}: $T_J = T_T + \Psi_{JT} \bullet P_D$

Ψ_{JB}: $T_J = T_B + \Psi_{JB} \bullet P_D$

Where:

P_D is the power dissipation shown by Equation 2.

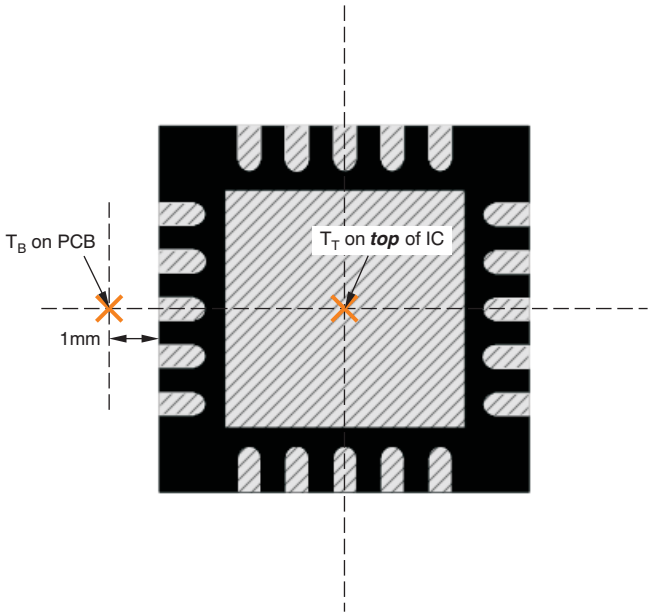
T_T is the temperature at the center-top of the IC package.

T_B is the PCB temperature measured 1 mm away from the IC package *on the PCB surface* (see Figure 43). (3)

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the Application Report SBVA025, *Using New Thermal Metrics*.



(a) Example RGW (QFN) Package Measurement

Figure 43. Measuring Points For T_T And T_B

Estimating Junction Temperature (continued)

By looking at Figure 44, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have very little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with Equation 3 is a good way to estimate T_J by simply measuring T_T or T_B, regardless of the application board size.

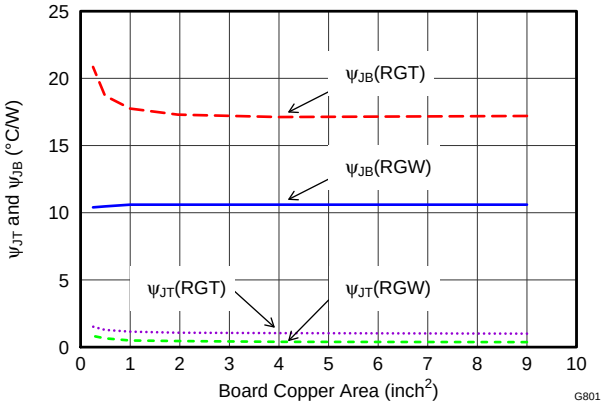


Figure 44. Ψ_{JT} And Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see Application Report SBVA025, *Using New Thermal Metrics*. For further information, see Application Report SPRA953, *Semiconductor and IC Package Thermal Metrics*.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

- *《使用前馈电容器和低压降稳压器的优缺点》*，SBVA042。
- *《使用新的热指标》*，SBVA025。
- *《TPS7A7x00EVM-718 评估模块》*，SLAU430。
- *《半导体和 IC 封装热指标》*，SPRA953。

11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商标

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11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A7100RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYLQ	Samples
TPS7A7100RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYLQ	Samples
TPS7A7100RGWR	ACTIVE	VQFN	RGW	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBS	Samples
TPS7A7100RGWT	ACTIVE	VQFN	RGW	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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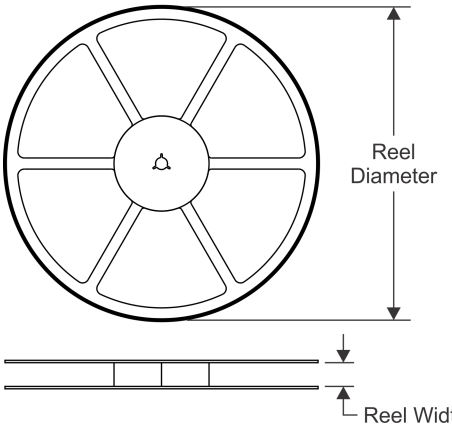
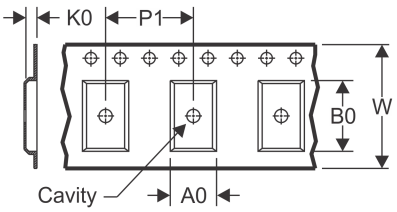
TAPE AND REEL INFORMATION

REEL DIMENSIONS

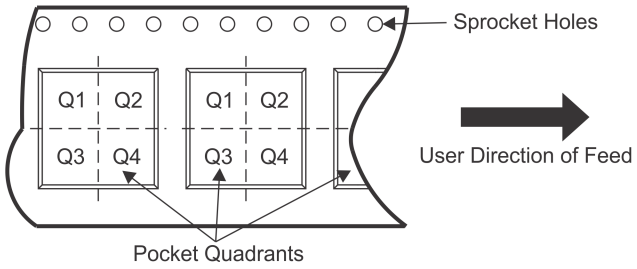


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

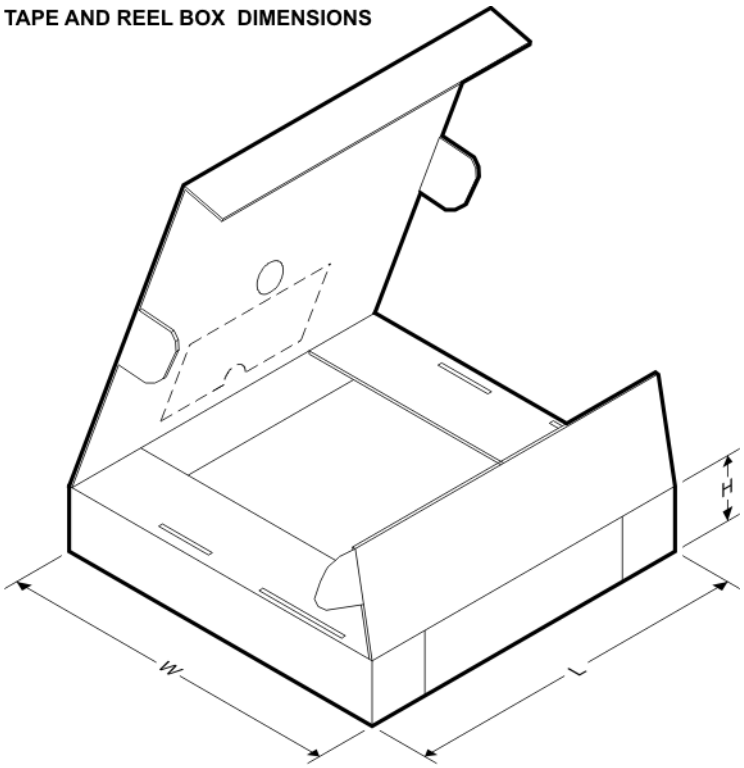
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A7100RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7A7100RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7A7100RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS7A7100RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

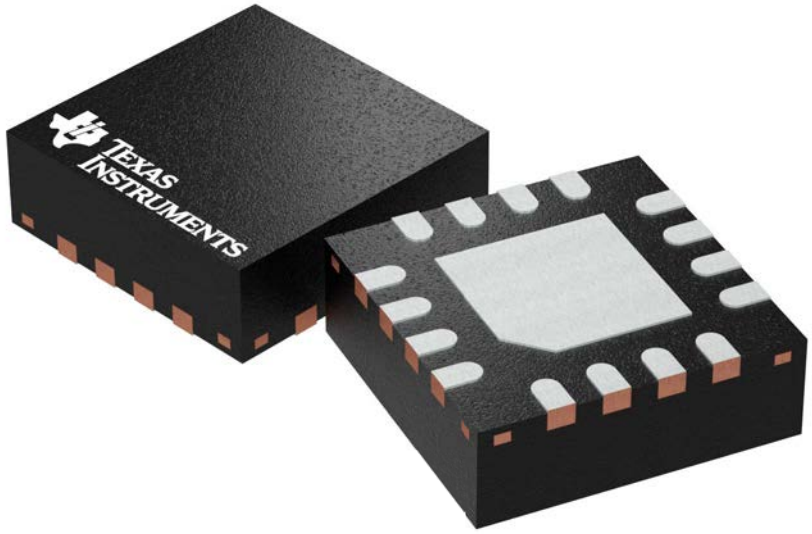


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A7100RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS7A7100RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS7A7100RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS7A7100RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

GENERIC PACKAGE VIEW

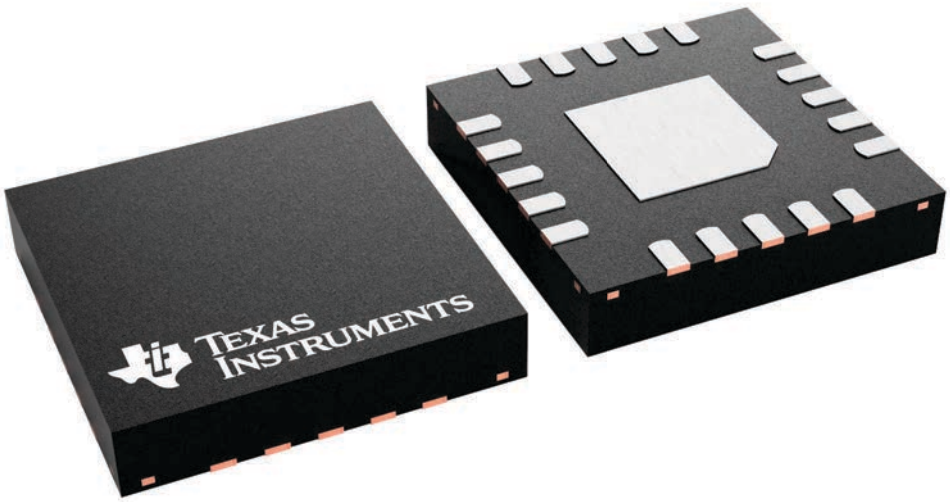
RGW 20

VQFN - 1 mm max height

5 x 5, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



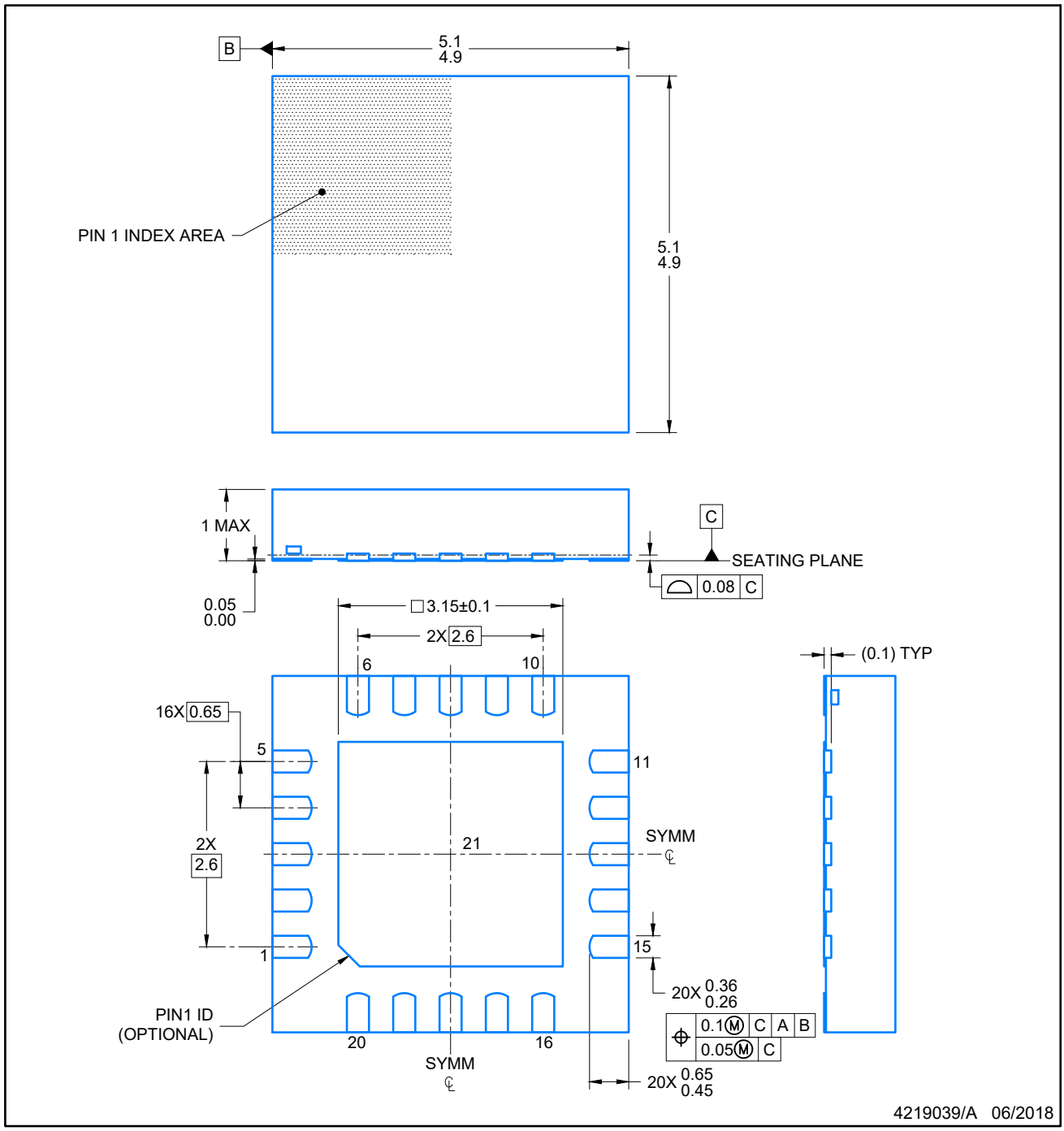
4227157/A

PACKAGE OUTLINE

RGW0020A

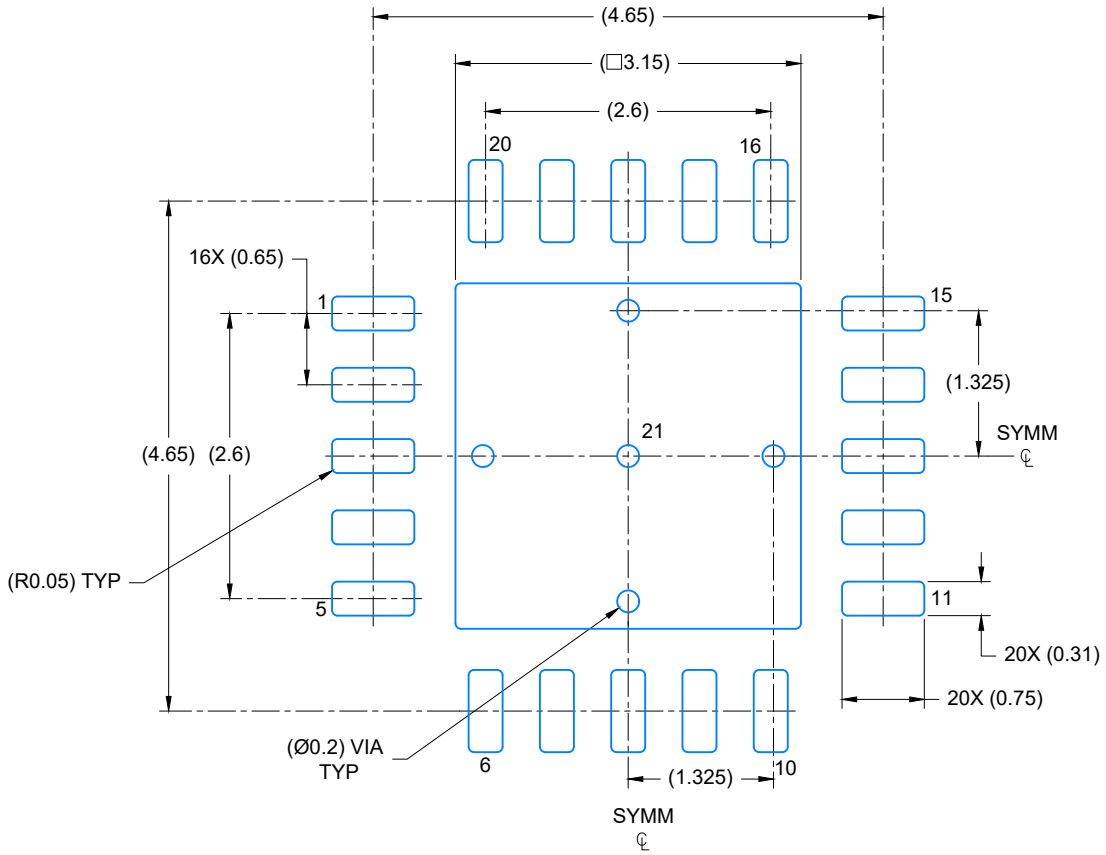
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



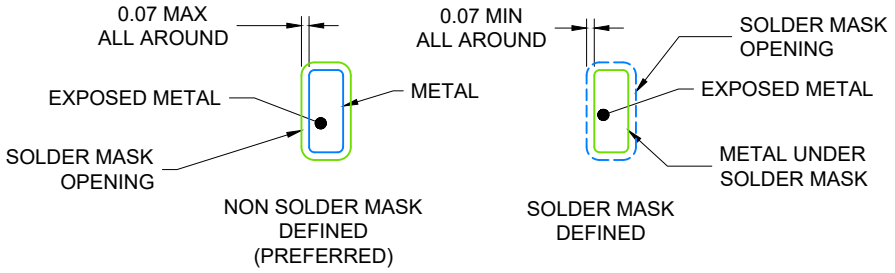
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 15X

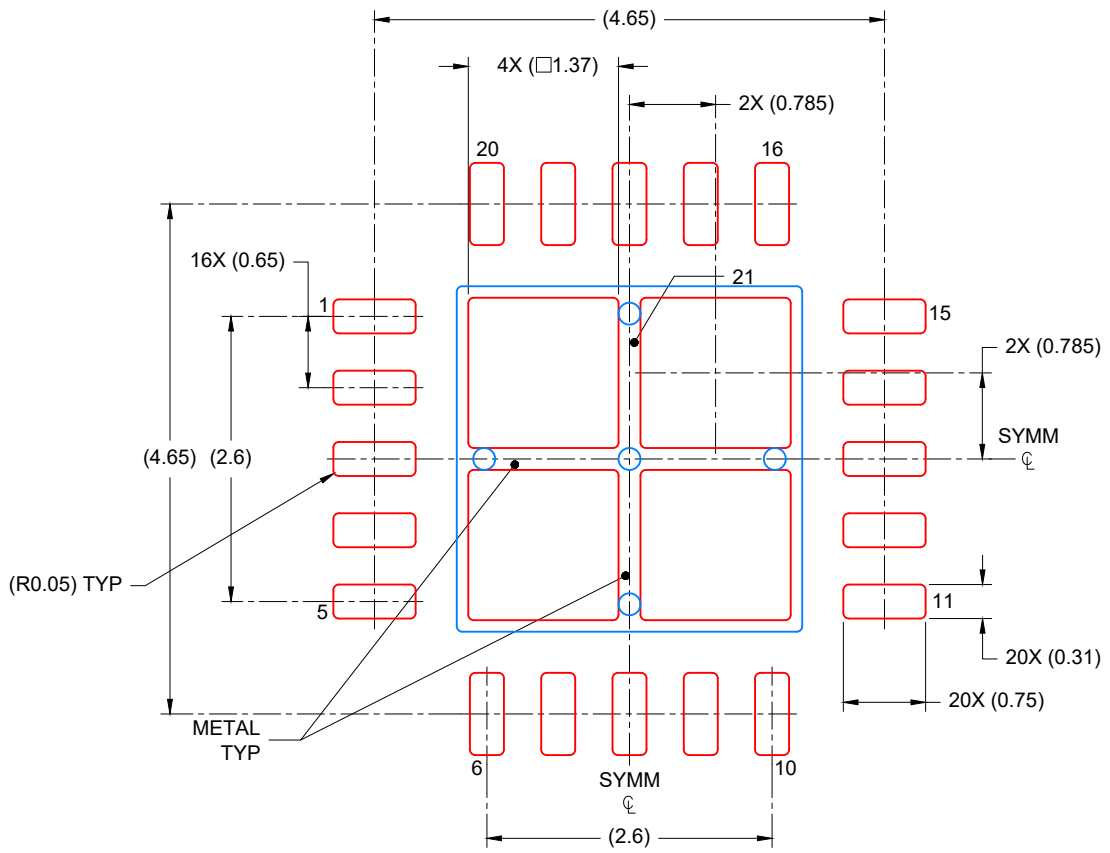


SOLDER MASK DETAILS

4219039/A 06/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

4219039/A 06/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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