

NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE82H110D uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

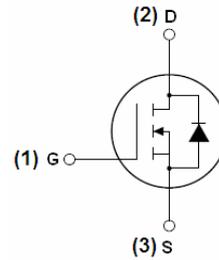
- $V_{DS} = 82V, I_D = 110A$
 $R_{DS(ON)} < 7m\Omega @ V_{GS}=10V$ (Typ:5.9m Ω)
- Special process technology for high ESD capability
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

100% ΔV_d s TESTED!



Schematic diagram



Marking and pin assignment



TO-263-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE82H110D	NCE82H110D	TO-263-2L	-	-	-

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	82	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	110	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D(100^\circ C)$	81	A
Pulsed Drain Current	I_{DM}	350	A
Maximum Power Dissipation	P_D	200	W
Derating factor		1.33	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	950	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta jc}$	0.75	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

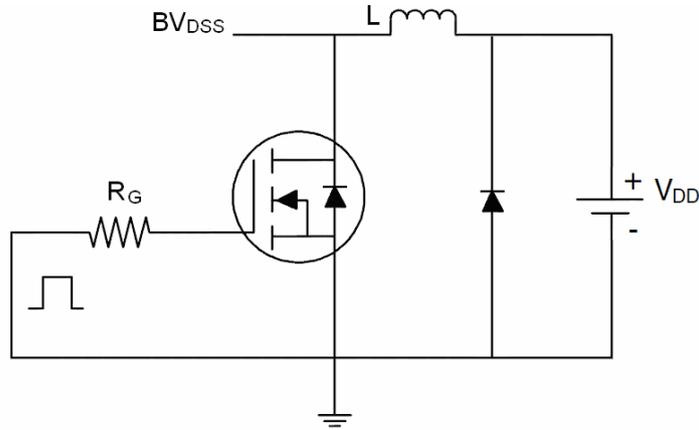
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	82	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=82V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$	-	5.9	7.0	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=20A$	60	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=40V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	6400	-	PF
Output Capacitance	C_{oss}		-	334	-	PF
Reverse Transfer Capacitance	C_{rss}		-	318	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, R_L=1\Omega$ $V_{GS}=10V, R_{GEN}=2.5\Omega$	-	21	-	nS
Turn-on Rise Time	t_r		-	39	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	70	-	nS
Turn-Off Fall Time	t_f		-	24	-	nS
Total Gate Charge	Q_g	$V_{DS}=40V, I_D=20A,$ $V_{GS}=10V$	-	120	-	nC
Gate-Source Charge	Q_{gs}		-	25.4	-	nC
Gate-Drain Charge	Q_{gd}		-	39.4	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=110A$	-	-	1.2	V
Diode Forward Current ^(Note 2)	I_S	-	-	-	110	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}, I_F = 20A$	-	43	-	nS
Reverse Recovery Charge	Q_{rr}	$di/dt = 100A/\mu s$ ^(Note 3)	-	93	-	nC

Notes:

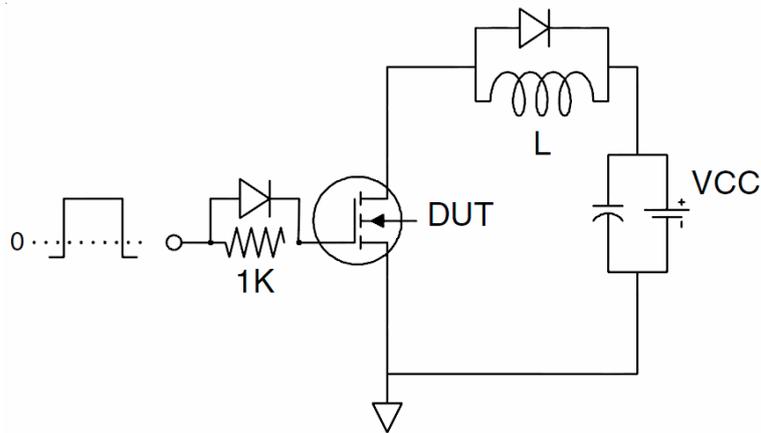
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=40V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

Test circuit

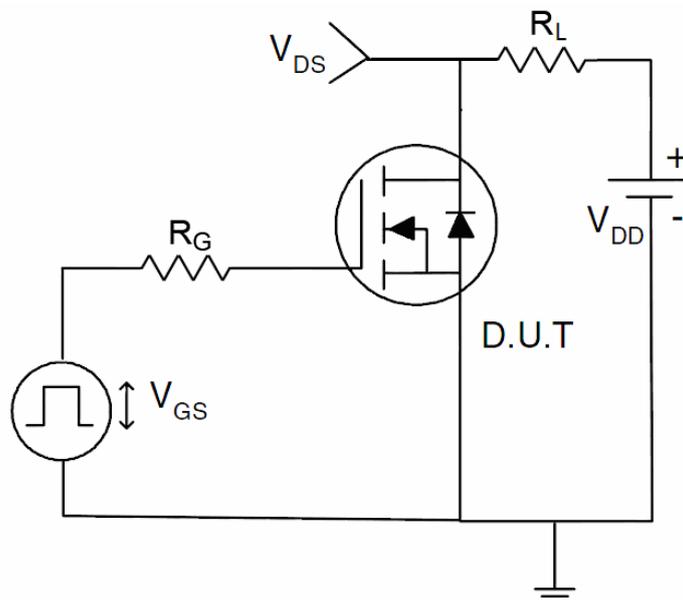
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

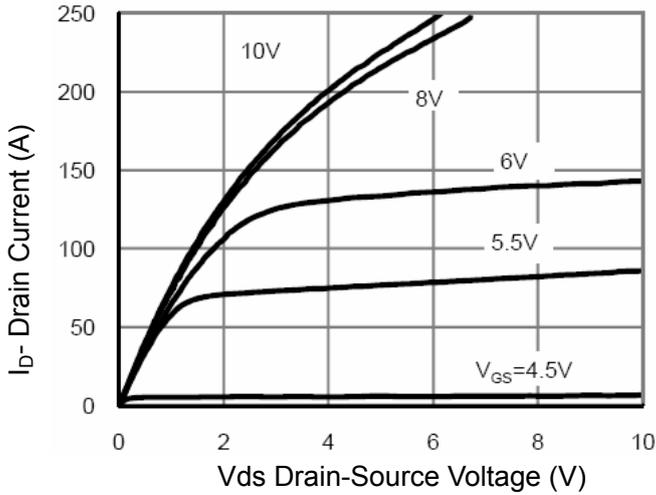


Figure 1 Output Characteristics

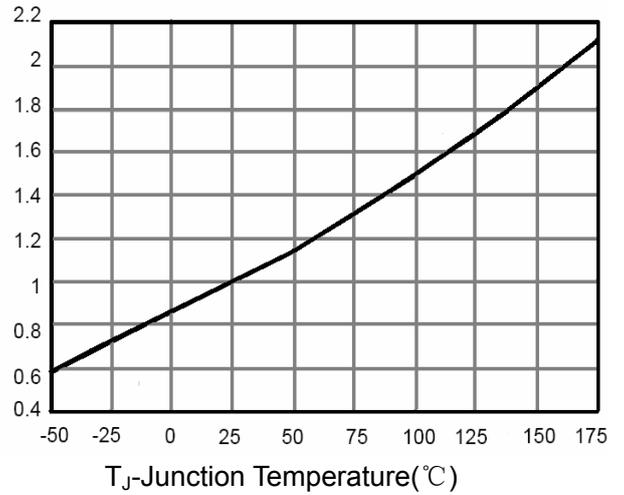


Figure 4 R_{dson} -Junction Temperature

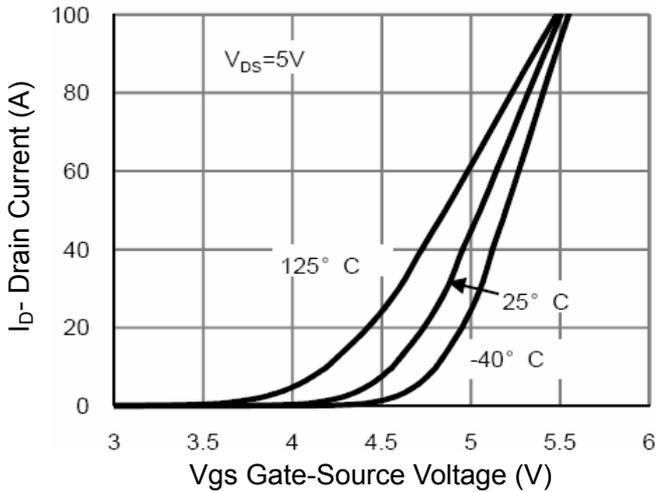


Figure 2 Transfer Characteristics

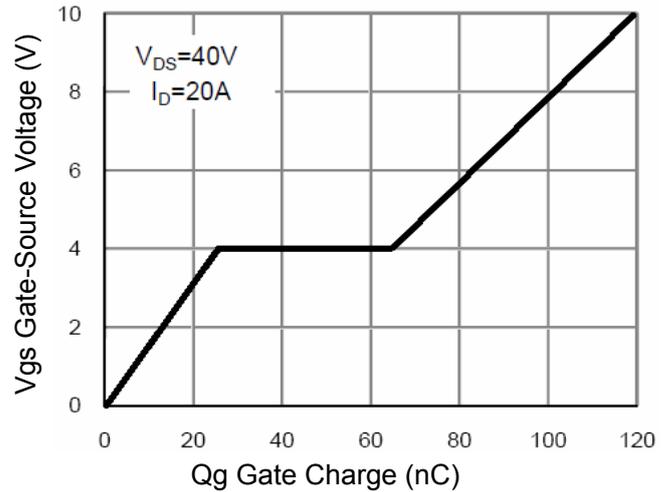


Figure 5 Gate Charge

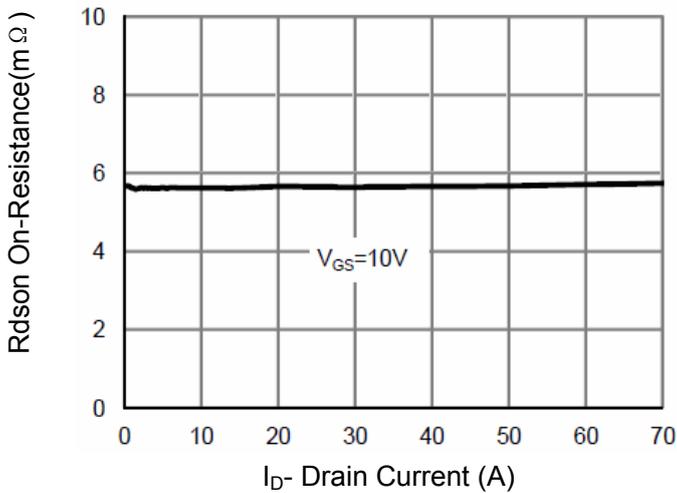


Figure 3 R_{dson} - Drain Current

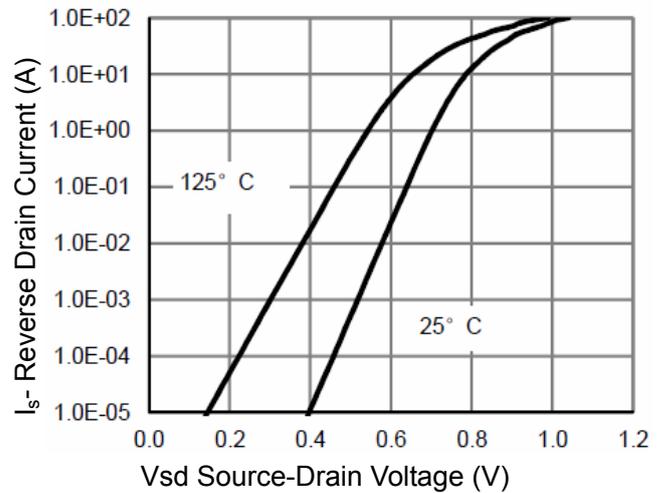


Figure 6 Source- Drain Diode Forward

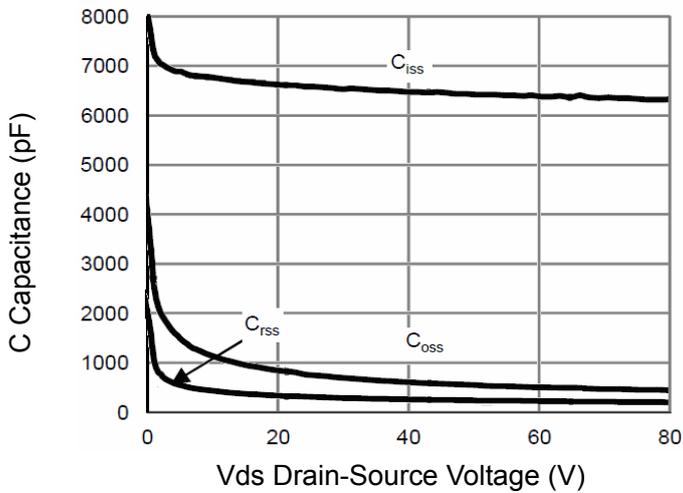


Figure 7 Capacitance vs Vds

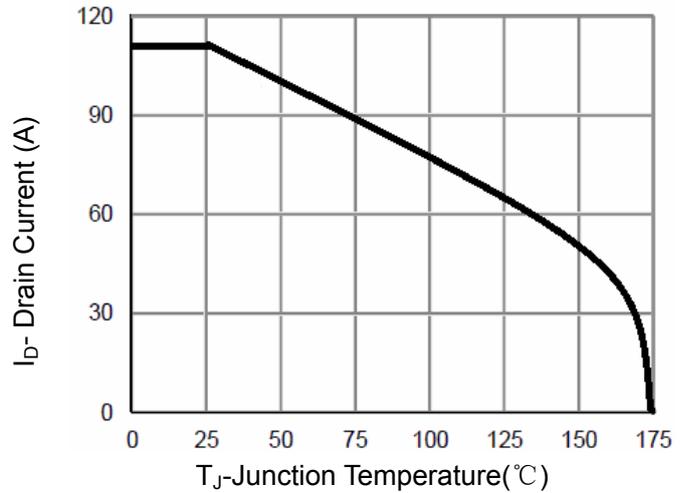


Figure 9 Current De-rating

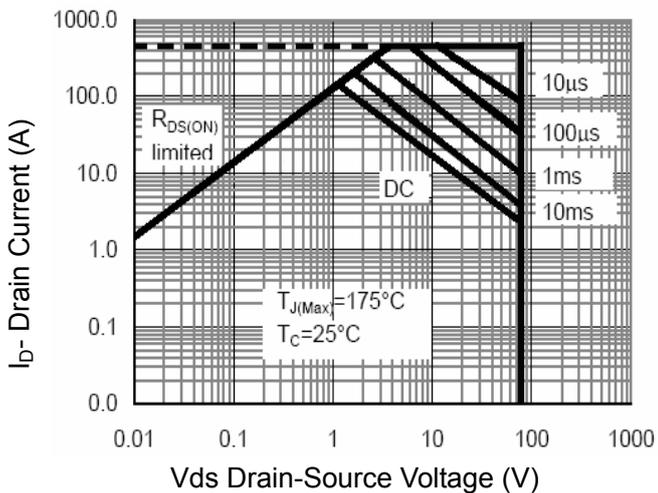


Figure 8 Safe Operation Area

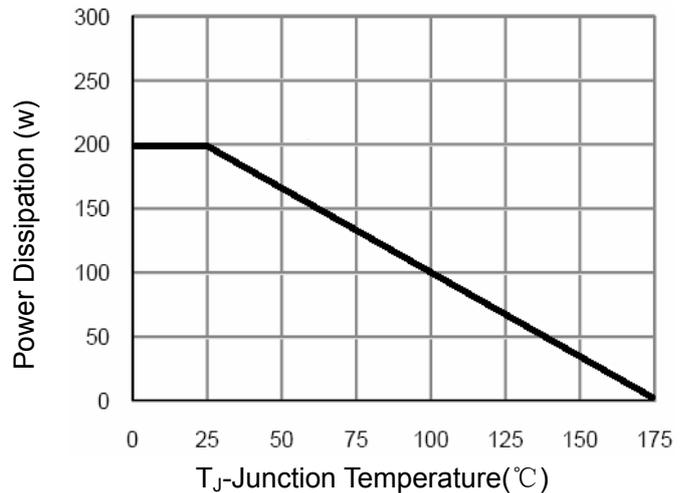


Figure 10 Power De-rating

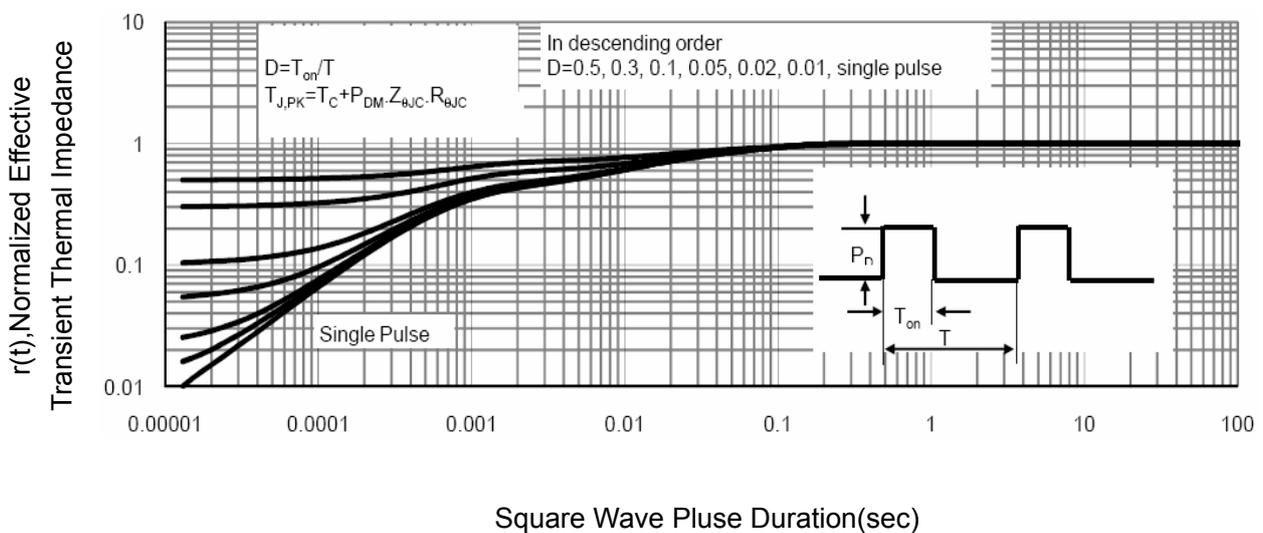


Figure 11 Normalized Maximum Transient Thermal Impedance

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