LM2703 Micropower Step-Up DC/DC Converter with 350mA Peak Current Limit

Check for Samples: LM2703

FEATURES

- **350mA, 0.7Ω, Internal Switch**
- **Uses Small Surface Mount Components**
- **Adjustable Output Voltage up to 21V**
- **2.2V to 7V Input Range**
- **Input Undervoltage Lockout**
- **0.01µA Shutdown Current**
- **Small 5-Lead SOT-23 Package**

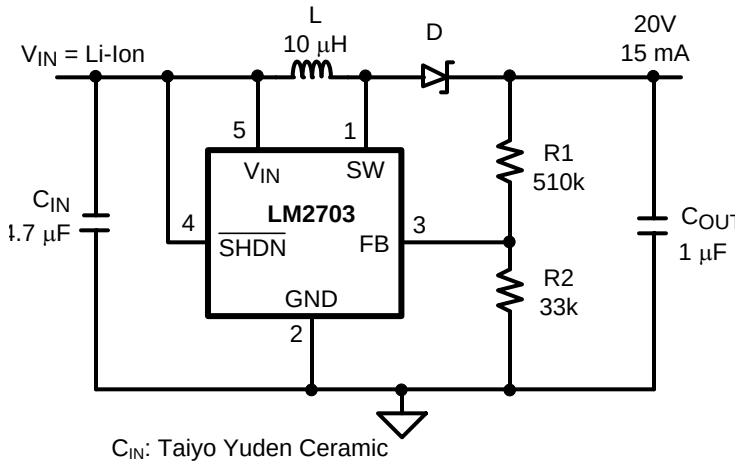
APPLICATIONS

- **LCD Bias Supplies**
- **White LED Back-Lighting**
- **Handheld Devices**
- **Digital Cameras**
- **Portable Applications**

DESCRIPTION

The LM2703 is a micropower step-up DC/DC in a small 5-lead SOT-23 package. A current limited, fixed off-time control scheme conserves operating current resulting in high efficiency over a wide range of load conditions. The 22V switch allows for output voltages as high as 21V. The low 400ns off-time permits the use of tiny, low profile inductors and capacitors to minimize footprint and cost in space-conscious portable applications. The LM2703 is ideal for LCD panels requiring low current and high efficiency as well as white LED applications for cellular phone back-lighting. The LM2703 can drive up to 4 white LEDs from a single Li-Ion battery.

Typical Application Circuit

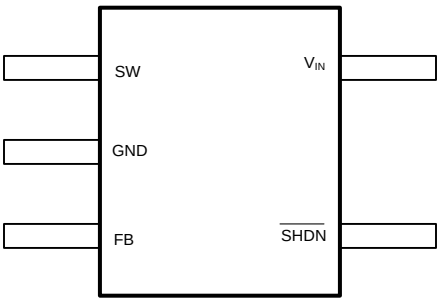


C_{IN}: Taiyo Yuden Ceramic
C_{OUT}: Taiyo Yuden Ceramic
L: Coilcraft DT1608C-103 or Murata
LQY33PN100M02
(low profile)

Figure 1. Typical 20V Application

Connection Diagram

Top View



The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. See the Electrical Characteristics table for the thermal resistance. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_D(MAX) = (T_{J(MAX)} - T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature.

Figure 2. SOT23-5
T_{Jmax} = 125°C, θ_{JA} = 220°C/W

PIN DESCRIPTIONS

Pin	Name	Function
1	SW	Power Switch input.
2	GND	Ground.
3	FB	Output voltage feedback input.
4	$\overline{SHDN}$	Shutdown control input, active low.
5	V_{IN}	Analog and Power input.

SW (Pin 1): Switch Pin.

This is the drain of the internal NMOS power switch. Minimize the metal trace area connected to this pin to minimize EMI.

GND (Pin 2): Ground Pin.

Tie directly to ground plane.

FB (Pin 3): Feedback Pin.

Set the output voltage by selecting values for R1 and R2 using:

$$R1 = R2 \left(\frac{V_{OUT}}{1.237V} - 1\right) \quad (1)$$

Connect the ground of the feedback network to an AGND plane which should be tied directly to the GND pin.

$\overline{SHDN}$ (Pin 4): Shutdown Pin.

The shutdown pin is an active low control. Tie this pin above 1.1V to enable the device. Tie this pin below 0.3V to turn off the device.

V_{IN} (Pin 5): Input Supply Pin.

Bypass this pin with a capacitor as close to the device as possible.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

V_{IN}	7.5V
SW Voltage	22.5V
FB Voltage	2V
$\overline{SHDN}$ Voltage	7.5V
Maximum Junction Temp. T_J (3)	150°C
Lead Temperature (Soldering 10 sec.)	300°C
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
ESD Ratings (4) Human Body Model Machine Model (5)	 2kV 200V

(1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be ensured. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. See the Electrical Characteristics table for the thermal resistance. The maximum allowable power dissipation at any ambient temperature is calculated using: P_D (MAX) = ($T_{J(MAX)}$ − T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature.
(4) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.
(5) ESD susceptibility using the machine model is 150V for SW pin.

Operating Conditions

Junction Temperature (1)	−40°C to +125°C
Supply Voltage	2.2V to 7V
SW Voltage Max.	22V

(1) All limits ensured at room temperature and at **temperature extremes**. All room temperature limits are 100% production tested or ensured through statistical analysis. All limits at temperature extremes are ensured via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Electrical Characteristics

Specifications in standard type face are for T_J = 25°C and those in **boldface type** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C). Unless otherwise specified. V_{IN} =2.2V.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
I_Q	Device Disabled	FB = 1.3V		40	**70**	µA
	Device Enabled	FB = 1.2V		235	**300**	
	Shutdown	$\overline{SHDN}$ = 0V		0.01	2.5	
V_{FB}	FeedbackTrip Point		**1.189**	1.237	**1.269**	V
I_{CL}	Switch Current Limit		275 **260**	350	400 **400**	mA
I_B	FB Pin Bias Current	FB = 1.23V (3)		30	**120**	nA
V_{IN}	Input Voltage Range		**2.2**		**7.0**	V
R_{DSON}	Switch R_{DSON}			0.7	**1.6**	Ω
T_{OFF}	Switch Off Time			400		ns

(1) All limits ensured at room temperature and at **temperature extremes**. All room temperature limits are 100% production tested or ensured through statistical analysis. All limits at temperature extremes are ensured via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) Feedback current flows into the pin.

Electrical Characteristics (continued)

Specifications in standard type face are for T_J = 25°C and those in **boldface type** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C). Unless otherwise specified. V_{IN} =2.2V.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
I_{SD}	$\overline{SHDN}$ Pin Current	$\overline{SHDN}$ = V_{IN}, T_J = 25°C		0	80	nA
		$\overline{SHDN}$ = V_{IN}, T_J = 125°C		15		
		$\overline{SHDN}$ = GND		0		
I_L	Switch Leakage Current	V_{SW} = 22V		0.05	5	µA
UVP	Input Undervoltage Lockout	ON/OFF Threshold		1.8		V
V_{FB} Hysteresis	Feedback Hysteresis			8		mV
$\overline{SHDN}$ Threshold	$\overline{SHDN}$ low			0.7	**0.3**	V
	$\overline{SHDN}$ High		**1.1**	0.7		
θ_{JA}	Thermal Resistance			220		°C/W

Typical Performance Characteristics

Enable Current vs V_{IN} (Part Switching)

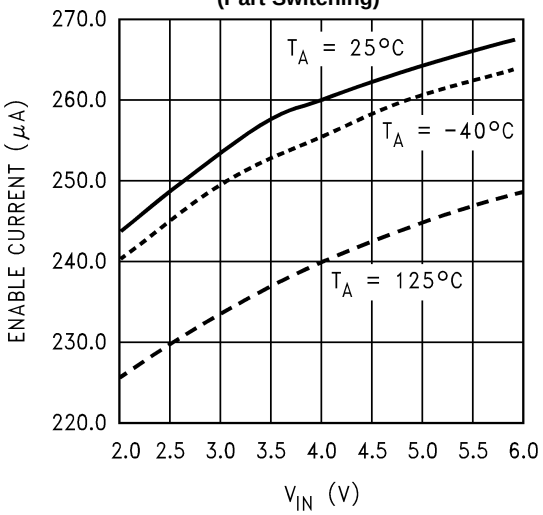


Figure 3.

Disable Current vs V_{IN} (Part Not Switching)

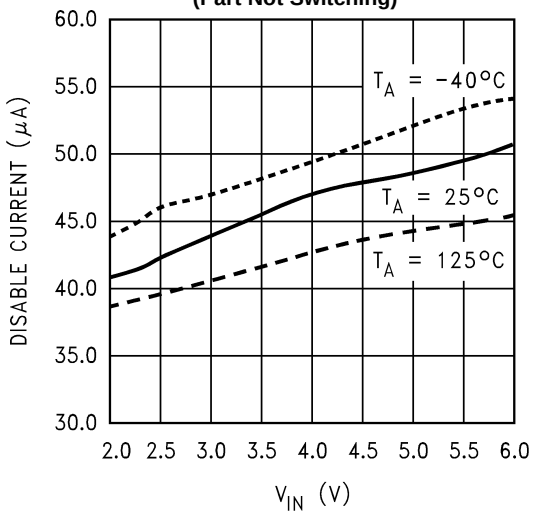


Figure 4.

Efficiency vs Load Current

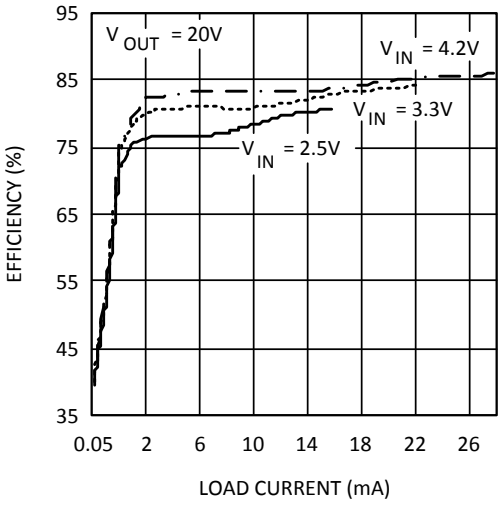


Figure 5.

Efficiency vs Load Current

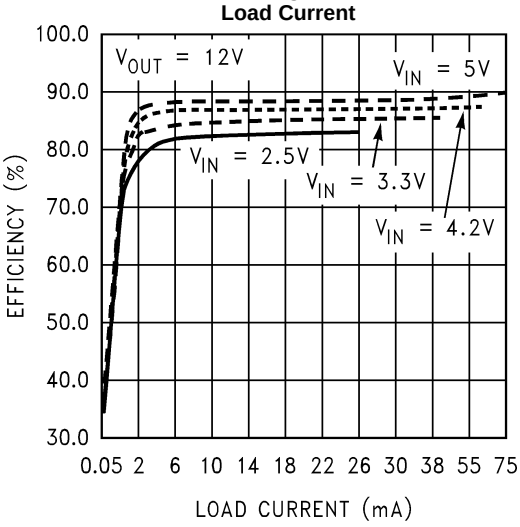


Figure 6.

Typical Performance Characteristics (continued)

Efficiency vs Load Current

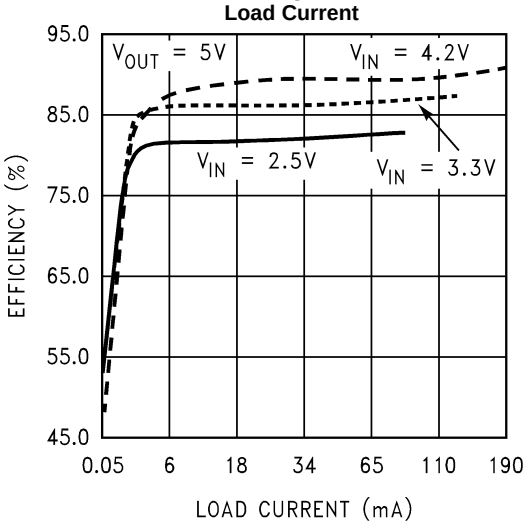


Figure 7.

$\overline{SHDN}$ Threshold vs V_{IN}

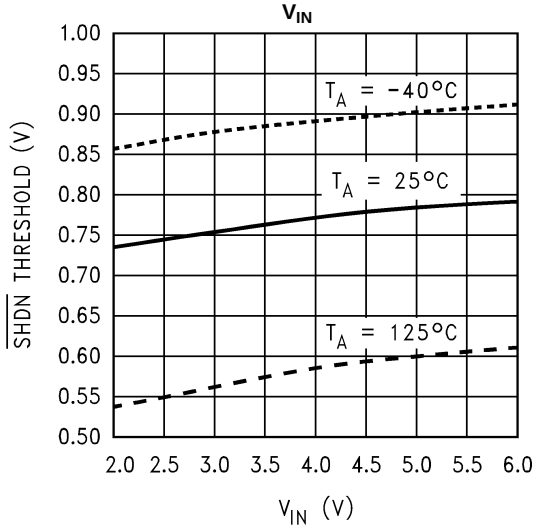


Figure 8.

Switch Current Limit vs V_{IN}

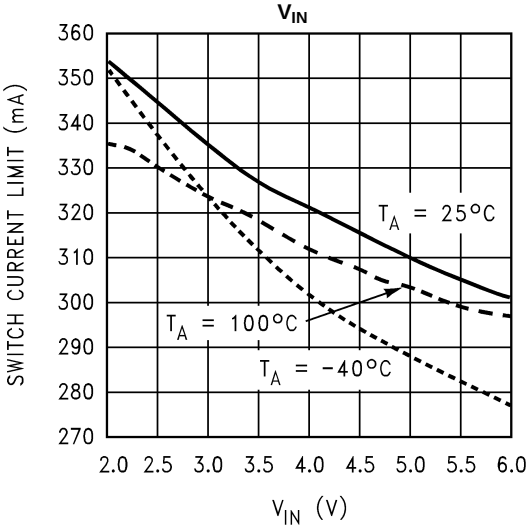


Figure 9.

Switch R_{DSON} vs V_{IN}

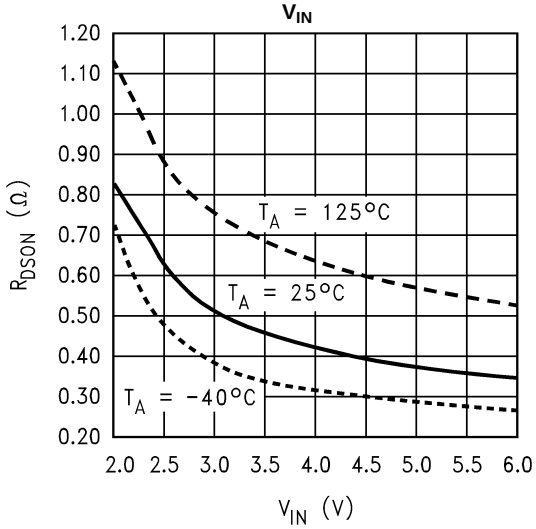


Figure 10.

Typical Performance Characteristics (continued)

FB Trip Point and FB Pin Current vs Temperature

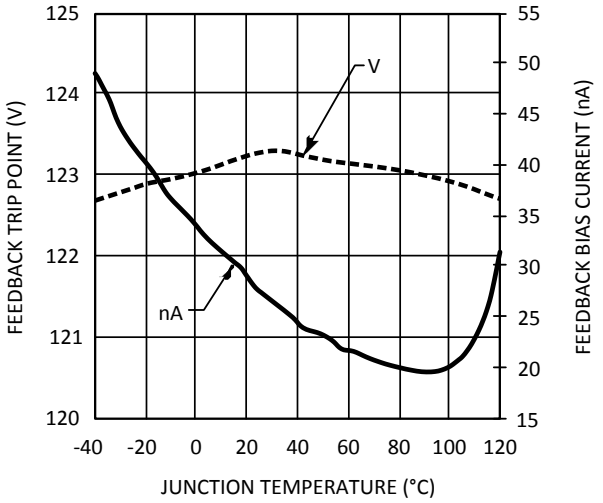


Figure 11.

Output Voltage vs Load Current

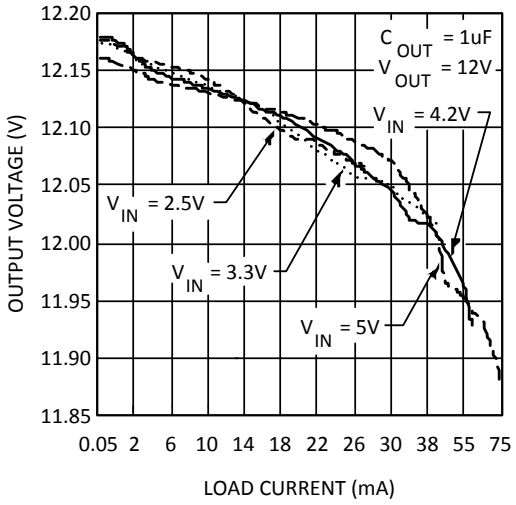
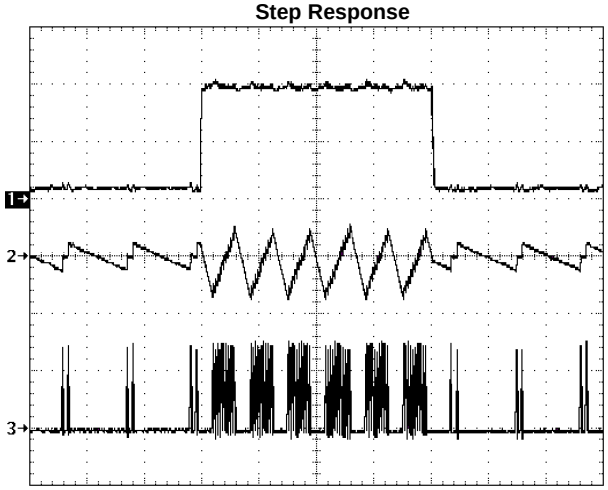


Figure 12.

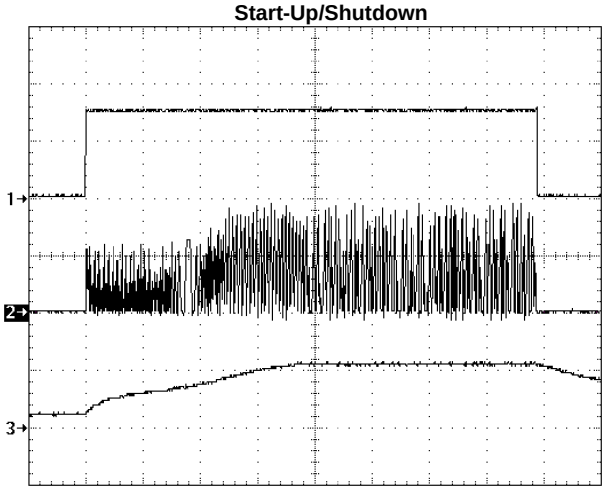
Step Response



V_{OUT} = 20V, V_{IN} = 2.5V
1) Load, 1mA to 10mA to 1mA, DC
2) V_{OUT}, 200mV/div, AC
3) I_L, 200mA/div, DC
T = 50µs/div

Figure 13.

Start-Up/Shutdown



V_{OUT} = 20V, V_{IN} = 2.5V
1) $\overline{SHDN}$, 1V/div, DC
2) I_L, 200mA/div, DC
3) V_{OUT}, 20V/div, DC
T = 400µs/div
R_L = 1.8kΩ

Figure 14.

OPERATION

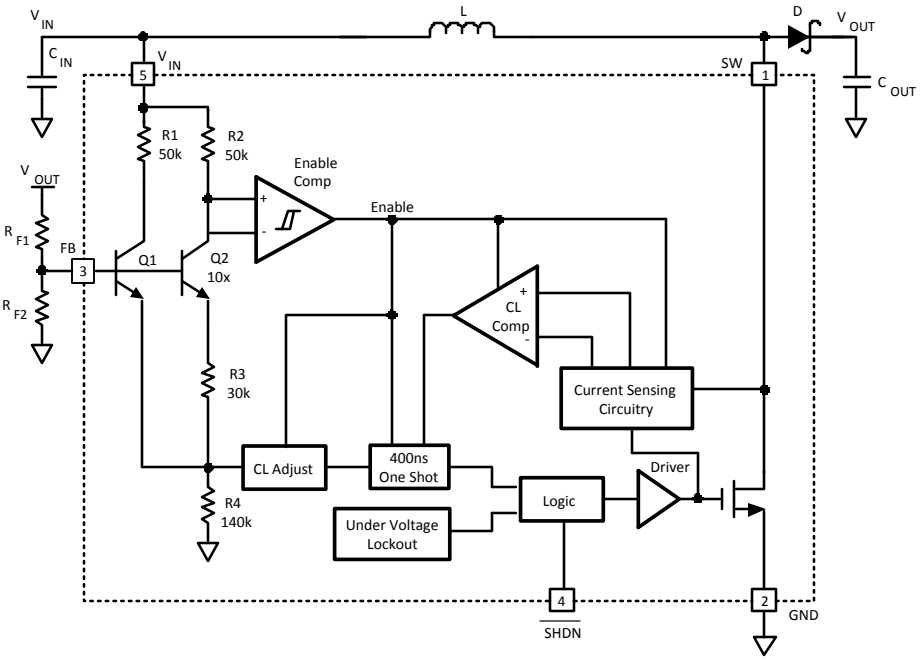
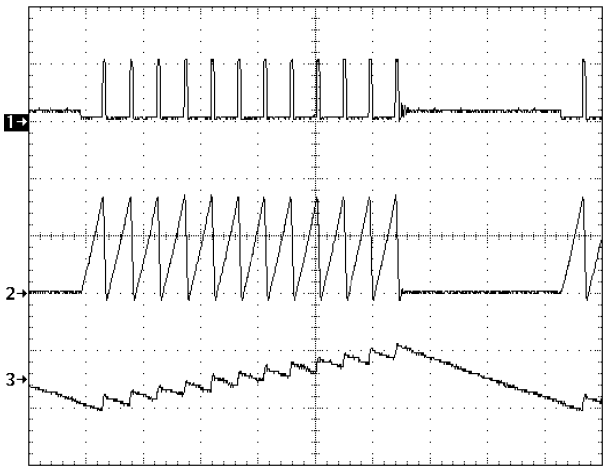


Figure 15. LM2703 Block Diagram



V_{OUT} = 20V, V_{IN} = 2.5V
1) V_{SW}, 20V/div, DC
2) Inductor Current, 200mA/div, DC
3) V_{OUT}, 200mV/div, AC
T = 4µs/div

Figure 16. Typical Switching Waveform

The LM2703 features a constant off-time control scheme. Operation can be best understood by referring to Figure 15 and Figure 16. Transistors Q1 and Q2 and resistors R3 and R4 of Figure 15 form a bandgap reference used to control the output voltage. When the voltage at the FB pin is less than 1.237V, the Enable Comp in Figure 15 enables the device and the NMOS switch is turned on pulling the SW pin to ground. When the NMOS switch is on, current begins to flow through inductor L while the load current is supplied by the output capacitor C_{OUT}. Once the current in the inductor reaches the current limit, the CL Comp trips and the 400ns One Shot turns

off the NMOS switch.The SW voltage will then rise to the output voltage plus a diode drop and the inductor current will begin to decrease as shown in Figure 16. During this time the energy stored in the inductor is transferred to C_{OUT} and the load. After the 400ns off-time the NMOS switch is turned on and energy is stored in the inductor again. This energy transfer from the inductor to the output causes a stepping effect in the output ripple as shown in Figure 16.

This cycle is continued until the voltage at FB reaches 1.237V. When FB reaches this voltage, the enable comparator then disables the device turning off the NMOS switch and reducing the Iq of the device to 40uA. The load current is then supplied solely by C_{OUT} indicated by the gradually decreasing slope at the output as shown in Figure 16. When the FB pin drops slightly below 1.237V, the enable comparator enables the device and begins the cycle described previously. The $\overline{SHDN}$ pin can be used to turn off the LM2703 and reduce the I_q to 0.01µA. In shutdown mode the output voltage will be a diode drop lower than the input voltage.

APPLICATION INFORMATION

INDUCTOR SELECTION

The appropriate inductor for a given application is calculated using the following equation:

$$L = \left(\frac{V_{OUT} - V_{IN(min)} + V_D}{I_{CL}}\right) T_{OFF} \quad (2)$$

where V_D is the schottky diode voltage, I_{CL} is the switch current limit found in the Typical Performance Characteristics section, and T_{OFF} is the switch off time. When using this equation be sure to use the minimum input voltage for the application, such as for battery powered applications. For the LM2703 constant-off time control scheme, the NMOS power switch is turned off when the current limit is reached. There is approximately a 200ns delay from the time the current limit is reached in the NMOS power switch and when the internal logic actually turns off the switch. During this 200ns delay, the peak inductor current will increase. This increase in inductor current demands a larger saturation current rating for the inductor. This saturation current can be approximated by the following equation:

$$I_{PK} = I_{CL} + \left(\frac{V_{IN(max)}}{L}\right) 200ns \quad (3)$$

Choosing inductors with low ESR decrease power losses and increase efficiency.

Care should be taken when choosing an inductor. For applications that require an input voltage that approaches the output voltage, such as when converting a Li-Ion battery voltage to 5V, the 400ns off time may not be enough time to discharge the energy in the inductor and transfer the energy to the output capacitor and load. This can cause a ramping effect in the inductor current waveform and an increased ripple on the output voltage. Using a smaller inductor will cause the I_{PK} to increase and will increase the output voltage ripple further. This can be solved by adding a 4.7pF capacitor across the R_{F1} feedback resistor (Figure 15) and slightly increasing the output capacitor. A smaller inductor can then be used to ensure proper discharge in the 400ns off time.

DIODE SELECTION

To maintain high efficiency, the average current rating of the schottky diode should be larger than the peak inductor current, I_{PK}. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown of the schottky diode larger than the output voltage.

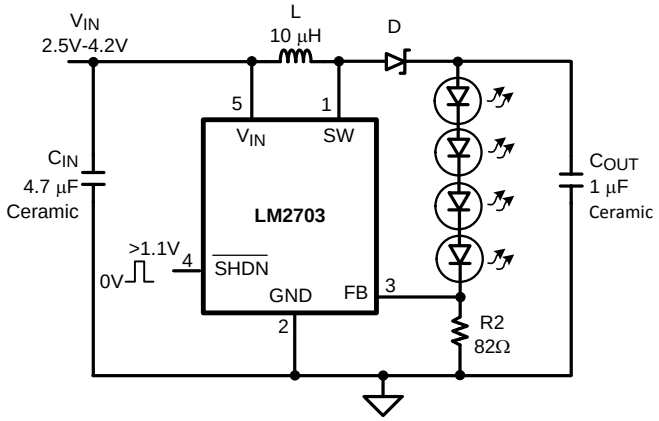
CAPACITOR SELECTION

Choose low ESR capacitors for the output to minimize output voltage ripple. Multilayer ceramic capacitors are the best choice. For most applications, a 1µF ceramic capacitor is sufficient. For some applications a reduction in output voltage ripple can be achieved by increasing the output capacitor.

Local bypassing for the input is needed on the LM2703. Multilayer ceramic capacitors are a good choice for this as well. A 4.7µF capacitor is sufficient for most applications. For additional bypassing, a 100nF ceramic capacitor can be used to shunt high frequency ripple on the input.

LAYOUT CONSIDERATIONS

The input bypass capacitor C_{IN}, as shown in Figure 1, must be placed close to the IC. This will reduce copper trace resistance which effects input voltage ripple of the IC. For additional input voltage filtering, a 100nF bypass capacitor can be placed in parallel with C_{IN} to shunt any high frequency noise to ground. The output capacitor, C_{OUT}, should also be placed close to the IC. Any copper trace connections for the Cout capacitor can increase the series resistance, which directly effects output voltage ripple. The feedback network, resistors R1 and R2, should be kept close to the FB pin to minimize copper trace connections that can inject noise into the system. The ground connection for the feedback resistor network should connect directly to an analog ground plane. The analog ground plane should tie directly to the GND pin. If no analog ground plane is available, the ground connection for the feedback network should tie directly to the GND pin. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency.



C_{IN}: Taiyo Yuden Ceramic
C_{OUT}: Taiyo Yuden Ceramic
L: Coilcraft DT1608C-103 or Murata
LQY33PN100M02 (low profile)
D: Motorola MBRM130LT3

Figure 17. White LED Application

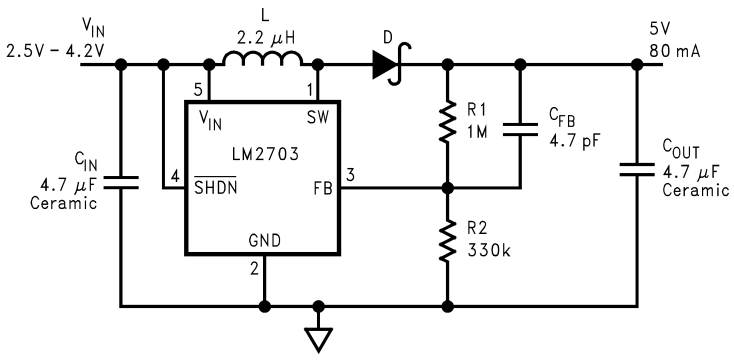


Figure 18. Li-Ion 5V Application

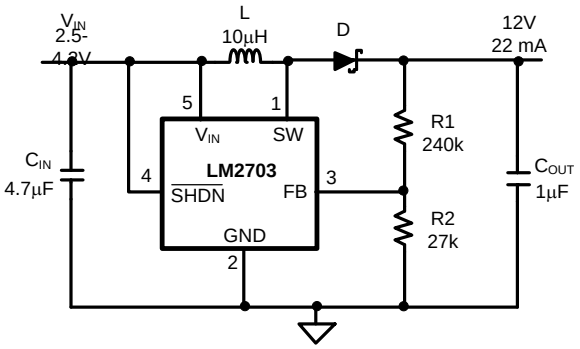


Figure 19. Li-Ion 12V Application

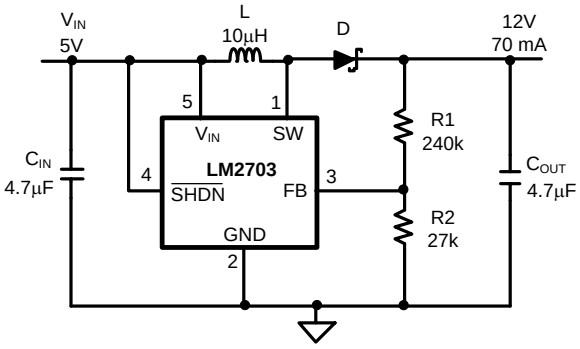


Figure 20. 5V to 12V Application

REVISION HISTORY

Changes from Revision E (May 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2703MF-ADJ	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	S48B	
LM2703MF-ADJ/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	S48B	Samples
LM2703MFX-ADJ/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	S48B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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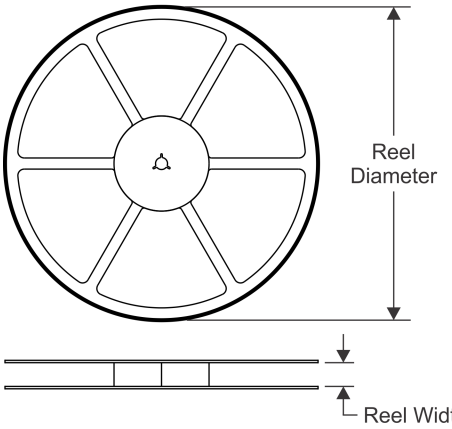
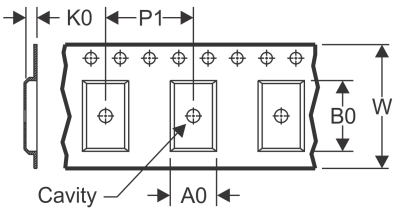
TAPE AND REEL INFORMATION

REEL DIMENSIONS

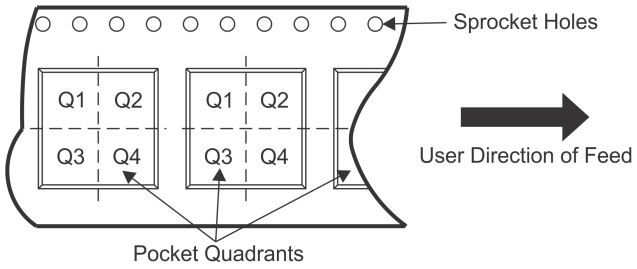


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

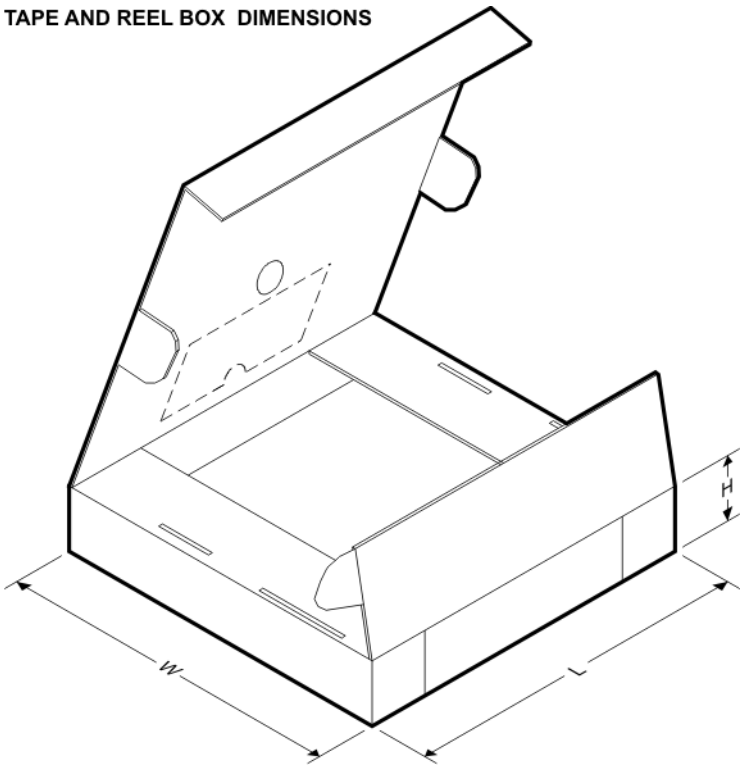
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2703MF-ADJ	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2703MF-ADJ/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2703MFX-ADJ/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

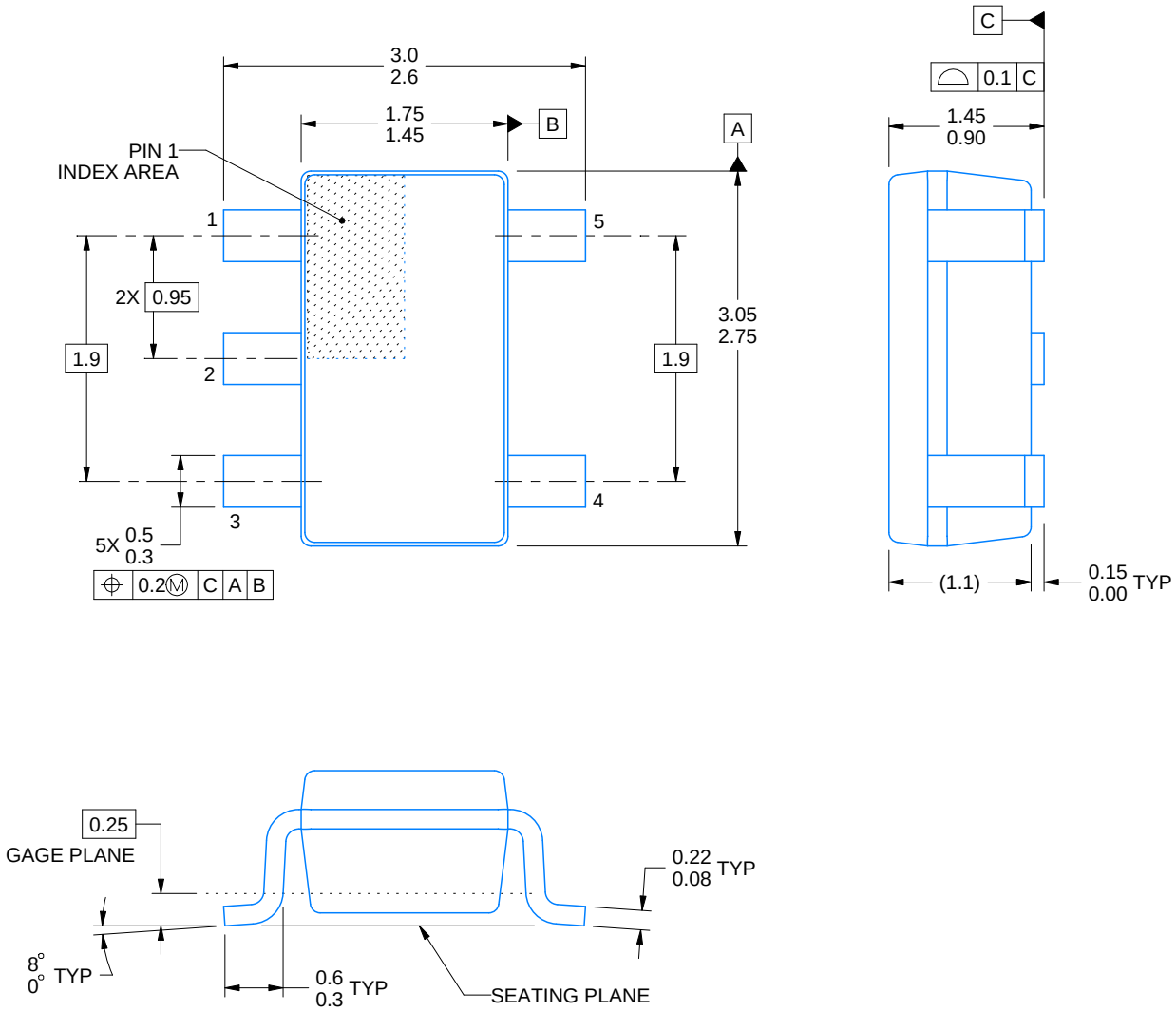
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2703MF-ADJ	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2703MF-ADJ/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2703MFX-ADJ/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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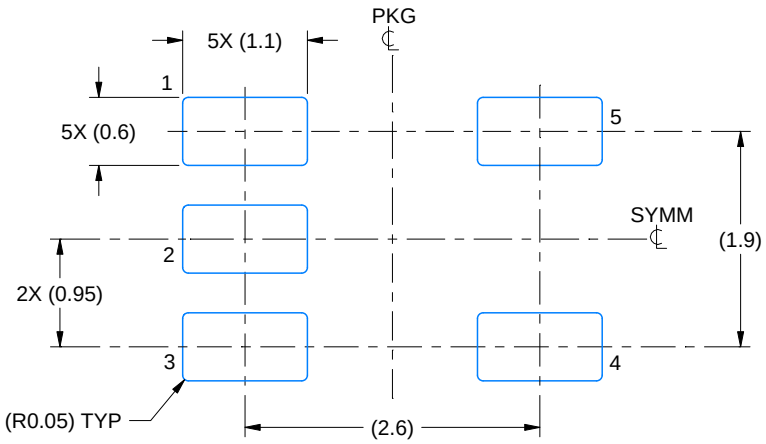
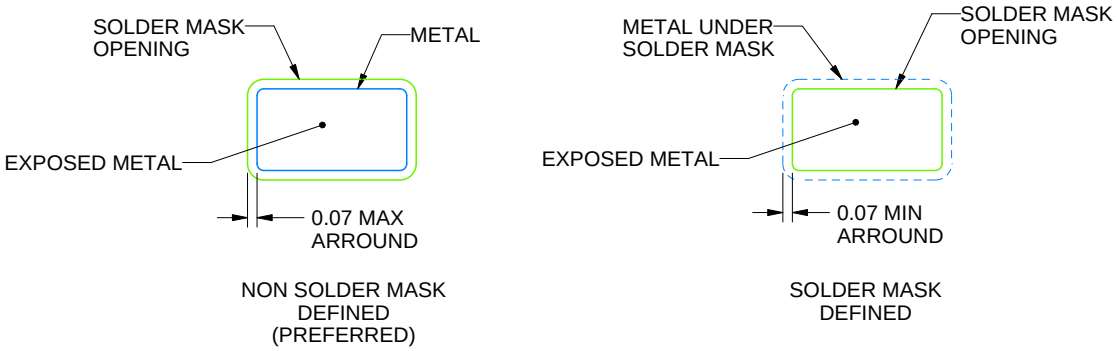
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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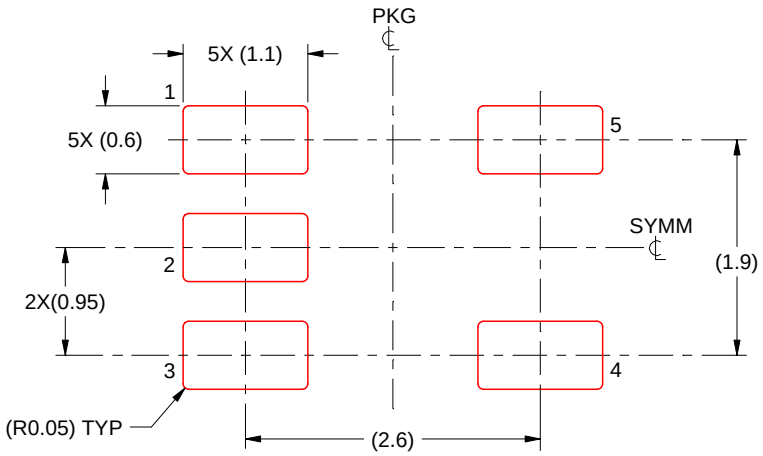
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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