AM5PA OTP Series

DATA SHEET v0.00

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Revision History

Rev	Date	Description	Page
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1. General Description

AM5PA Series is a 4-bit microprocessor with the advantages of low cost and high performance, containing 4-bit ALU, ROM, RAM, I/O ports, timers, interrupt, clock generator, audio synthesizer, PWM outputs, etc. The audio synthesizer contains one-voice channel. Features such as Watchdog Timer (WDT), Low Voltage Reset (LVR), and Infrared Ray Transmitter (IR) can reduce system costs and enhance reliability. Furthermore, with CMOS technology, SLEEP and SLOW functions can minimize power dissipation.

RISC MCU architecture is very easy to program and control. There are 44 instructions, most of which are executed only in a single cycle. The hardware audio decoder of AM5PA Series supports an ADPCM algorithm at a wide range of selectable bit rates, which can be used to select various modes of the audio filter to meet user's needs. In audio output stage, user can select direct-drive (PWM). Besides, AM5PA Series supports 6 levels low voltage detect (LVDT-X) and can detects external voltage.

2. Features

1) Single power supply can operate from 2.2 V to 5.5 V for AM5PA Series.
2) Program ROM can be up to 64K x 10-bit (0000H ~ FFFFH).
3) There are four bodies in AM5PA Series:

Product	Voice Duration (sec)	ROM Size (10-bit)	Clock Source	Audio Output	Volume Control	Noise Shaper	LVDT-X	PWMIO	IR	Reset
AM5PA340x	340	840K	RM	PWM	v	v	v	12	PRA[3]	PRA[0]
AM5PA180x	180	448K	RM	PWM	v	v	v	8	PRA[3]	PRA[0]
AM5PA084x	84	208K	RM	PWM	v	v	v	8	PRA[3]	PRA[0]
AM5PA041x	41	104K	RM	PWM	v	v	—	8	PRA[3]	PRA[0]

4) I/O Ports:

Product	I/O Pins	Port Name
AM5PA340x	16	PRA, PRB, PRC and PRD
AM5PA180x	12	PRA, PRB and PRC
AM5PA084x	12	PRA, PRB and PRC
AM5PA041x	8	PRA, PRB

5) Each pin of all I/O ports can be a wake-up pin when configured as input.

6) Support at most 4-level stack, which can be used as data SRAM for additional 16 x 4-bit space.

Product	Data SRAM	4-Level Stack or Used As Additional Data SRAM
AM5PA340x	200x4 (28H ~ EFH)	16x4 (F0H ~ FFH)
AM5PA180x	200x4 (28H ~ EFH)	16x4 (F0H ~ FFH)
AM5PA084x	200x4 (28H ~ EFH)	16x4 (F0H ~ FFH)
AM5PA041x	200x4 (28H ~ EFH)	16x4 (F0H ~ FFH)

7) Operation Mode

Provide Normal and Sleep Mode. When user executes SLEEP command, System clock will stop completely to save power. User can wake up the device from SLEEP Mode by changing data of input port.

8) Each I/O pin can be controlled by three I/O registers: **(Register Control)**

a) I/O direction register
b) I/O data register
c) I/O pull-low register

9) All four ports with large current output: **(Code Option)**

10) Each I/O pin can be set as one of the following states via mask option: ***(*Code *Option)***

a) Floating input
b) Input with pull low
c) Output
d) Software I/O (Register Control)

11) Low-cost OSC:

Provide ±1.5% internal resistance oscillator.

12) Built-in Infrared Ray (IR) carrier output: **(Code Option)**

There are built-in IR carrier output pins in AM5PA Series, which can be used as transmission pins for wireless transmission. User can set PRA[3] as the IR carrier pin. Through code option, the built-in IR carrier output can be switched to high or low.

13) Audio synthesizer:

The audio synthesizer has one voice channels. For the voice channel, AM5PA Series supports a selectable bit rate ADPCM algorithm with high-quality voice compression.

14) The hardware supports automatic loop function of playing sound files.

15) Audio Filter: **(Register Control)**

AM5PA Series has two hardware audio filters that can work together or separately to minimize unwanted audio noise.

16) Audio output method: **(Register Control)**

12-bit direct-drive output (PWM) is supported to provide best audio output quality.

17) 16-level global volume control: **(Register Control)**

There is a 16-level global volume control for direct-drive output (PWM).

18) 6-level Low voltage detector (LVDT-X): **(Register Control)**

AM5PA Series is support 6-level low voltage detect that can detect voltage : 2.4v, 2.7v, 3.3v, 3.6, 4.0v., 4.4v.

AM5PA Series LVDT-X function supports external power source detection.

Note: AM5PA041x doesn't support LVDT-X function.

19) 12-channel hardware PWMIO control: **(Register Control)**

There is a 512 levels resolution and the PWM carry frequency is 125Hz.

20) Built-in power noise filter:

When there's power noise, AM5PA series will activate the filter mechanism of noise automatically to avoid IC fails due to power noises.

21) Number of instructions: 44.

3. Block Diagram

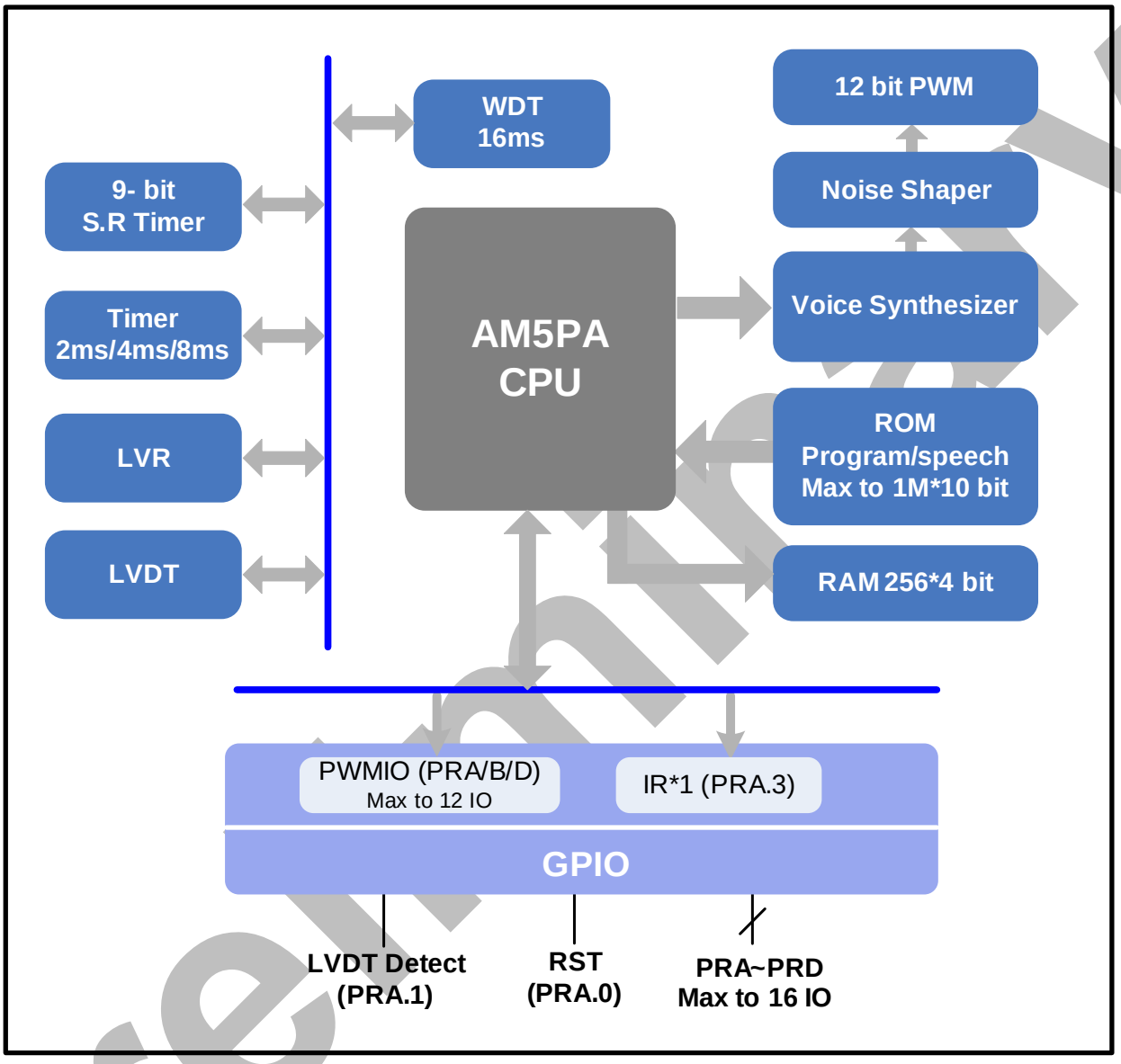


Figure 3.1 Block Dragram of AM5PA Series

4. Memory Organization

4.1 ROM

ROM memory is divided into six portions. The first portion 0x0 ~ 0xF is addressed for Reset Vector in normal mode. The second portion 0x10 ~ 0x1F is addressed for Interrupt Vector in normal mode. The third portion 0x20 ~ 0x3FF is reserved and not available for storing programs. The fourth portion 0x400 ~ 0x7FF is reserved for the system information. The fifth portion 0x800 ~ 0xFFFF is addressed for user's main program and voice data. The last portion 0x10000 ~ 0xXXFFF can be used to store voice data. Because JMP and CALL instructions can only reach an immediate address within a 16-bit wide page, the main program and ISR therefore can only be located in the 0x800 ~ 0xFFFF address range. In addition, except for Program Counter (PC), all pointers such as voice pointer (VPTR) and temporary register (TREG) can reach up to 0xXFFFF. FIGURE 3.1 shows the ROM map.

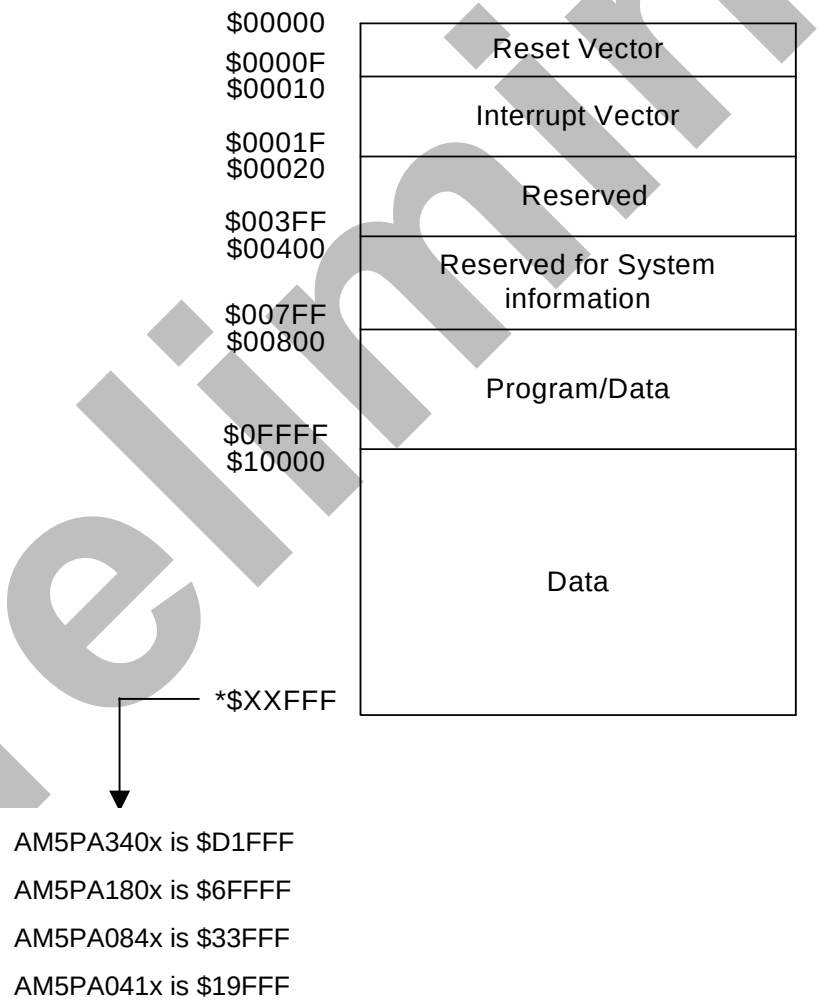


Figure 4.1 ROM Map of AM5PA Series

4.2 SRAM

SRAM is composed of Special Function Register (SFR), working SRAM, general SRAM and stack SRAM. Address 0x00 ~ 0x27 is reserved for SFR and address 0x28 ~ 0x3F is for the working SRAM that can be executed with logic or arithmetic instructions. Address 0x40~0x4F is the TREG backup and re-load SRAM which can be executed with the POP and RDPC instruction. Address 0x50~0xEF is the general SRAM and address 0xF0~0xFF is the stack SRAM, as shown in FIGURE 3.3. The stack SRAM is reserved for storing the current PC value when a CALL instruction or interrupt occurs. Furthermore, the SRAM of AM5PA Series also supports indirect addressing mode.

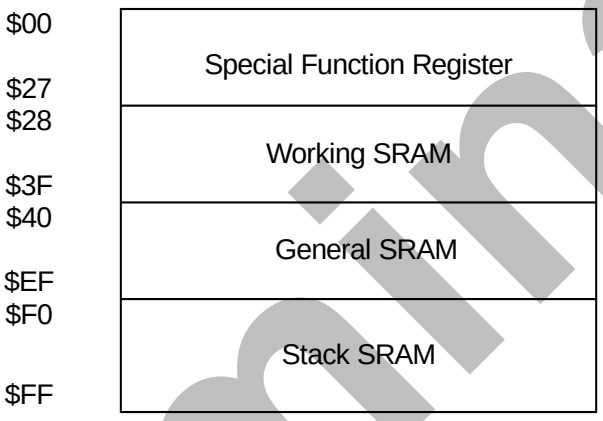


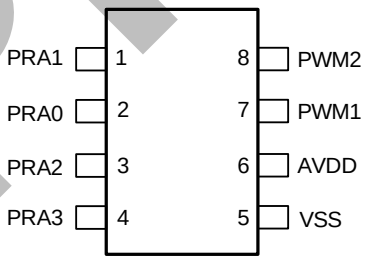
Figure 4.2 SRAM Map of AM5PA Series

5. Pin Configuration and Pin Description

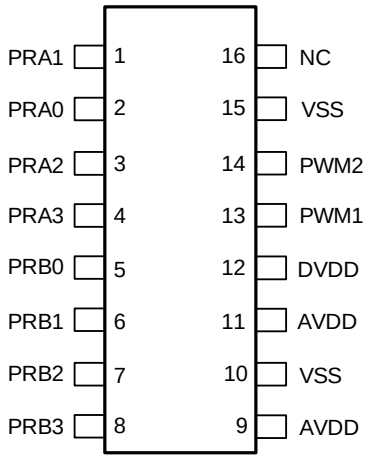
5.1 Pin Configuration

AM5PA series supported SOP8L, SOP16L, SOP20L, SSOP24L types. Difference IC Body package type is pin-to-pin compatible, PCB layout can be the same.

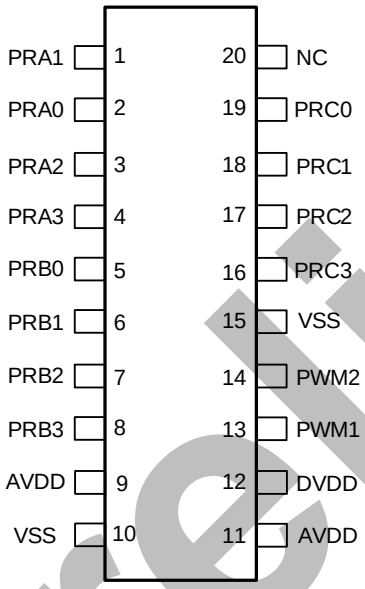
5.1.1 8 Pin – AM5PA340x/AM5PA180x/AM5PA084x/AM5PA041x SOPL



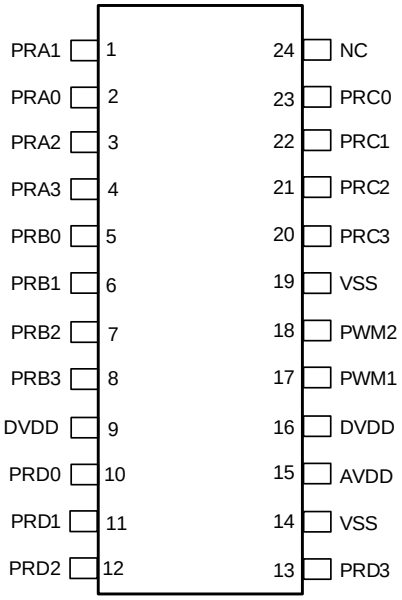
5.1.2 16 Pin – AM5PA340x/AM5PA180x/AM5PA084x/AM5PA041x SOPL



5.1.3 20 Pin – AM5PA340x/AM5PA180x/AM5PA084x SSOPL



5.1.4 24 Pin – AM5PA340x/AM5PA180x/AM5PA084x SSOP24L



5.2 Pin Description

Pin Name	Attr.	Description
IO PORT		
PRA[0] / Reset	I/O	Four I/O modes can be set via code option for each I/O pin: (1) Floating input mode, (2) Pull-low input mode, (3) Output mode, (4) Software IO mode. Buffer Output type. Or 2 kinds of output current: (1) Normal current, (2) Large current. **(Code Option)** Or selected as an external RESET pin with weak pull-low capability. **(Code Option)** Or selected as an PWMIO Output pin. **(Code Option)**
PRA[1]	I/O	Four I/O modes can be set via code option for each I/O pin: (1) Floating input mode, (2) Pull-low input mode, (3) Output mode, (4) Software IO mode. Buffer Output type. Or 2 kinds of output current: (1) Normal current, (2) Large current. **(Code Option)** Or selected as an PWMIO Output pin. **(Code Option)** Or LVDT-X detect pin **(Code Option)**
PRA[2]	I/O	Four I/O modes can be set via code option for each I/O pin: (1) Floating input mode, (2) Pull-low input mode, (3) Output mode, (4) Software IO mode. Buffer Output type. Or 2 kinds of output current: (1) Normal current, (2) Large current. **(Code Option)** Or selected as an PWMIO Output pin. **(Code Option)**

Pin Name	Attr.	Description
PRA[3] / IR	I/O	Four I/O modes can be set via code option for each I/O pin: (1) Floating input mode, (2) Pull-low input mode, (3) Output mode, (4) Software IO mode. Buffer Output type. Or 2 kinds of output current: (1) Normal current, (2) Large current. **(Code Option)** Or selected as an IR Carrier Output pin with programmable 38 KHz or 56KHz. **(Code Option)** Or selected as an PWMIO Output pin. **(Code Option)**
PRB0 ~ 3	I/O	Four I/O modes can be set via code option for each I/O pin: (1) Floating input mode, (2) Pull-low input mode, (3) Output mode, (4) Software IO mode. Buffer Output type. Or 2 kinds of output current: (1) Normal current, (2) Large current. **(Code Option)** Or selected as an PWMIO Output pin. **(Code Option)**
PRC0 ~ 3	I/O	Four I/O modes can be set via code option for each I/O pin: (1) Floating input mode, (2) Pull-low input mode, (3) Output mode, (4) Software IO mode. Buffer Output type. Or 2 kinds of output current: (1) Normal current, (2) Large current. **(Code Option)**
PRD0 ~ 3	I/O	Four I/O modes can be set via code option for each I/O pin: (1) Floating input mode, (2) Pull-low input mode, (3) Output mode, (4) Software IO mode. Buffer Output type. Or 2 kinds of output current: (1) Normal current, (2) Large current. **(Code Option)** Or selected as an PWMIO Output pin. **(Code Option)**
Audio PAD		
PWM1	O	PWM1 output.
PWM2	O	PWM2 output.
POWER PAD		
AVDD	Power	Positive power supply for analog portion
DVDD	Power	Positive power supply for digital portion
VSS	Power	Ground Potential.

6. Electrical Characteristics

The electrical characteristics of AM5PA Series are given in the following tables in which all the data are measured at room temperature. Various production processes among lots or different testing conditions may influence the data result.

6.1 Absolute Maximum Rating

SYMBOL	RATING	UNIT
V_{SS} ~ V_{DD}	-0.5 ~ +5.5	V
V_{in} (For all input)	V_{SS}-0.3 < V_{in} < V_{DD}+0.3	V
V_{out} (For all output)	V_{SS} < V_{out} < V_{DD}	V
T_{op} (Operating)	-25 ~ +85	℃
T_{st} (Storage)	-25 ~ +85	℃

6.2 DC Characteristics

SYMBOL	PARAMETER		VDD	MIN.	TYP.	MAX.	UNIT	CONDITION
V_{DD}	Operating Voltage			2.2	3	5.5	V	2 MHz
I_{SB}	Supply Current	Halt	3			1	uA	SLEEP Mode
			4.5			2		
I_{op}		Operating	3		4.4		mA	2 MHz, RM, PWM on, No Loading
			4.5		6.4			
V_{IH}	Input High Voltage			0.7V_{DD}		V_{DD}	V	
V_{IL}	Input Low Voltage			V_{SS}		0.3V_{DD}	V	
I_{IH}	Input Current (Internal weak pull-low)		3		3.3		uA	V_{il} = 0 V
			4.5		8.6			
I_{OH}	Output High Current (Normal Current)		3		6.42		mA	V_{oh} = 2.6 V
			4.5		15.36			V_{oh} = 3.7 V
I_{OH}	Output High Current (Large Current)		3		10.22			V_{oh} = 2.6 V
			4.5		24.71			V_{oh} = 3.7 V
I_{ol}	Output Low Current (Normal Current)		3		7.84			V_{ol} = 0.4 V
			4.5		16.77			V_{ol} = 0.8 V
I_{ol}	Output Low Current (Large Current)		3		19.85			V_{ol} = 0.4 V
			4.5		42.06			V_{ol} = 0.8 V

SYMBOL	PARAMETER	VDD	MIN.	TYP.	MAX.	UNIT	CONDITION
dF/F	Frequency Stability	3.4		±3%		%	$\frac{F(V)}{F(3)}$, 2.2<V<3.4
dF/F		5.1		±3%		%	$\frac{F(V)}{F(4.5)}$, 2.7<V<5.1
dF/F	F_{osc} Variation	3	1.97	2	2.03	MHz	2M ± 1.5%
		4.5					

Note：Ambient temperature is 25℃. Alpha will keep user updated when the temperature setting is changed.

7. IO Port Share Pin List

7.1 AM5PA041x

Port / Funciton	PRA				PRB			
	0	1	2	3	0	1	2	3
VPP	V							
Reset	V							
IR				V				
PWMIO	V	V	V	V	V	V	V	V
Large Current		V	V	V	V	V	V	V

7.2 AM5PA084x/AM5PA180x

Port / Funciton	PRA				PRB				PRC			
	0	1	2	3	0	1	2	3	0	1	2	3
VPP	V											
Reset	V											
IR				V								
PWMIO	V	V	V	V	V	V	V	V				
Large Current		V	V	V	V	V	V	V	V	V	V	V
LVDT-X		V										

7.3 AM5PA340x

Port / Funciton	PRA				PRB				PRC				PRD			
	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
VPP	V															
Reset	V															
IR				V												
PWMIO	V	V	V	V	V	V	V	V					V	V	V	V
Large Current		V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
LVDT		V														