TPS56x219A 采用 8 引脚 SOT-23 封装的 4.5V 至 17V 输入、2A/3A 同步降压稳压器

1 特性

- TPS562219A：集成有 133mΩ 和 80mΩ 场效应晶体管 (FET) 的 2A 转换器
- TPS563219A：集成有 68mΩ 和 39mΩ FET 的 3A 转换器
- D-CAP2™模式控制，此模式控制具有 650kHz 的开关频率
- 输入电压范围：4.5V 至 17V
- 输出电压范围：0.76V 至 7V
- 650kHz 开关频率
- 低关断电流（低于 10μA）
- 1% 反馈电压精度 (25°C)
- 从预偏置输出电压中启动
- 逐周期过流限制
- 断续模式欠压保护
- 非锁存过压保护 (OVP)，欠压闭锁 (UVLO) 和热关断 (TSD) 保护
- 可调软启动
- 电源正常输出

2 应用

- 数字电视电源
- 高清 Blu-ray Disc™播放器
- 网络家庭终端设备
- 数字机顶盒 (STB)

3 说明

TPS562219A 和 TPS563219A 是采用 8 引脚 SOT-23 封装的简单易用型 2A/3A 同步降压转换器。

两款器件均经过优化，最大限度地减少了运行所需的外部组件并且可以实现低待机电流。

这些开关模式电源 (SMPS) 器件采用 D-CAP2™ 模式控制，从而提供快速瞬态响应，并且在无需外部补偿组件的情况下支持诸如高分子聚合物等低等效串联电阻 (ESR) 输出电容器以及超低 ESR 陶瓷电容器。

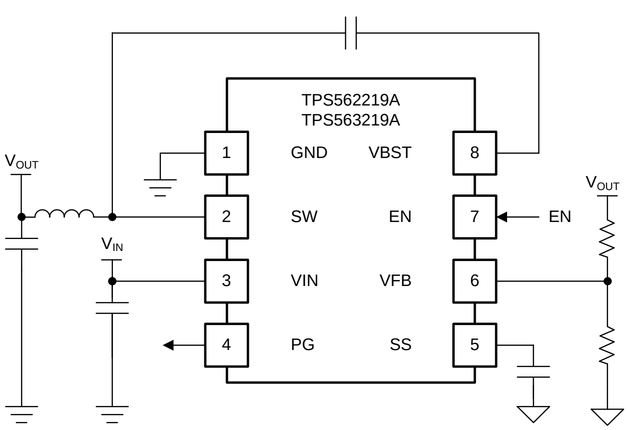
这些器件始终在连续传导模式下运行，与非连续传导模式相比，该模式可降低轻负载条件下的输出纹波电压。TPS562219A 和 TPS563219A 采用 8 引脚 1.6mm × 2.9mm SOT (DDF) 封装，额定环境温度范围为 –40°C 至 85°C。

器件信息(1)

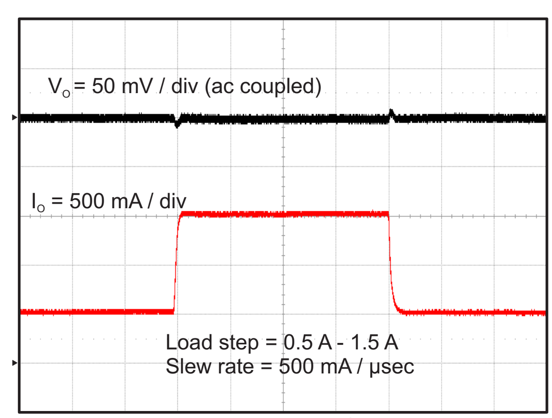
器件型号	封装	封装尺寸（标称值）
TPS562219A	SOT (8)	1.60mm x 2.90mm
TPS563219A		

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

简化原理图



TPS562219A 瞬态响应



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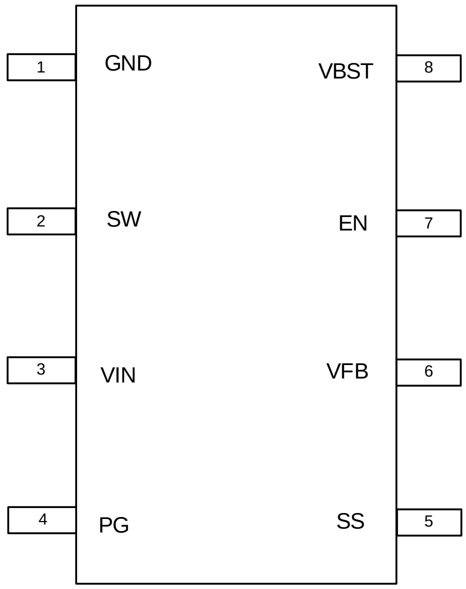
4 修订历史记录

日期	修订版本	注释
2016 年 11 月	*	首次发布。

5 Pin Configuration and Functions

DDF Package
8 Pin SOT
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
GND	1	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	Switch node connection between high-side NFET and low-side NFET.
VIN	3	Input voltage supply pin. The drain terminal of high-side power NFET.
PG	4	Power good open drain output
SS	5	Soft-start control. An external capacitor should be connected to GND.
VFB	6	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	7	Enable input control. Active high and must be pulled up to enable the device.
VBST	8	Supply input for the high-side NFET gate drive circuit. Connect 0.1 µF capacitor between VBST and SW pins.

6 Specifications

6.1 Absolute Maximum Ratings

T_J = -40°C to 150°C (unless otherwise noted) [1]

		MIN	MAX	UNIT
Input voltage range	VIN, EN	–0.3	19	V
	VBST	–0.3	25	V
	VBST (10 ns transient)	–0.3	27.5	V
	VBST (vs SW)	–0.3	6.5	V
	VFB, PG	–0.3	6.5	V
	SS	–0.3	5.5	V
	SW	–2	19	V
	SW (10 ns transient)	–3.5	21	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 [2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

T_J = –40°C to 150°C (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply input voltage range		4.5	17	V
V_I	Input voltage range	VBST	–0.1	23	V
		VBST (10 ns transient)	–0.1	26	
		VBST(vs SW)	–0.1	6	
		EN	–0.1	17	
		VFB, PG	–0.1	5.5	
		SS	–0.1	5	
		SW	–1.8	17	
		SW (10 ns transient)	–3.5	20	
T_A	Operating free-air temperature		–40	85	°C

6.4 Thermal Information

THERMAL METRIC [1]		TPS562219A	TPS563219A	UNIT
		DDF (SOT)		
		8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.1	87.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.1	41.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.9	14.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.6	4.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.8	14.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_J = –40°C to 150°C, VIN = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN}	Operating – non-switching supply current	V_{IN} current, T_A = 25°C, EN = 5 V, V_{FB} = 0.8 V		650	900	µA
I_{VINSDN}	Shutdown supply current	V_{IN} current, T_A = 25°C, EN = 0 V		3	10	µA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage	EN	1.6			V
V_{ENL}	EN low-level input voltage	EN			0.6	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V	225	450	900	kΩ
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V_{FBTH}	V_{FB} threshold voltage	T_A = 25°C, V_O = 1.05 V	757	765	773	mV
		T_A = 0°C to 85°C, V_O = 1.05 V (1)	753		777	mV
		T_A = -40°C to 85°C, V_O = 1.05 V (1)	751		779	mV
I_{VFB}	V_{FB} input current	V_{FB} = 0.8V, T_A = 25°C		0	±0.1	µA
MOSFET						
$R_{DS(on)h}$	High side switch resistance	T_A = 25°C, V_{BST} – SW = 5.5 V, TPS562219A		133		mΩ
		T_A = 25°C, V_{BST} – SW = 5.5 V, TPS563219A		68		mΩ
$R_{DS(on)l}$	Low side switch resistance	T_A = 25°C, TPS562219A		80		mΩ
		T_A = 25°C, TPS563219A		39		mΩ
CURRENT LIMIT						
I_{OCL}	Current limit (1)	DC current, V_{OUT} = 1.05 V, L1 = 2.2 µH, TPS562219A	2.5	3.2	4.3	A
		DC current, V_{OUT} = 1.05 V, L1 = 1.5 µH, TPS563219A	3.5	4.2	5.3	A
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold (1)	Shutdown temperature		155		°C
		Hysteresis		35		°C
SOFT START						
I_{SS}	SS charge current	V_{SS} = 1.2 V	4.2	6	7.8	µA
POWER GOOD						
V_{THPG}	PG threshold	V_{FB} rising (Good)	85%	90%	95%	
		V_{FB} falling (Fault)		85%		
IPG	PG sink current	PG = 0.5 V	0.5	1		mA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP threshold	OVP Detect		125%x Vfbth		
V_{UVP}	Output UVP threshold	Hiccup detect		65%x Vfbth		
$t_{HiccupOn}$	Hiccup Power On Time			1		cycle
$t_{HiccupOff}$	Hiccup Power Off Time			7		cycle
UVLO						
UVLO	UVLO threshold	Wake up VIN voltage	3.45	3.75	4.05	V
		Hysteresis VIN voltage	0.13	0.32	0.55	V

(1) Not production tested.

6.6 Timing Requirements

			MIN	TYP	MAX	UNIT
ON-TIME TIMER CONTROL						
t_{ON}	On time	V_{IN} = 12 V, V_O = 1.05 V		150		ns
$t_{OFF(MIN)}$	Minimum off time	T_A = 25°C, V_{FB} = 0.5 V		260	310	ns

6.7 Typical Characteristics

6.7.1 TPS562219A Characteristics

V_{IN} = 12V (unless otherwise noted)

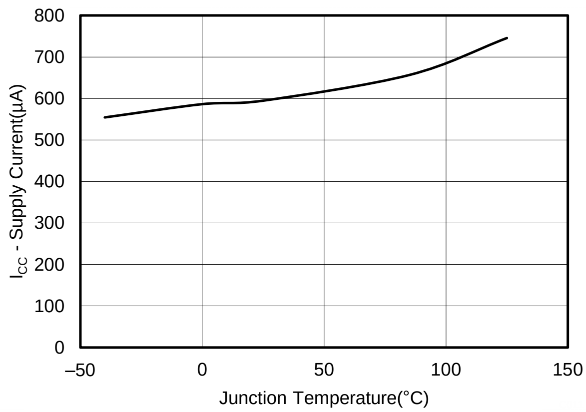


图 1. Supply Current vs Junction Temperature

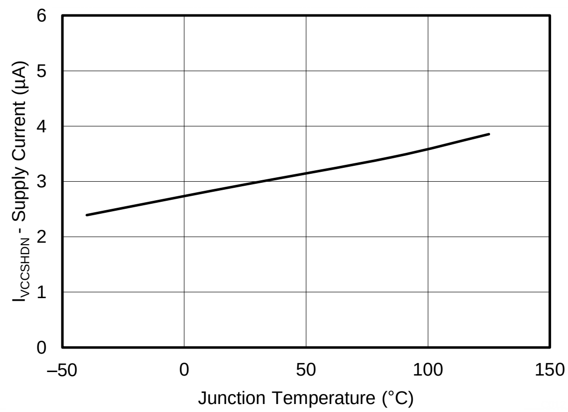


图 2. VIN Shutdown Current vs Junction Temperature

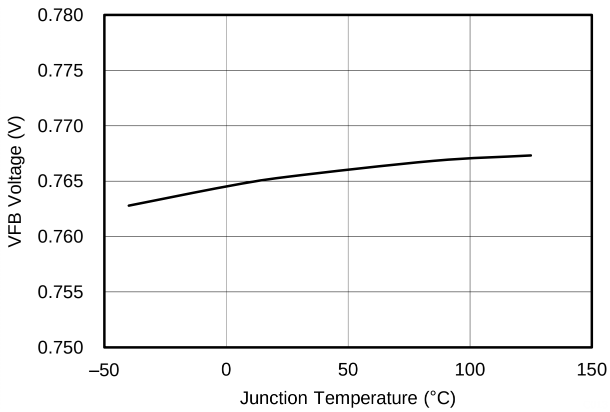


图 3. VFB Voltage vs Junction Temperature

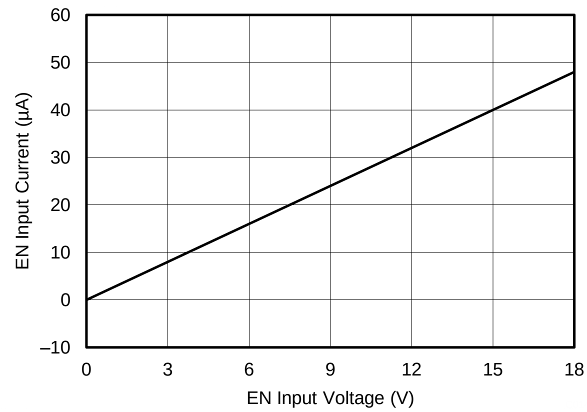


图 4. EN Current vs EN Voltage

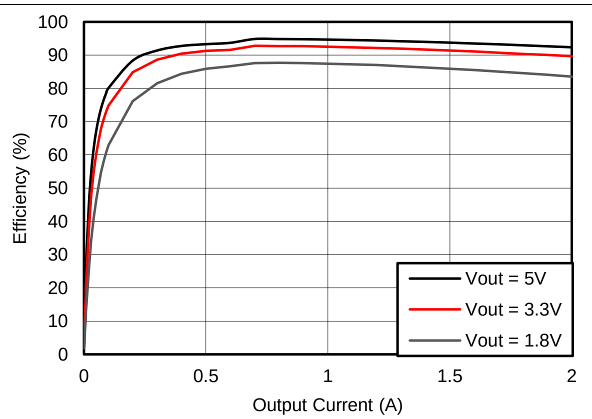


图 5. Efficiency vs Output Current

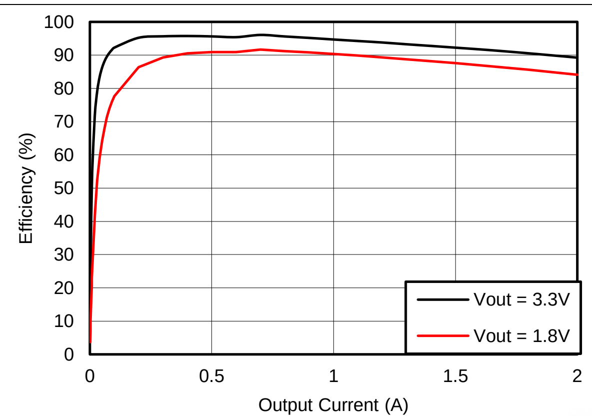


图 6. Efficiency vs Output Current (V_I= 5V)

TPS562219A Characteristics (接下页)

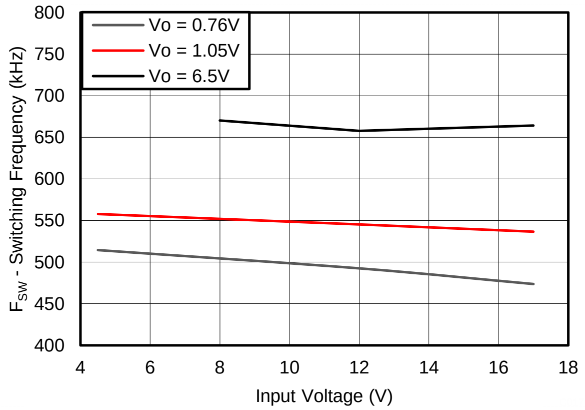


图 7. Switching Frequency vs Input Voltage

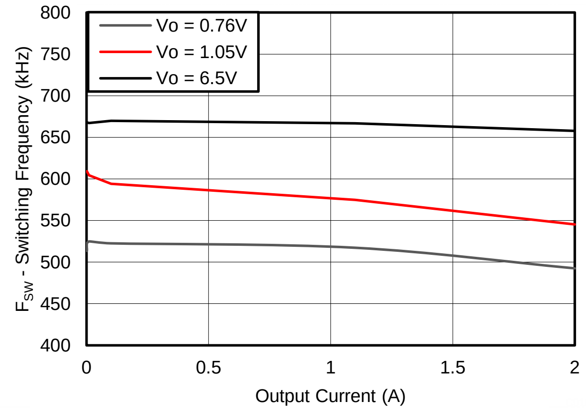


图 8. Switching Frequency vs Output Current

6.7.2 TPS563219A Characteristics

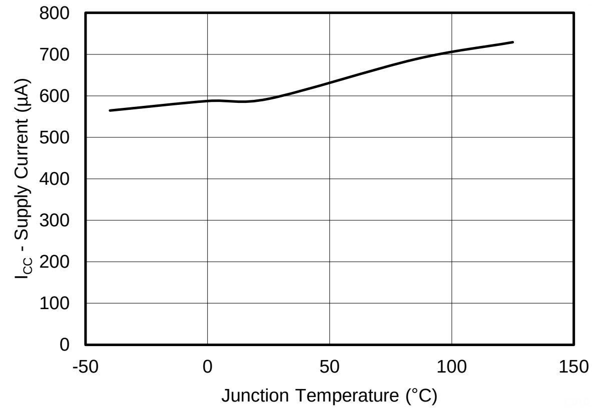


图 9. Supply Current vs Junction Temperature

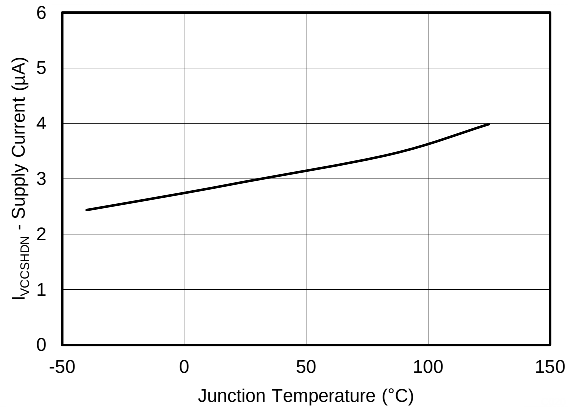


图 10. VIN Shutdown Current vs Junction Temperature

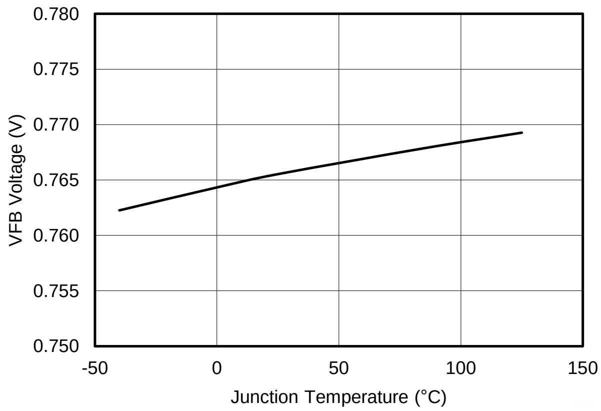


图 11. VFB Voltage vs Junction Temperature

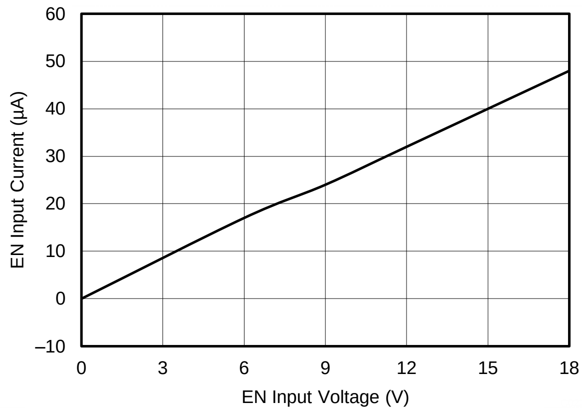


图 12. EN Current vs EN Voltage

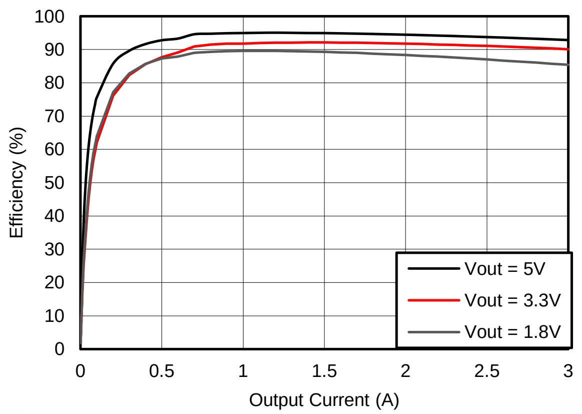


图 13. Efficiency vs Output Current

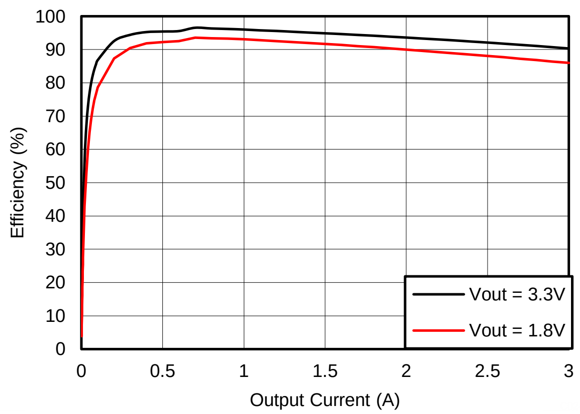


图 14. Efficiency vs Output Current (V_I = 5V)

TPS563219A Characteristics (接下页)

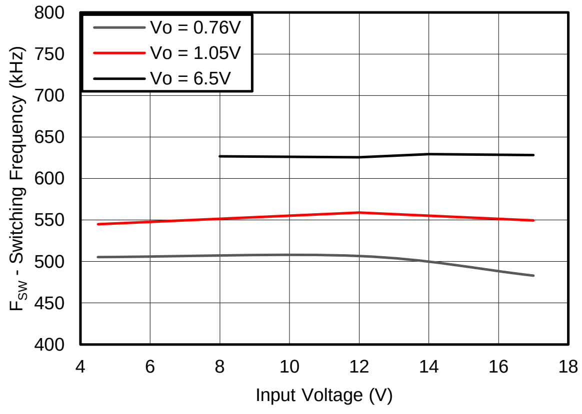


图 15. Switching Frequency vs Input Voltage

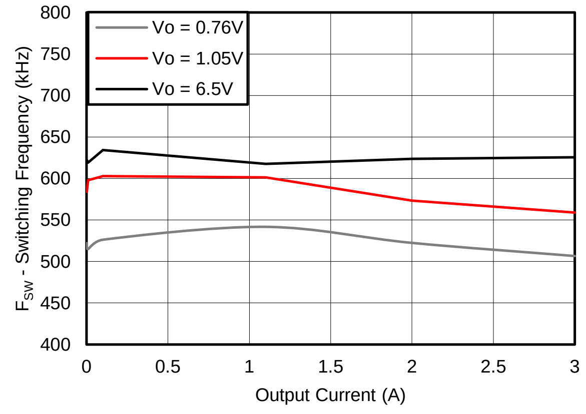


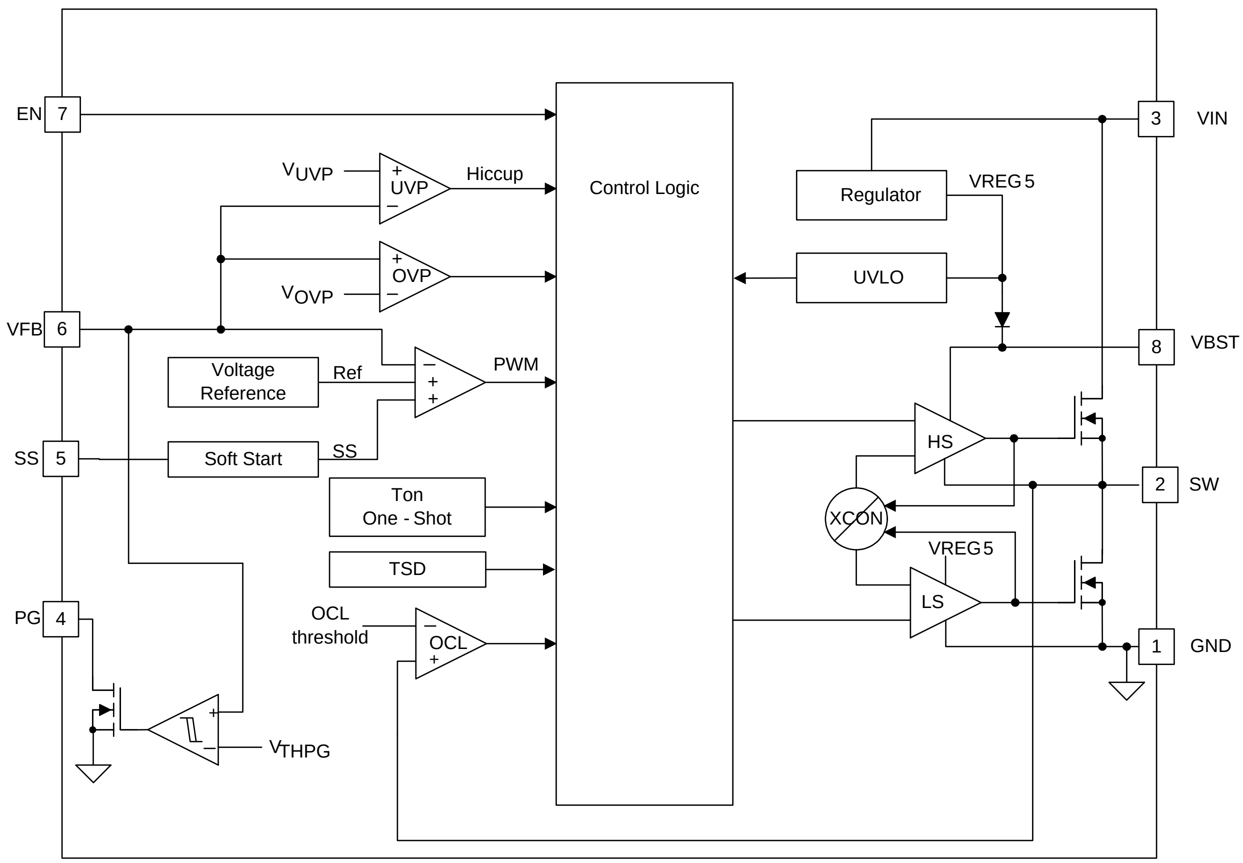
图 16. Switching Frequency vs Output Current

7 Detailed Description

7.1 Overview

The TPS562219A and TPS563219A are 2-A, 3-A synchronous step-down converters. The proprietary D-CAP2™ mode control supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP2™ mode control can reduce the output capacitance required to meet a specific level of performance.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 The Adaptive On-Time Control and PWM Operation

The main control loop of the TPS562219A and TPS563219A are adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. The D-CAP2™ mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot duration is set proportional to the converter input voltage, VIN, and inversely proportional to the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

Feature Description (接下页)

7.3.2 Soft Start and Pre-Biased Soft Start

The TPS562219A and TPS563219A have adjustable soft-start. When the EN pin becomes high, the SS charge current (I_{SS}) begins charging the capacitor which is connected from the SS pin to GND (C_{SS}). Smooth control of the output voltage is maintained during start up. The equation for the soft start time, T_{SS} is shown in 公式 1.

$$Tss(ms) = \frac{Css \times V_{FBTH} \times 0.86}{Iss} \quad (1)$$

where V_{FBTH} is 0.765 V and Iss is 6 µA.

If the output capacitor is pre-biased at startup, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.3 Power Good

The power good output, PG is an open drain output. The power good function becomes active after 1.7 times soft-start time. When the output voltage becomes within –10% of the target value, internal comparators detect power good state and the power good signal becomes high. If the feedback voltage goes under 15% of the target value, the power good signal becomes low.

7.3.4 Current Protection

The output over-current limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN}, V_{OUT}, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL threshold is returned to the higher value.

There are some important considerations for this type of over-current protection. The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the VFB voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device will shut down after the UVP delay time (typically 14 µs) and re-start after the hiccup time.

When the over current condition is removed, the output voltage returns to the regulated value.

7.3.5 Over Voltage Protection

TPS562219A and TPS563219A detect over voltage condition by monitoring the feedback voltage (VFB). When the feedback voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high and the high-side MOSFET turns off. This function is non-latch operation.

7.3.6 UVLO Protection

Under voltage lock out protection (UVLO) monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.7 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 155°C), the device is shut off. This is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS562219A and TPS563219A can operate in their normal switching modes. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM, the TPS562219A and TPS563219A operate at a quasi-fixed frequency of 650 kHz.

7.4.2 Forced CCM Operation

When the TPS562209 and TPS563209 are in the normal CCM operating mode and the switch current falls below 0 A, the TPS562219A and TPS563219A begin operating in forced CCM.

7.4.3 Standby Operation

When the TPS562219A and TPS563219A are operating in either normal CCM or forced CCM, they may be placed in standby by asserting the EN pin low.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS562219A and TPS563219A are typically used as step down converters, which convert a voltage from 4.5 V - 17 V to a lower voltage. Webench software is available to aid in the design and analysis of circuits.

8.2 Typical Application

8.2.1 Typical Application, TPS562219A

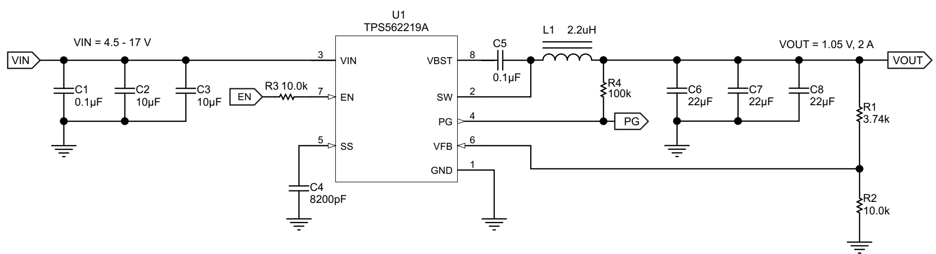


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图 17. TPS562219A 1.05V/2A Reference Design

8.2.1.1 Design Requirements

For this design example, use the parameters shown in 表 1.

表 1. Design Parameters

PARAMETER	VALUES
Input voltage range	4.5 V to 17 V
Output voltage	1.05 V
Output current	2 A
Output voltage ripple	20 mVpp

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using 公式 2 to calculate V_{OUT}.

To improve efficiency at light loads consider using larger value resistors, too high of resistance are more susceptible to noise and voltage errors from the VFB input current are more noticeable.

$$V_{OUT} = 0.765 \times \left(1 + \frac{R1}{R2}\right) \tag{2}$$

8.2.1.2.2 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \tag{3}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of 公式 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in 表 2.

表 2. TPS562219A Recommended Component Values

Output Voltage (V)	R2 (kΩ)	R3 (kΩ)	L1(uH)			C6 + C7 + C8(μF)
			MIN	TYP	MAX	
1	3.09	10.0	1.5	2.2	4.7	20 - 68
1.05	3.74	10.0	1.5	2.2	4.7	20 - 68
1.2	5.76	10.0	1.5	2.2	4.7	20 - 68
1.5	9.53	10.0	1.5	2.2	4.7	20 - 68
1.8	13.7	10.0	1.5	2.2	4.7	20 - 68
2.5	22.6	10.0	2.2	3.3	4.7	20 - 68
3.3	33.2	10.0	2.2	3.3	4.7	20 - 68
5	54.9	10.0	3.3	4.7	4.7	20 - 68
6.5	75	10.0	3.3	4.7	4.7	20 - 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using 公式 4, 公式 5 and 公式 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

Use 650 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of 公式 5 and the RMS current of 公式 6.

$$I l_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (4)$$

$$I l_{PEAK} = I_O + \frac{I l_{P-P}}{2} \quad (5)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I l_{P-P}^2} \quad (6)$$

For this design example, the calculated peak current is 2.34 A and the calculated RMS current is 2.01 A. The inductor used is a TDK CLF7045T-2R2N with a peak current rating of 5.5 A and an RMS current rating of 4.3 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS562219A and TPS563219A are intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 μF to 68 μF. Use 公式 7 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (7)$$

For this design two TDK C3216X5R0J226M 22μF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286A and each output capacitor is rated for 4A.

8.2.1.2.3 Input Capacitor Selection

The TPS562219A and TPS563219A require an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 μF is recommended for the decoupling capacitor. An additional 0.1 μF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

8.2.1.2.4 Bootstrap capacitor Selection

A 0.1µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

8.2.1.3 Application Curves

The following application curves were generated using the application circuit of 图 17.

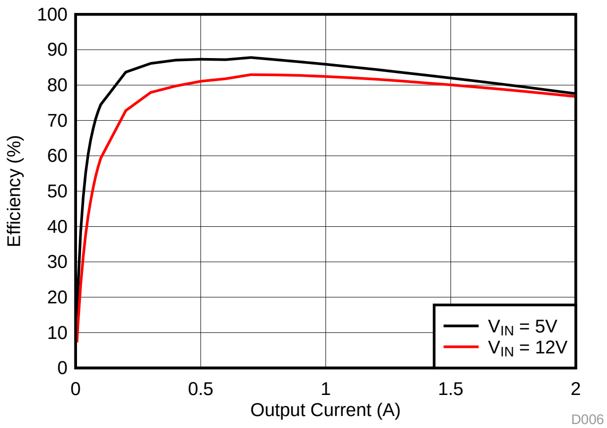


图 18. TPS562219A Efficiency

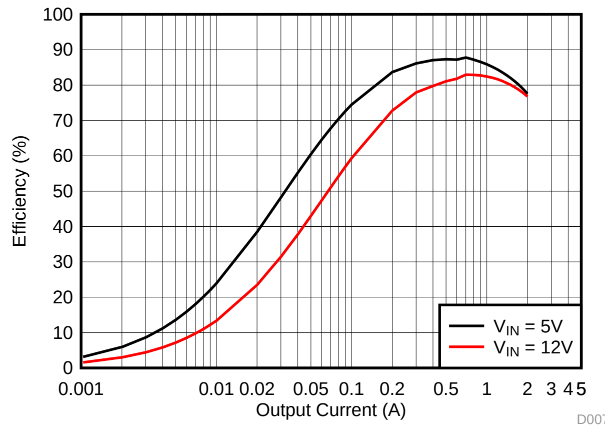


图 19. TPS562219A Light Load Efficiency

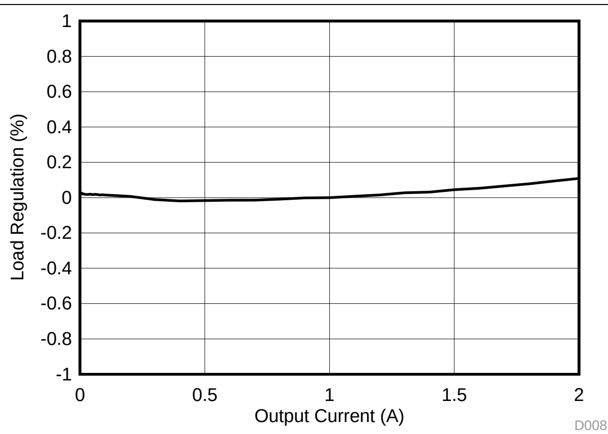


图 20. TPS562219A Load Regulation, V_I = 5 V

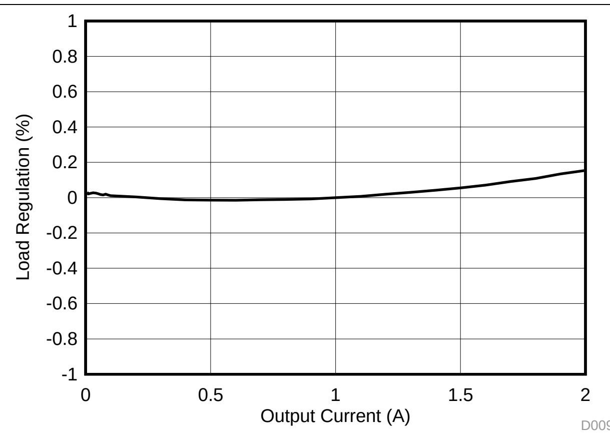


图 21. TPS562219A Load Regulation, V_I = 12 V

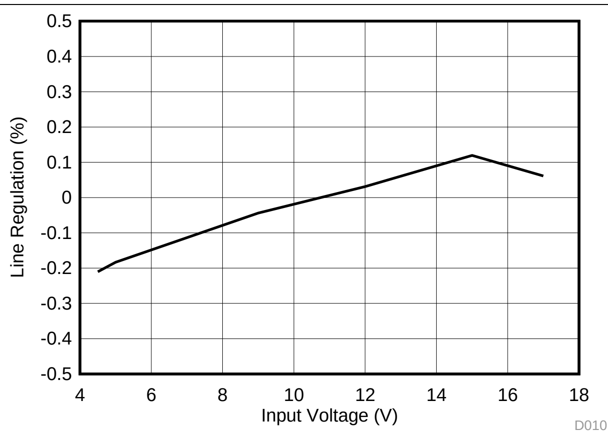


图 22. TPS562219A Line Regulation

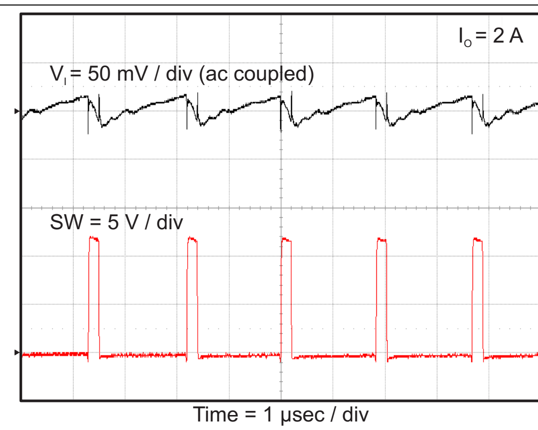


图 23. TPS562219A Input Voltage Ripple

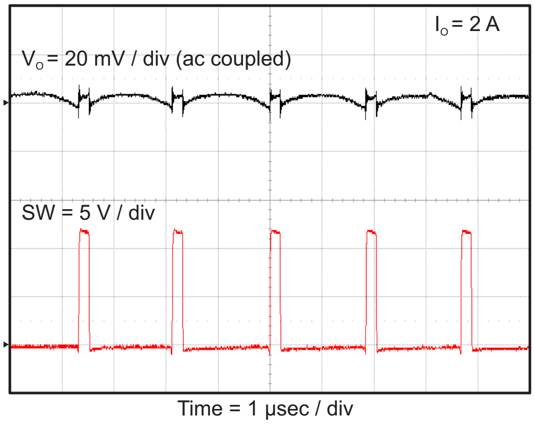


图 24. TPS562219A Output Voltage Ripple

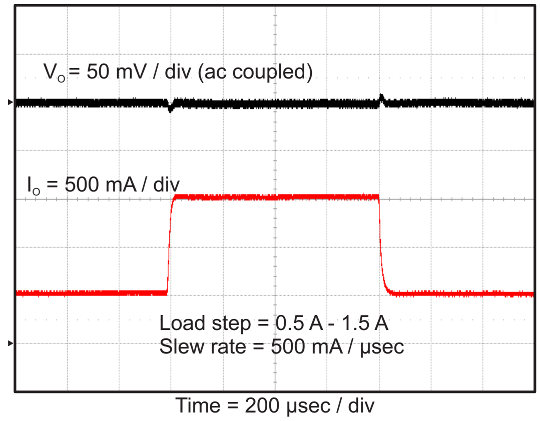


图 25. TPS562219A Transient Response

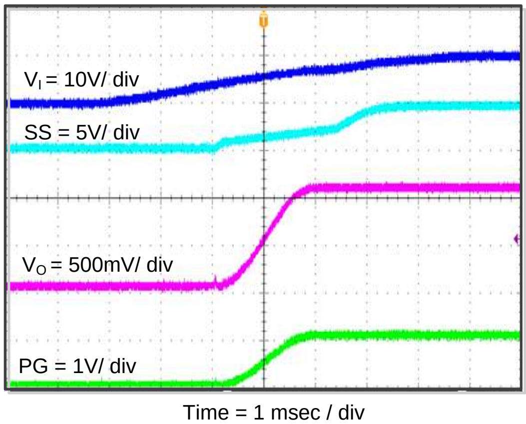


图 26. TPS562219A Start Up Relative To V_I

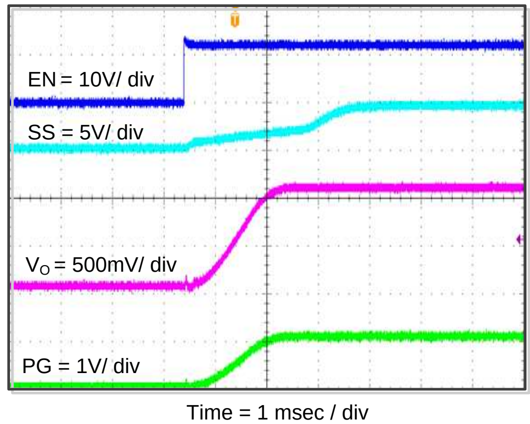


图 27. TPS562219A Start Up Relative To EN

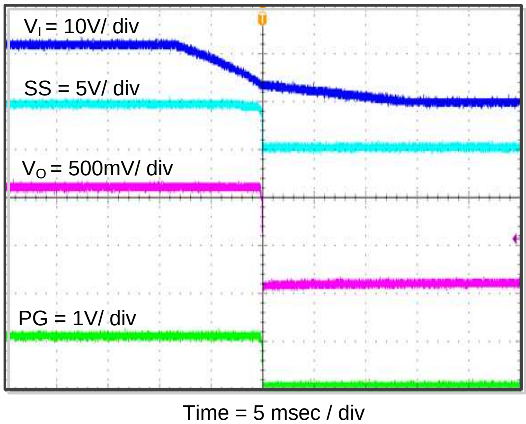


图 28. TPS562219A Shut Down Relative To V_I

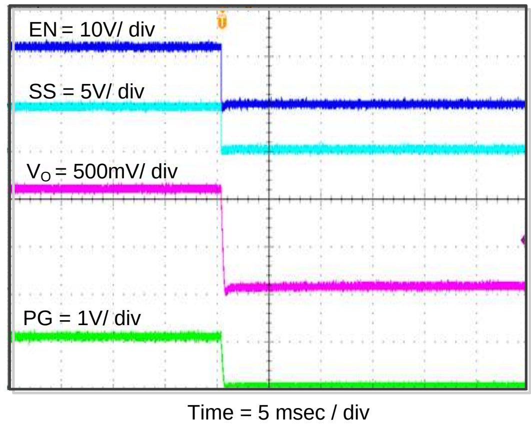


图 29. TPS562219A Shut Down Relative To EN

8.2.2 Typical Application, TPS563219A

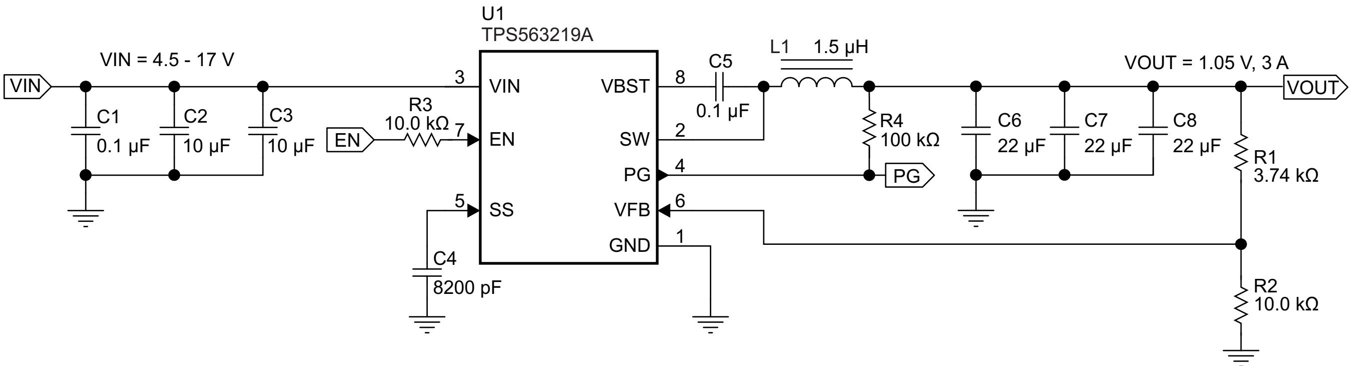


图 30. TPS563219A 1.05V/3A Reference Design

8.2.2.1 Design Requirements

For this design example, use the parameters shown in 表 3.

表 3. Design Parameters

PARAMETER	VALUE
Input voltage range	4.5 V to 17V
Output voltage	1.05V
Output current	3A
Output voltage ripple	20mVpp

8.2.2.2 Detailed Design Procedures

The detailed design procedure for TPS563219A is the same as for TPS562200 except for inductor selection.

8.2.2.2.1 Output Filter Selection

表 4. TPS563219A Recommended Component Values

Output Voltage (V)	R2 (kΩ)	R3 (kΩ)	L1 (µH)			C6 + C7 + C8 (µF)
			MIN	TYP	MAX	
1	3.09	10.0	1.0	1.5	4.7	20 - 68
1.05	3.74	10.0	1.0	1.5	4.7	20 - 68
1.2	5.76	10.0	1.0	1.5	4.7	20 - 68
1.5	9.53	10.0	1.0	1.5	4.7	20 - 68
1.8	13.7	10.0	1.5	2.2	4.7	20 - 68
2.5	22.6	10.0	1.5	2.2	4.7	20 - 68
3.3	33.2	10.0	1.5	2.2	4.7	20 - 68
5	54.9	10.0	2.2	3.3	4.7	20 - 68
6.5	75	10.0	2.2	3.3	4.7	20 - 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using 公式 8, 公式 9 and 公式 10. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for f_{SW}.

Use 650 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of 公式 9 and the RMS current of 公式 10.

$$Il_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (8)$$

$$II_{PEAK} = I_O + \frac{II_{P-P}}{2} \quad (9)$$

$$I_{LO(RMS)} = \sqrt{I_O{}^2 + \frac{1}{12} II_{P-P}{}^2} \quad (10)$$

For this design example, the calculated peak current is 3.505 A and the calculated RMS current is 3.014 A. The inductor used is a TDK CLF7045T-1R5N with a peak current rating of 7.3-A and an RMS current rating of 4.9-A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS563209 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 μF to 68 μF. Use 公式 6 to determine the required RMS current rating for the output capacitor. For this design, three TDK C3216X5R0J226M 22 μF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.292 A and each output capacitor is rated for 4 A.

8.2.2.3 Application Curves

The following application curves were generated using the application circuit of 图 30.

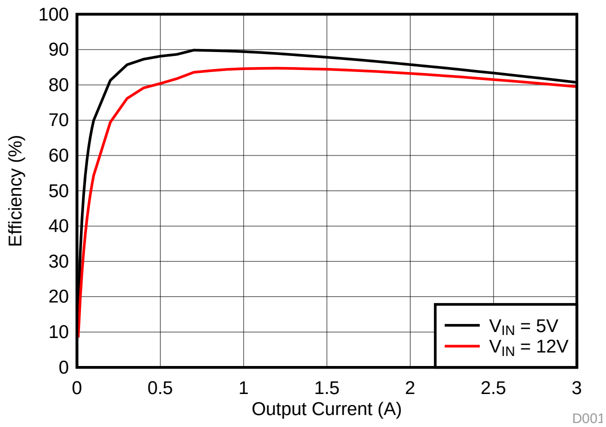


图 31. TPS563219A Efficiency

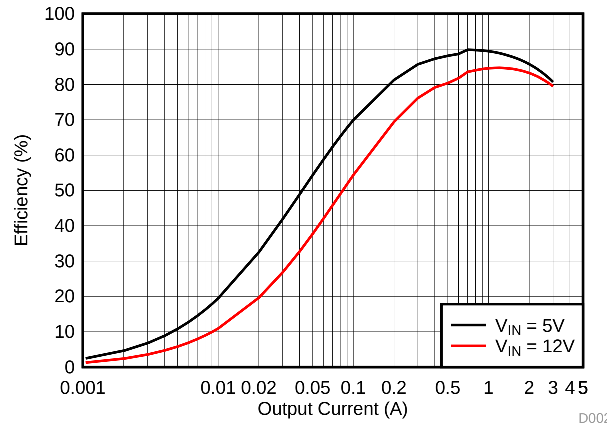


图 32. TPS563219A Light Load Efficiency

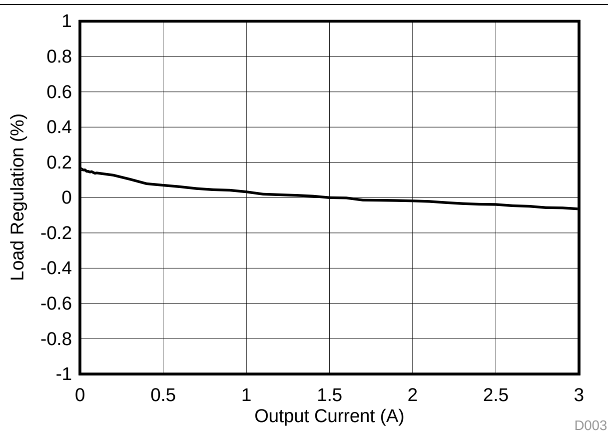


图 33. TPS563219A Load Regulation, V_I = 5 V

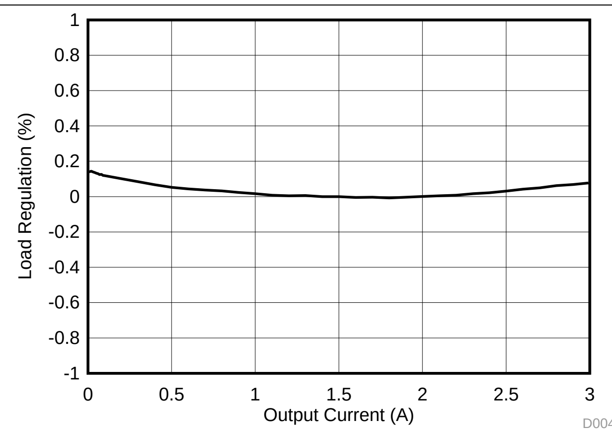


图 34. TPS563219A Load Regulation, V_I = 12 V

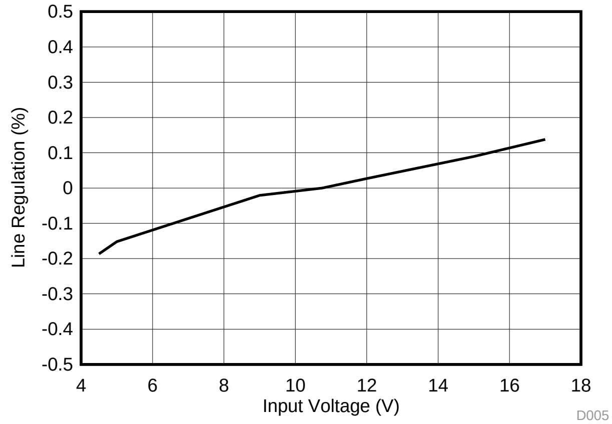


图 35. TPS563219A Line Regulation

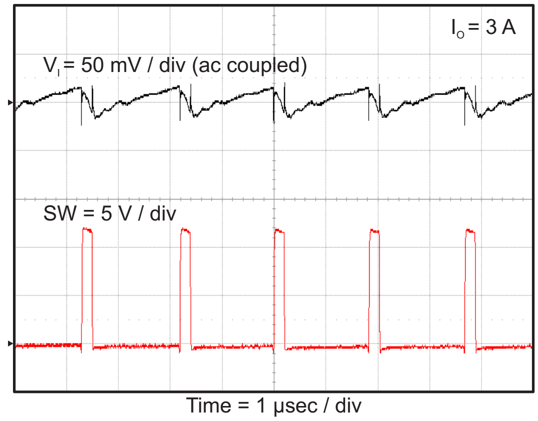


图 36. TPS563219A Input Voltage Ripple

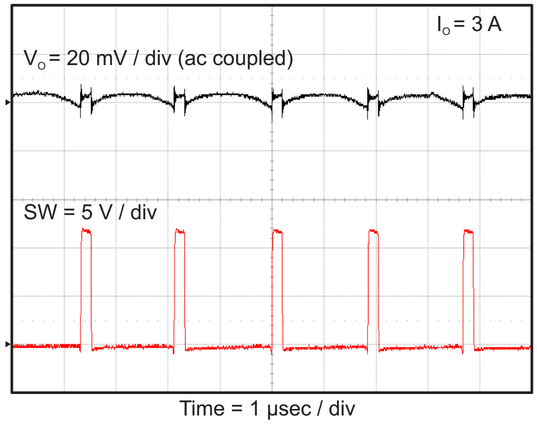


图 37. TPS563219A Output Voltage Ripple

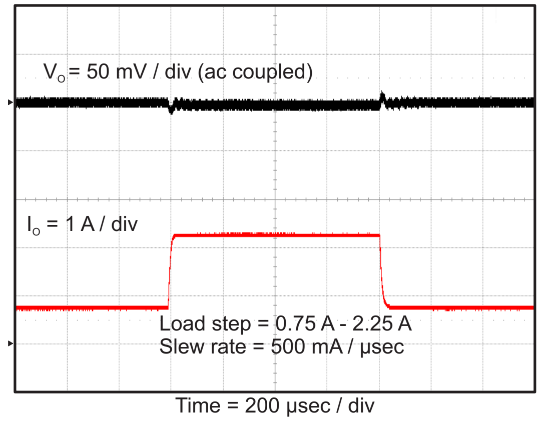


图 38. TPS563219A Transient Response

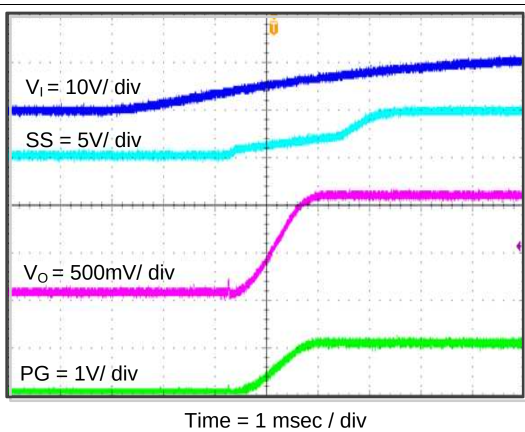


图 39. TPS563219A Start Up Relative To V_I

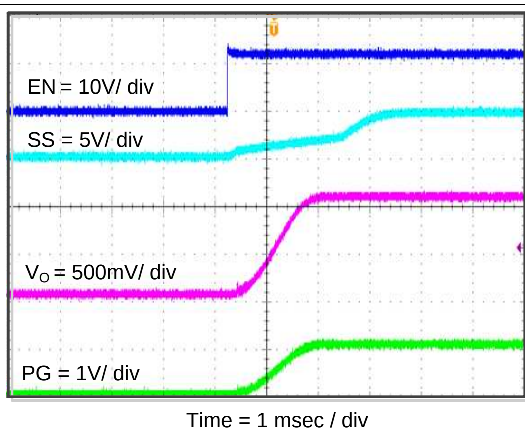


图 40. TPS563219A Start Up Relative To EN

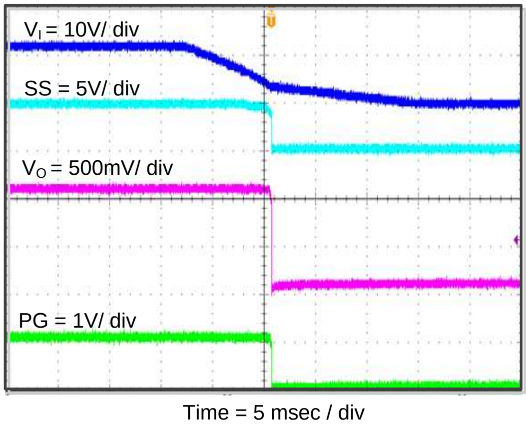


图 41. TPS563219A Shut Down Relative To V_I

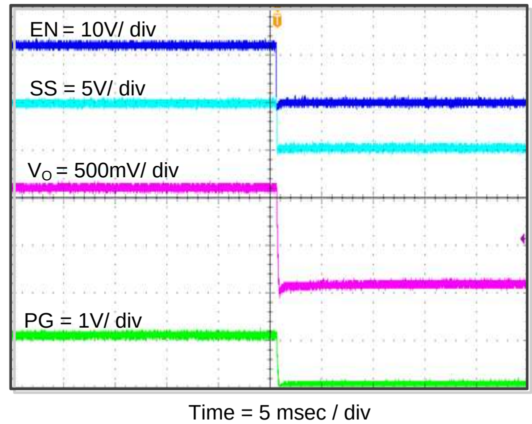


图 42. TPS563219A Shut Down Relative To EN

9 Power Supply Recommendations

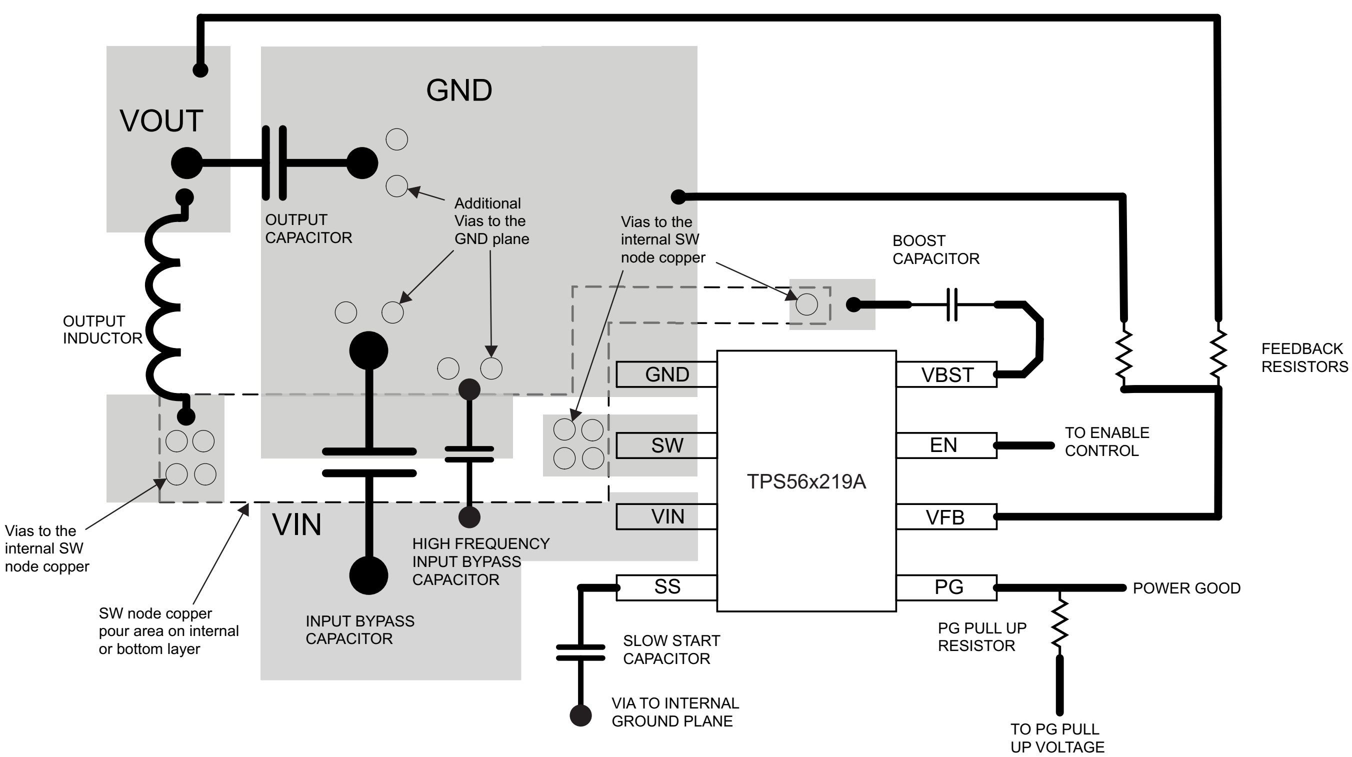
The TPS562209 and TPS563209 are designed to operate from input supply voltage in the range of 4.5V to 17V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 65%. Using that criteria, the minimum recommended input voltage is V_O / 0.65.

10 Layout

10.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example



11 器件和文档支持

11.1 器件支持

11.2 文档支持

11.3 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持和社区资源、工具和软件，以及样片或购买的快速访问。

表 **5.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS562219A	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS563219A	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.4 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.5 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 商标

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11.7 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS562219ADDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	2219A	Samples
TPS562219ADDFT	ACTIVE	SOT-23-THIN	DDF	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	2219A	Samples
TPS563219ADDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	3219A	Samples
TPS563219ADDFT	ACTIVE	SOT-23-THIN	DDF	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	3219A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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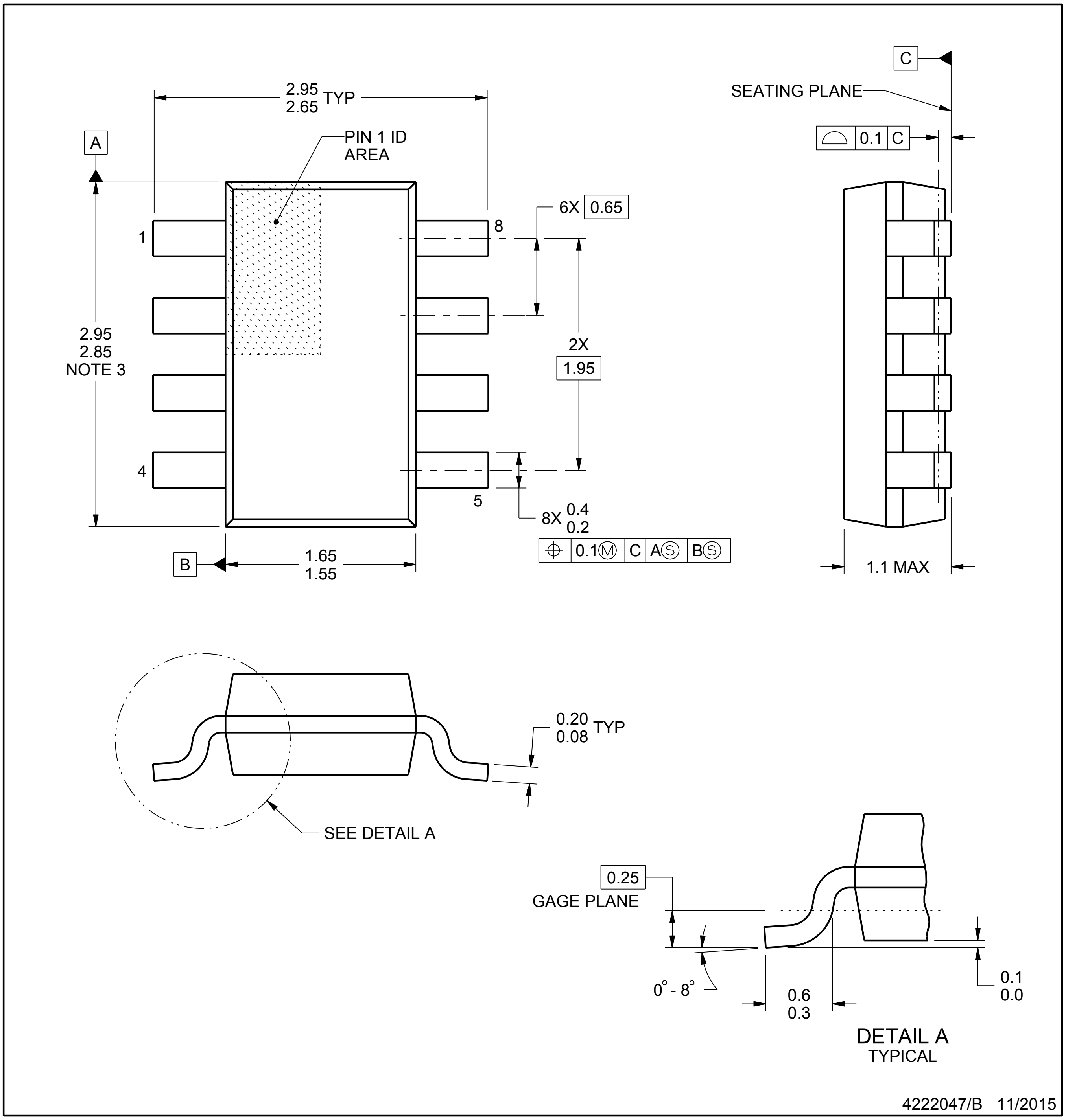
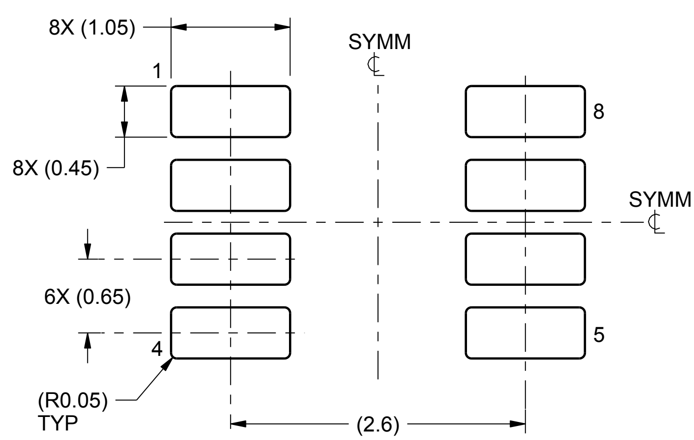
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

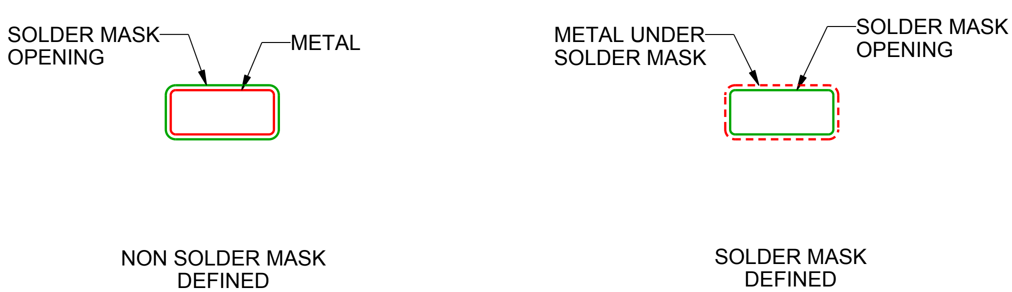


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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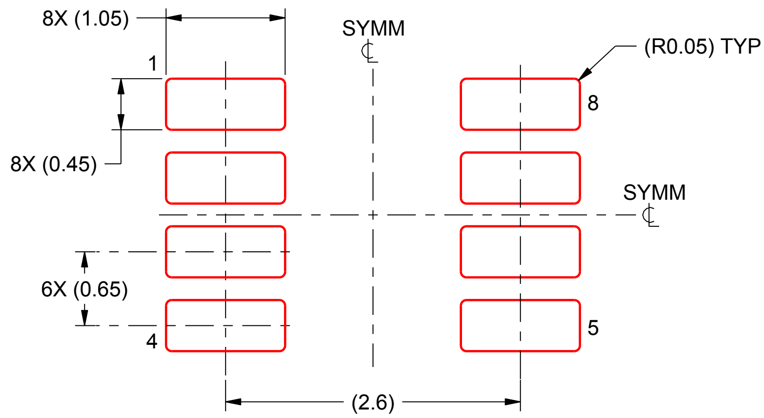
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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